Lecture 36: Power Amplifiers

* Narrowband vs. Broadband
* Linear vs. Constant Envelope operation

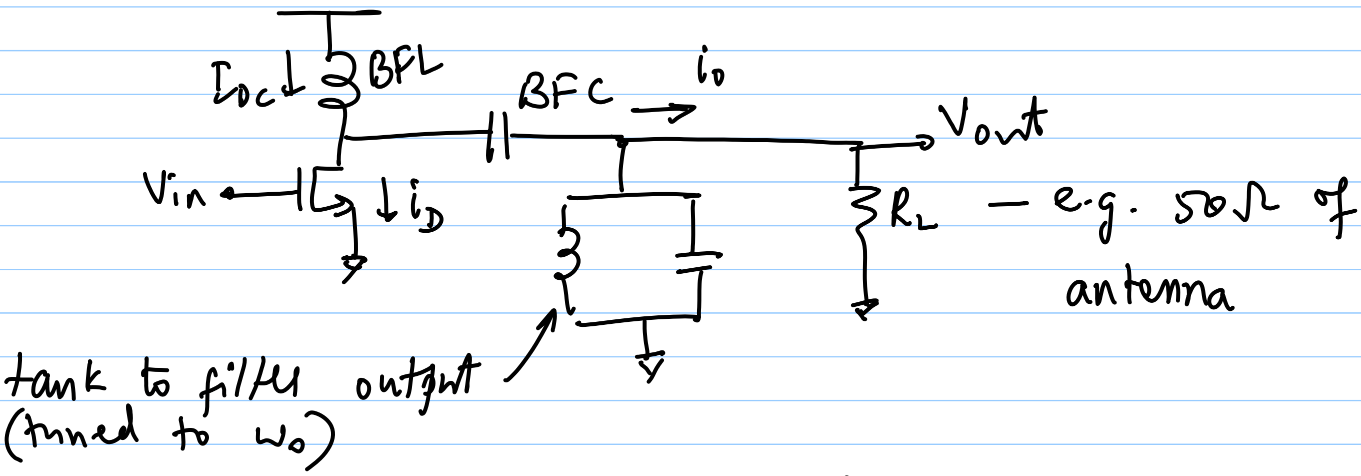
AM etc. | PM, FM etc. (usually switching PAs)

* Tradeoffs
  - → Power gain
  - → Linearity
  - → Output Power
  - → Efficiency (drain eff. & power added eff.)

Classical PAs (linear)

→ class A, AB, B, C

→ classified based on bias conditions

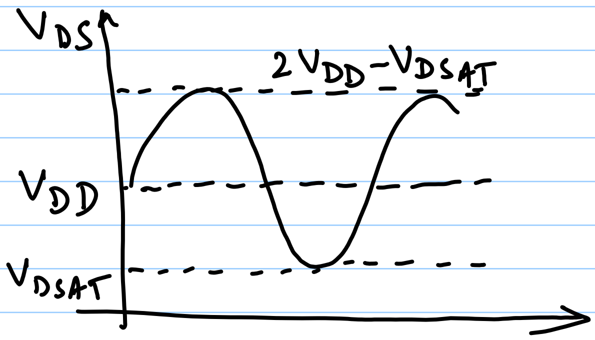


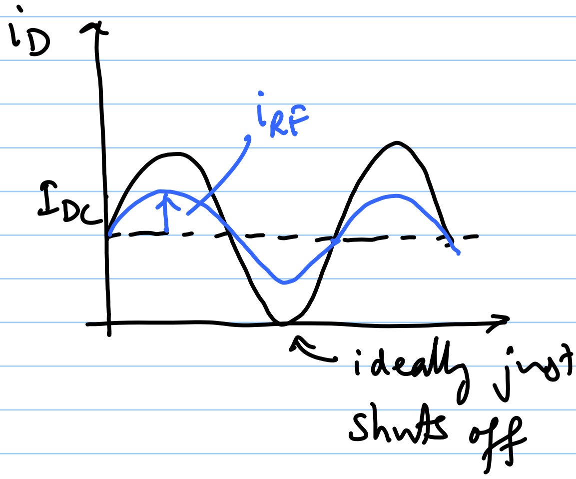
* BFC prevents DC power diss. in R_L
* BFL provides approximately constant current

* tank ckt with high Q provides linear output

I Class A

* 360° conduction angle
* $V_{in_{min.}} = V_T$





* high linearity
* poor efficiency

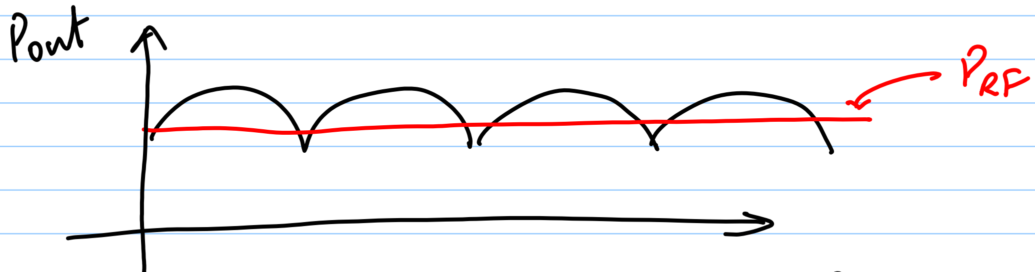
$$i_D = I_{DC} + i_{RF} \sin \omega_0 t$$

$$i_o = I_{DC} - i_D = -i_{RF} \sin \omega_0 t$$

$$V_{out} = i_o \cdot R_L = -i_{RF} R_L \sin \omega_0 t$$

$$V_{DS} = V_{DD} + i_o \cdot R_L = V_{DD} - i_{RF} \cdot R_L \sin \omega_0 t$$

$$P_{out} = i_{out} \cdot V_{out} = i_{RF}^2 R_L \sin^2 \omega_0 t$$



$$P_{RF} = (i_{RF,rms})^2 \cdot R_L = \frac{i_{RF}^2 R_L}{2}$$

P_{DC} = DC power from V_{DD}

$= V_{DD} \cdot I_{DC} = V_{DD} \cdot i_{RF}$ (assume M_1 just cuts off at lower extreme)

η = drain current efficiency

$$= \frac{P_{out}}{P_{DC}} = \frac{\frac{1}{2} i_{RF}^2 R_L}{i_{RF} \cdot V_{DD}} = \frac{1}{2} \frac{i_{RF} \cdot R_L}{V_{DD}}$$

max. value of $i_{RF} \cdot R_L = V_{DD}$ (max. swing neglecting V_{DSAT})

$\Rightarrow \eta_{max} = \frac{1}{2}$ or 50%

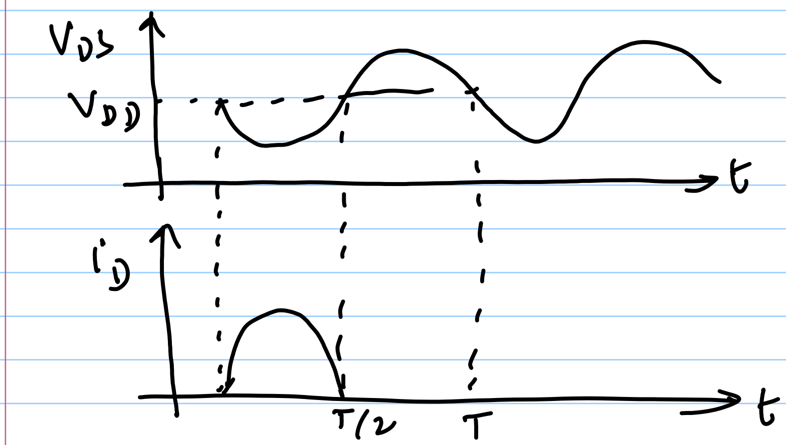
practical $\eta \sim$ 30–35%

Normalised Power output capability $\equiv P_N$

$$P_N = \frac{P_{rf}}{V_{DSpk.} \cdot i_{dpk.}} = \frac{V_{DD}^2 / 2R_L}{(2V_{DD}) \cdot \left(\frac{2V_{DD}}{R_L}\right)}$$

$= 1/8$ // High device stress

II Class B PA



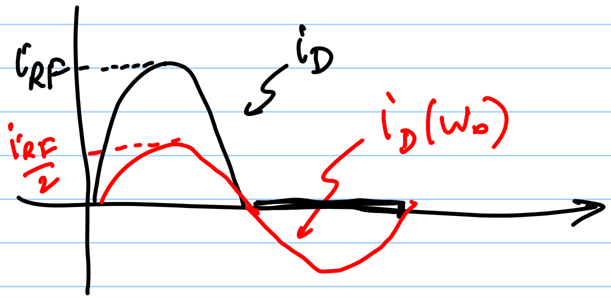
* 180° conduction angle
* current flow only when V_{DS} is small $\rightarrow$ low $P_{diss.}$

$i_D = i_{RF} \sin \omega_0 t$ for $0 - T/2$

* Tank filters out harmonics of i_D, leaving a sinusoidal voltage across R_L
* fundamental current:

$$i_D(\omega_0) = \frac{2}{T}\int_0^{T/2} i_{RF} \sin \omega_0 t \cdot \sin \omega_0 t \, dt$$

$$= \frac{i_{RF}}{2}$$



$$V_o = \frac{i_{RF}}{2} R_L \sin \omega_0 t$$

$$V_o(\max) \simeq V_{DD} \Rightarrow i_{RF}(\max.) = \frac{2V_{DD}}{R_L}$$

$$P_o(\max.) = \frac{V_{DD}^2}{2R_L}$$

$$i_{DC} = \frac{1}{T}\int_0^{T/2} \frac{2V_{DD}}{R_L} \sin \omega_0 t \, dt = \frac{2V_{DD}}{\pi R_L}$$

$$\therefore P_{DC} = i_{DC} \cdot V_{DD}$$

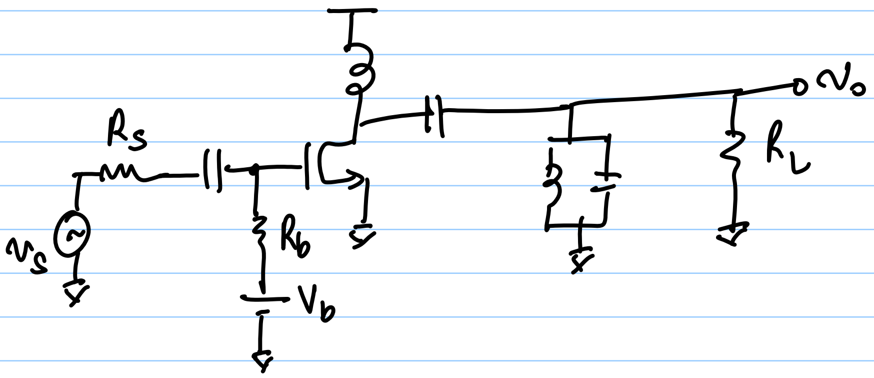
$$= \frac{2V_{DD}^2}{\pi R_L}$$

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{V_{DD}^2/2R_L}{2V_{DD}^2/\pi R_L} = \frac{\pi}{4} = 78.5\%$$

$$P_N = \frac{P_{RF}}{V_{DS(max.)}\, i_{D(max.)}}$$

$$= \frac{V_{DD}^2 / 2R_L}{2V_{DD} \cdot \frac{2V_{DD}}{R_L}} = \frac{1}{8} \quad \text{High stress}$$

With biasing:



$v_s = V_{RF} \sin \omega_0 t$

class-A

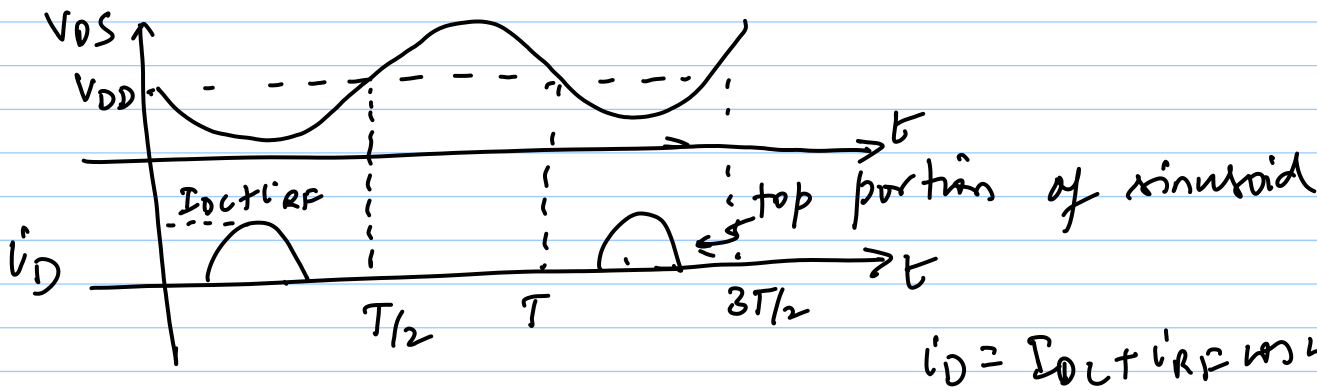
$V_b > (V_T + V_{RF})$

class-B

$V_b = V_T$

III class-C PA $\Rightarrow V_b < V_T$

conducts for $< 180°$



$i_D = I_{DC} + i_{RF} \cos \omega_0 t$

for $i_D > 0$

2Φ = conduction angle

$$\Phi = \cos^{-1}\left(\frac{-I_{DC}}{i_{RF}}\right)$$

"Bias current"

$$I_{DC} = -i_{RF} \cos \Phi$$

{ offset current is negative }

average current

$$\overline{i_D} = \frac{1}{2\pi}\int_{-\Phi}^{\Phi} (I_{DC} + i_{RF}\cos\varphi)\, d\varphi$$

$$= \frac{1}{2\pi} 2\Phi I_{DC} + \frac{1}{2\pi}(i_{RF}\sin\varphi)\Big|_{-\Phi}^{\Phi}$$

$$= \frac{i_{RF}}{\pi}\left[\sin\Phi - \Phi\cos\Phi\right]$$

fundamental :

$$i_{fund} = \frac{2}{T}\int_0^T i_D \cos w_0 t\, dt$$

$$= \frac{1}{2\pi}\left(4 I_{DC}\sin\Phi + 2 i_{RF}\Phi + i_{RF}\sin 2\Phi\right)$$

$$= \frac{i_{RF}}{2\pi}\left(2\Phi - \sin 2\Phi\right)$$

max. swing $= V_{DD}$

$$\Rightarrow \quad V_{DD} = i_{RF}\frac{R_L}{2\pi}(2\Phi - \sin 2\Phi)$$

$$\Rightarrow \quad i_{RF_{max.}} = \frac{2\pi V_{DD}}{R_L[2\Phi - \sin 2\Phi]}$$

$$\Rightarrow \quad i_{D pk.} = i_{RF_{max.}} + I_{DC}$$

$$= \frac{2\pi V_{DD}}{R_L(2\Phi - \sin 2\Phi)}\left[1 + \frac{\sin\Phi - \Phi\cos\Phi}{\pi}\right]$$

$$\Rightarrow \quad \eta_{max.} = \frac{2\Phi - \sin 2\Phi}{4(\sin\Phi - \Phi\cos\Phi)}$$

as $\Phi \to 0$, $\eta \to 100\%$

but gain & $P_{out} \to 0$

* We can obtain high efficiency at the expense of linearity, gain & P_{out}

Switching PAs

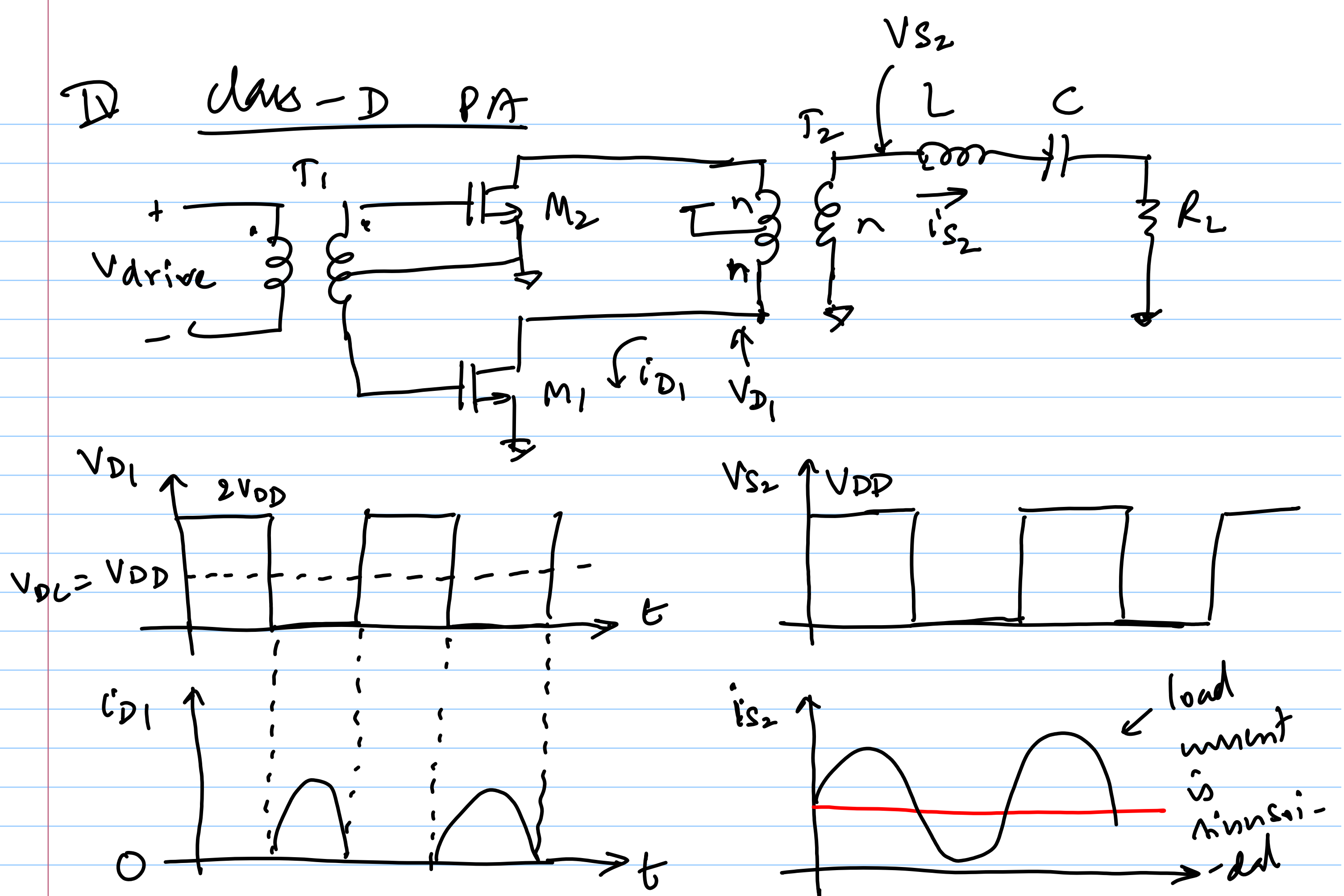
Basic Principle: Use MOSFET as a switch rather than as a controlled current source in the case of linear PAs

ideal switch ON $\Rightarrow$ $V=0$, $I>0$ Power $=0$

OFF $\Rightarrow$ $V>0$, $I=0$ Power $=0$

no loss in switch $\Rightarrow$ 100% efficiency

IV class-D PA



You can show that:

normalised power handling capability

$$P_N = \frac{P_{out}}{V_{DSpk} \cdot i_{Dpk}} = \frac{1}{\pi}$$ ← much lower stress than linear PAs

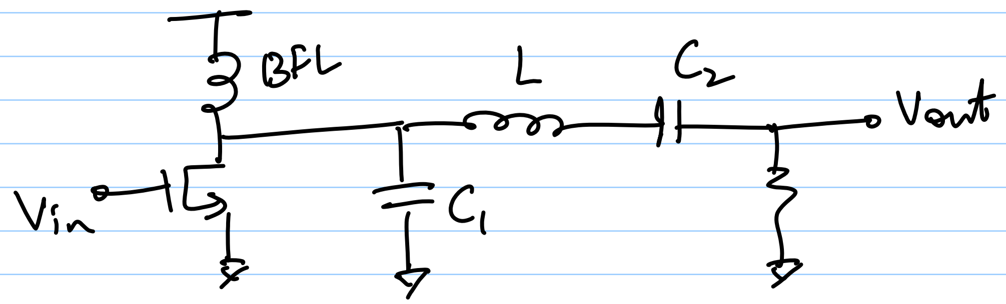
ideal $\eta = 100\%$

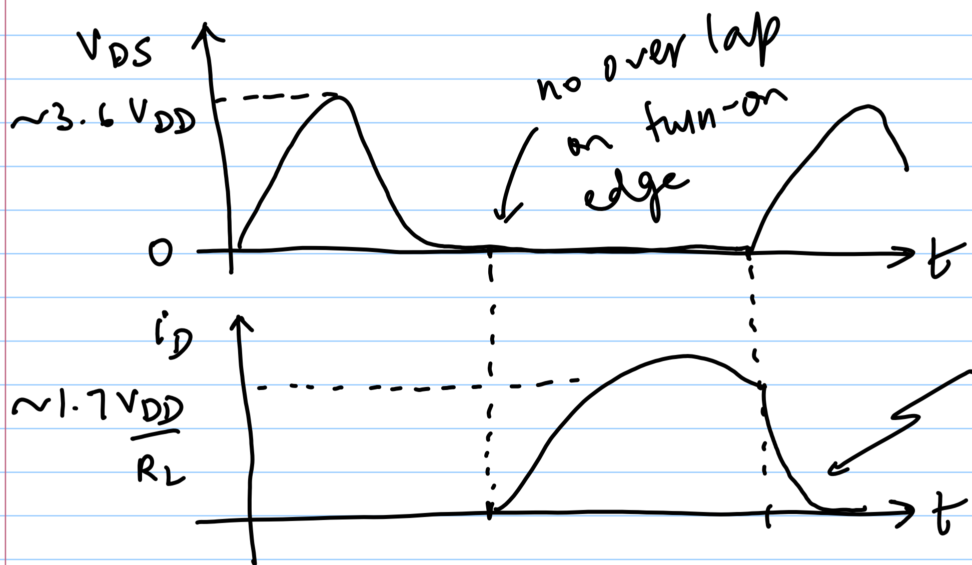
Practical: switches must be very fast relative to ω_0, otherwise $\eta < 100\%$.

V Class-E PAs

key ideas * switch voltage = 0 before current flows

* use higher order filter to shape the pulses





turn-off transient may not be as good (esp. BJT PA)

Ref: Sokal & Sokal, JSSC June 1975

Design Equations

$$L = \frac{Q R_L}{\omega}$$

$$C_1 = \frac{1}{\omega R_L \left(\frac{\pi^2}{4}+1\right)\left(\frac{\pi}{2}\right)} \simeq \frac{1}{5.447\, \omega R_L}$$

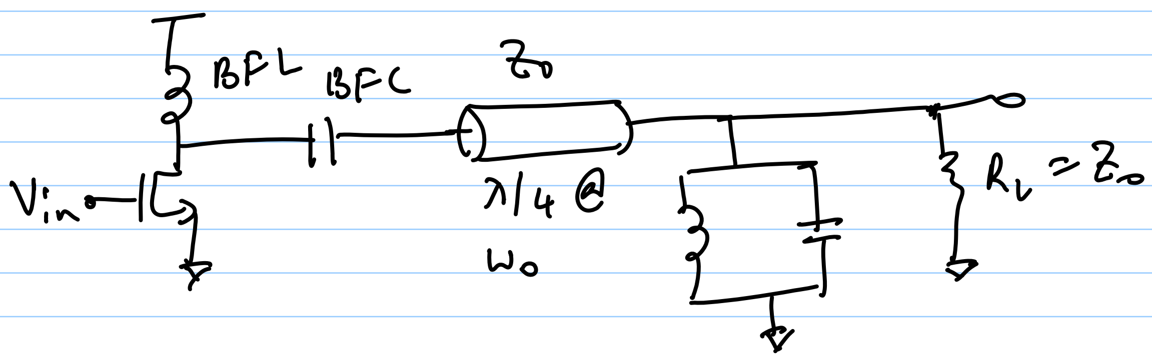
$$C_2 \simeq C_1 \left(\frac{5.447}{Q}\right)\left(1 + \frac{1.42}{Q-2.08}\right)$$

$$P_{out}\,(\text{max.}) = \frac{2}{1+\pi^2/4} \cdot \frac{V_{DD}^2}{R_L} \simeq 0.577 \frac{V_{DD}^2}{R_L}$$

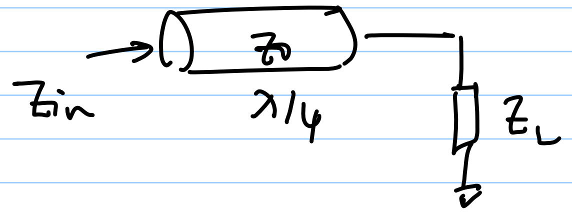
$$P_N = \frac{P_o}{V_{DS_{pk}} \cdot i_{D_{pk}}} \simeq 0.098 \leftarrow \text{high stress}$$

note that
$$\left.\begin{aligned} V_{DS_{pk}} &= 3.6\, V_{DD} \\ i_{D_{pk}} &= 1.7 \frac{V_{DD}}{R_L} \end{aligned}\right\} \text{very high values}$$

VI Class-F PAs



$\lambda/4$ Xfmr



$$Z_{in} = \frac{Z_0^2}{Z_L}$$

here $Z_{in} = R_L$ @ w_0

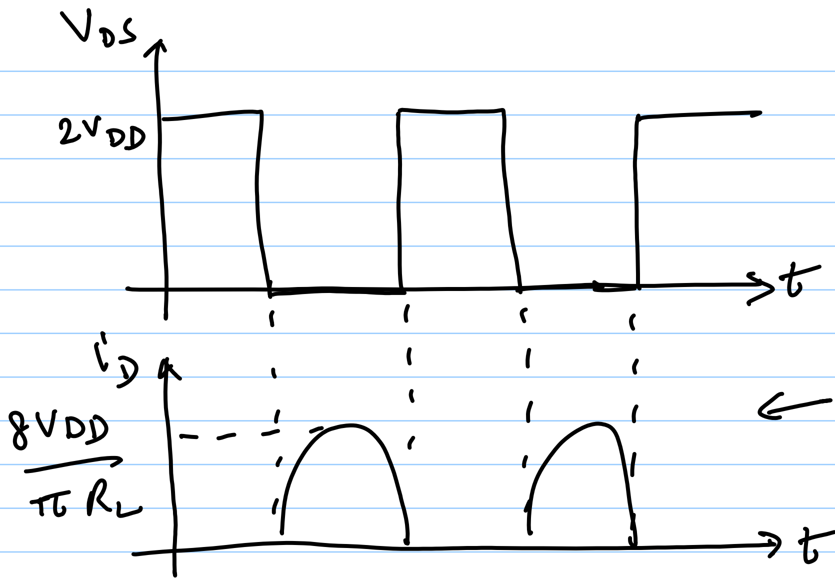
LC tank $\Rightarrow$ $Z(w) = 0$ for $w \neq \omega_0$ (short ckt)

@ $w = 2n w_0$, T-line $l = 2n\frac{\lambda}{4} = n\frac{\lambda}{2}$

$\Rightarrow$ short ckt. @ Drain

@ $w = (2n+1) w_0$, T-line $l = (2n+1)\lambda/4$

LC-tank short ckt $\Rightarrow$ open ckt. @ Drain



$\leftarrow$ sinusoidal current pulses into drain

$$v_{fund.} = \frac{4}{\pi}(V_{DD})$$

$$P_o = \left[\frac{4}{\pi}\left(\frac{V_{DD}}{\sqrt{2}}\right)\right]^2 \cdot \frac{1}{R_L} = \frac{8V_{DD}^2}{\pi^2 R_L}$$

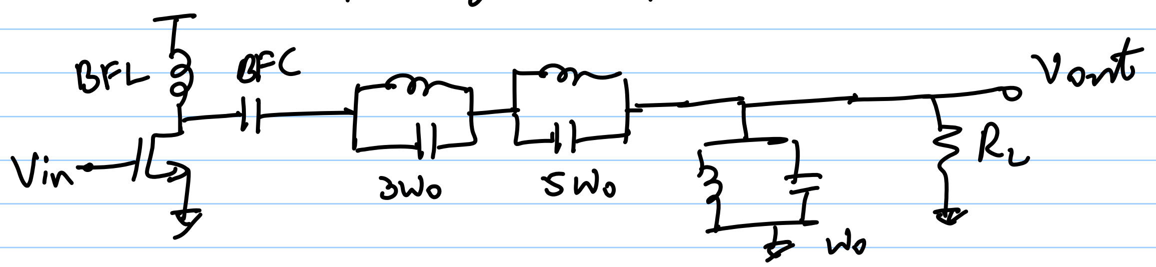
$$\eta_{ideal} = 100\%$$

in practice $\eta > \eta_{class-E}$

$$P_N = \frac{P_o}{V_{DS_{pk.}} \cdot i_{D_{pk.}}} = \frac{8V_{DD}^2/\pi^2 R_L}{2V_{DD} \cdot \frac{8V_{DD}}{\pi R_L}}$$

$$= \frac{1}{2\pi} \approx 0.16 \quad \text{(better than class-E)}$$

alternative topology: replace T-lines with L-C



* Note: Switching PAs are <u>constant envelope</u> PAs

$V_{out} = f(V_{DD})$, & not $f(V_{in})$

<u>Other design considerations</u>:

1) Power-added Efficiency:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}$$

obviously $PAE < \eta$

→ takes power gain into account

2) stability: * C_{gd} is very important (layout)

* stability-gain trade off

3) Breakdown

* output swings upto $2V_{DD}$
* BV reduces as tech. scales
  - → DB & SB diode breakdown (A)
  - → D-S punchthrough (B)
  - → Time-dependent dielectric breakdown (TDDB) (C)
  - → Gate oxide rupture (D)

(A) : Diode BV ~ few V (2-3X V_{DD})

(B) : If V_D is large, depletion region extends to source, eliminating the channel

(C) : Gate oxide damage due to energetic carriers – @ high fields, high energy e⁻s create oxide traps ; charge trapped here shift device V_T (cumulative)

(D) : Gate oxide rupture occurs @ high gate fields

4) Large-Signal impedance matching