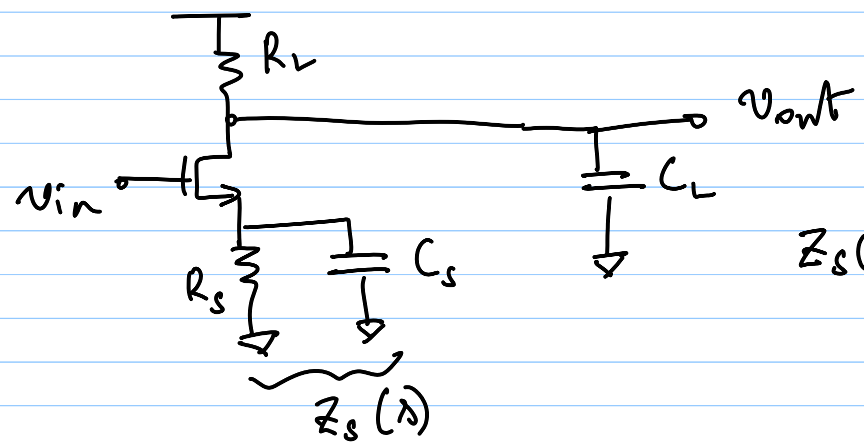
Lecture 35 : Wideband Amplifiers – II

VII Zero-peaked C.S. Amplifier



$$Z_s(s) = R_s \,||\, \frac{1}{sC_s} = \frac{R_s}{1 + sC_sR_s}$$

$$G_m(s) = \frac{g_m}{1 + g_m Z_s(s)}$$

$$Z_L(s) = \frac{R_L}{1 + sC_LR_L}$$

$$\Rightarrow \quad G_m(s) = \frac{g_m}{1 + \dfrac{g_mR_s}{1+sC_sR_s}}$$

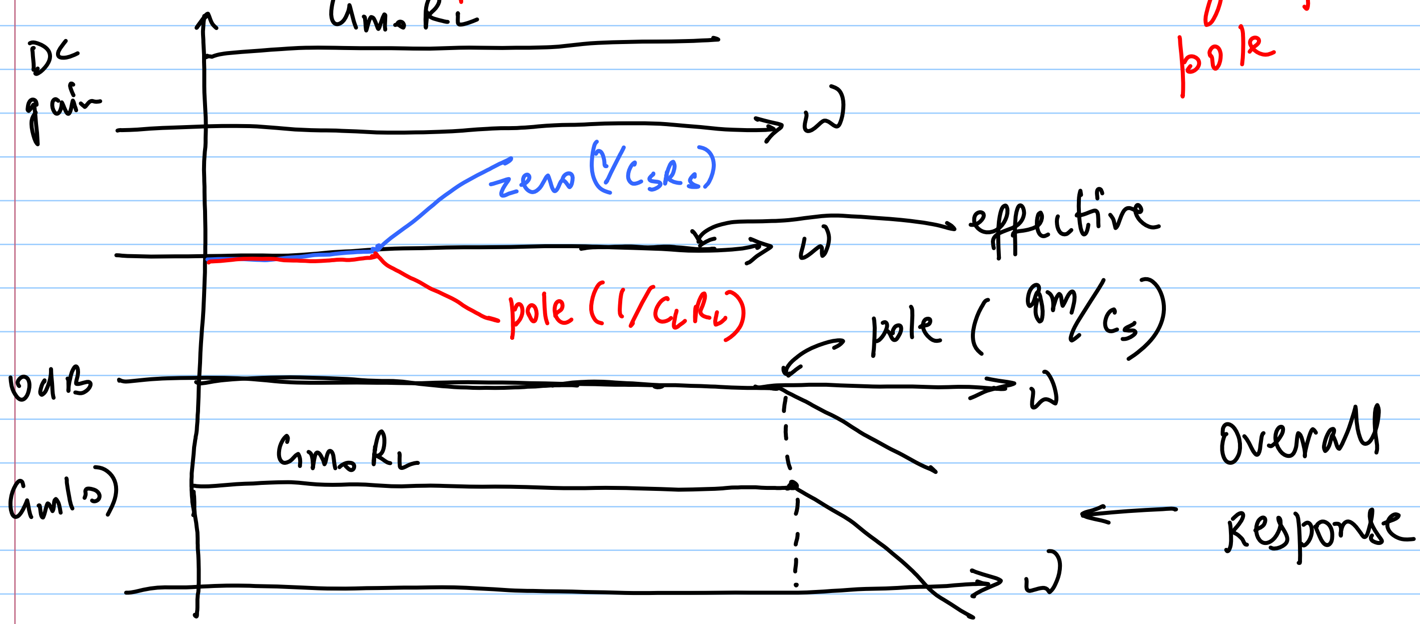
$$= \frac{g_m}{1+g_mR_s} \cdot \frac{1+sC_sR_s}{1 + sC_s\left(\dfrac{R_s}{1+g_mR_s}\right)}$$

$$\simeq G_{m0} \cdot \frac{1+sC_sR_s}{1 + sC_s/g_m} \qquad \{g_mR_s \gg 1\}$$

$$A_v(s) = G_m(s) \cdot Z_L(s)$$

$$= G_{m0} \cdot \frac{1+sC_sR_s}{1+sC_s/g_m} \cdot \frac{R_L}{1+sC_LR_L}$$

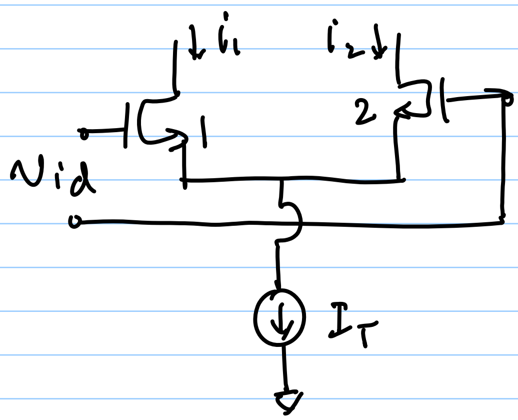
$$= \underbrace{(G_{m0} R_L)}_{\text{DC gain}} \underbrace{\left[\frac{1+s C_S R_S}{1+s C_L R_L}\right]}_{\text{pole-zero cancellation}} \cdot \underbrace{\left[\frac{1}{1+\frac{s C_S}{g_m}}\right]}_{\text{high freq. pole}}$$



f_T -doublers

$$\omega_T = 2\pi f_T = \frac{g_m}{C_{gs}+C_{gd}} \approx \frac{g_m}{C_{gs}} = \frac{g_m}{C_{in}}$$

(i) Diff-pair :



$i_{od} = i_1 - i_2$

$g_{md} = g_{m1,2}$ unchanged

$C_{id} = (C_{gs1})\text{series}(C_{gs2})$

$= \frac{C_{gs1,2}}{2}$

$\Rightarrow f_T' \approx 2 f_T$

remember that for a single transistor

$$f_T = \frac{g_m}{C_{gs}} \propto \sqrt{I_{bias}} \quad \text{(long-channel)}$$

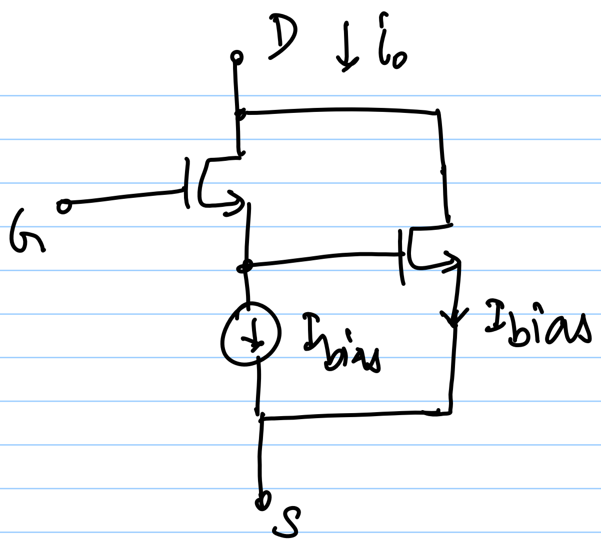
$$I_{bias} \rightarrow 2I_{bias} \Rightarrow f_T \rightarrow 1.41 f_T \quad \text{(best case)}$$

But diff. pair : $2I_{bias} \Rightarrow f_T' = 2f_T$

* Diff signal path may not be convenient

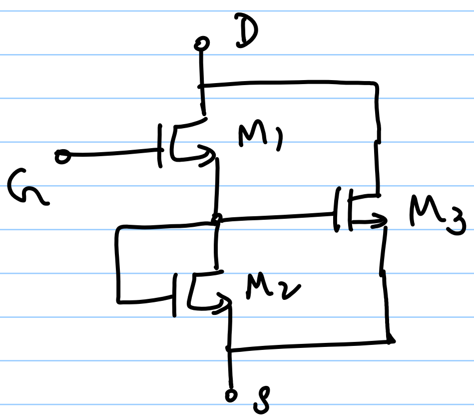
(ii) Single-ended f_T-doubler (similar to Darlington pair)

* interchange G & S connections on one of the diff pair devices & sum the outputs



* Both devices are biased at I_{bias}

$\Rightarrow$



Battjes f_T doubler (Tektronix)

* M_2–M_3 is a current mirror $\Rightarrow$ equal I_{bias}

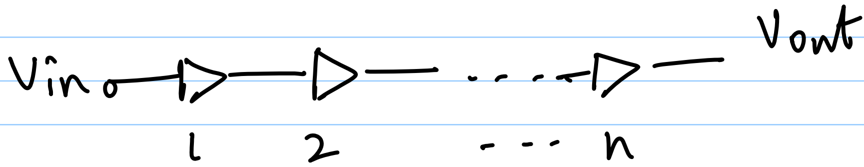
but C_{gs_2} & C_{gs_3} are in parallel

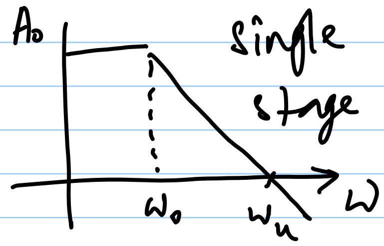
$$\Rightarrow \quad C_{as} = (C_{gs_1}) \text{ series } (C_{gs_2} \parallel C_{gs_3})$$

$$f_T' \approx (1.5)\, f_T$$

* f_T -doublers will not work well if C_{is} limited by other factors
  - → load cap C_L
  - → parasitic C_{SB} cap

Cascaded Amplifiers





* All n amplifiers are identical
* Each stage has single-pole response

$$A(s) = \frac{A_0}{1 + s/\omega_0}$$

overall cascade TF is

$$H(s) = \left(\frac{A_0}{1 + s/\omega_0}\right)^n$$

* find -3dB BW of the cascade (ω_{on}):

at $\omega = \omega_{on}$, $|H(j\omega)| = \frac{1}{\sqrt{2}} |H(0)|$

$$\Rightarrow \left[\frac{A_0}{\sqrt{1+\left(\frac{\omega_{on}}{\omega_o}\right)^2}}\right]^n = \frac{1}{\sqrt{2}} A_0^n$$

$$\Rightarrow \boxed{\omega_{on} = \omega_o \sqrt{2^{1/n}-1}}$$

BW shrinkage

Recall that $A_0 \omega_o = \omega_u \Rightarrow \boxed{\omega_{on} = \frac{\omega_u}{A_0}\sqrt{2^{1/n}-1}}$

a) BW shrinkage

* as $n \to \infty$, $\omega_{on} \to 0$
* as $n \to \infty$, DC gain $A_{on} = A_0^n \to \infty$
* we want to find approximate expression for ω_{on} as $f(n)$

$$2^{1/n} = \exp\left\{\ln\left(2^{1/n}\right)\right\} = \exp\left\{\frac{1}{n}\ln 2\right\}$$

for large n, we the first two terms in expansion

$$\exp\left\{\frac{1}{n}\ln 2\right\} \simeq 1 + \frac{1}{n}\ln 2$$

$$\Rightarrow \omega_{on} \simeq \omega_o \sqrt{\frac{1}{n}\ln 2} \simeq \frac{0.833\, \omega_o}{\sqrt{n}} \quad //$$

* i.e. BW shrinks as $1/\sqrt{n}$ for large n
* $n \geq 4 \Rightarrow$ error $< 5\%$

b) Optimum gain per stage

* Given total gain $A_{tot.}$, we want to find optimal n & maximize BW

$$A_0^n = A_{tot.} \Rightarrow A_0 = A_{tot.}^{1/n}$$

$$\omega_{on} = \frac{\omega_u}{A_{tot.}^{1/n}} \sqrt{2^{1/n} - 1}$$

apply $\frac{d\omega_{on}}{dn} = 0$

after some algebra:

$$n_{opt.} = \frac{\ln 2}{\ln\left\{1 + \frac{\ln 2}{2 \ln A_{tot.}}\right\}}$$

for large $A_{tot.}$,

$$\ln\left\{1 + \frac{\ln 2}{2 \ln A_{tot.}}\right\} \approx \frac{\ln 2}{2 \ln A_{tot.}}$$

$$\ln(1+x) \approx x \quad \text{for} \quad x << 1$$

$$\Rightarrow \boxed{n_{opt.} \approx 2 \ln A_{tot.}}$$

optimum gain/stage:

$$A_{o_{opt.}} = (A_{tot.})^{1/n_{opt}} = \exp\left\{\frac{1}{n_{opt.}} \ln A_{tot.}\right\}$$

$$\approx e^{1/2}$$

$$\boxed{A_{o,opt.} = \sqrt{e}}$$

optimum BW:

$$\omega_{on,opt.} = \frac{\omega_u}{A_{tot.}^{1/n_{opt.}}} \sqrt{2^{1/n_{opt.}} - 1}$$

$$\approx \frac{\omega_u}{\sqrt{e}} \left[\exp\left\{\frac{1}{n_{opt.}} \ln 2\right\} - 1\right]^{1/2}$$

$$\boxed{\omega_{on,opt.} \approx \omega_u \sqrt{\frac{\ln 2}{2e \ln A_{tot.}}}}$$

$$\omega_{on,opt.} \approx \frac{0.357\,\omega_u}{\sqrt{\ln A_{tot.}}}$$

in other words,

* $BW \times \sqrt{\ln G}$ = constant
* If $A_{tot.} \rightarrow A_{tot.} \times 100$, $BW \rightarrow < BW \times 2$
* Overall amp does not have constant GBW product (obviously, because GBW is constant only for single-pole systems)

* GBW product for this cascaded amp

$$= A_{tot} \cdot \omega_{on}$$

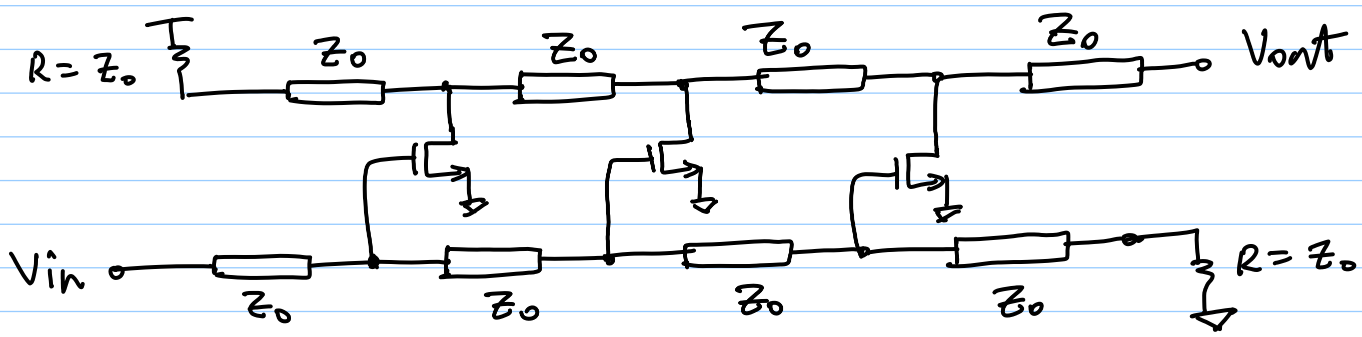
$$= A_{tot} \cdot \frac{0.357\omega_n}{\sqrt{\ln(A_{tot})}} \Rightarrow \text{increases without bound}$$

G-BW-delay Tradeoff

* Delay is less important in systems with 1-way comm. (e.g. TV, optical fibre comm.)
* Coupling between G & BW is weak for higher order cascaded systems
* If delay can be arbitrary, what G or B can be achieved?

* recall: $BW \propto \frac{1}{\text{rise time}}$
* imagine an amp that stores energy in input step for a long time, then dumps it suddenly into an output $\Rightarrow$ very fast rise time $\Rightarrow$ high BW

Distributed Amplifier (Travelling Wave Amp.)



* inputs to transistors supplied by tapped delay line
* output fed into another tapped delay line
* Assume input has a voltage step.
  → after a delay through each line, it appears at transistor inputs
  → each transistor generates current equal to $g_m \times$ input step
  → currents of all transistors sum coherently in time, if delays of input & output line are matched

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* at each point of the tapped delay line, $Z_{in} = Z_0/2$
* Overall gain $\boxed{A_v = \frac{n \cdot g_m \cdot Z_0}{2}}$ for n stages
  → $A_v \propto n$
  → $A_v > 0$ if $g_m > 0$
  → BW does not factor directly into tradeoff
  → assume that C_{in} & C_{out} of transistors are absorbed into RLGC of TDL
  → $C_{in} > C_{out} \Rightarrow$ matching between TDLs is difficult $\{C_{gs} > C_{db}\}$

* Can be power-hungry
* TDLs can be replaced by lumped LC equivalents (artificial T-lines)
* Main advantage: You can achieve significant gain @ freq. close to f_T
* high gain & low NF not possible
* area is large
* Z_0's for G & D T-lines need not be the same
* If T-lines are lossy, $A_v \Rightarrow 0$ as $N \Rightarrow \infty$

→ Vin on gate line decays exponentially
→ A_v increases linearly with n
⇒ $n_{opt.}$ exists for a given set of TDL's and MOSFETs.

<u>Artificial T-lines</u>

* has BW limitation because of lumped LC (ideal lossless TDL has no BW limitation)
* $T_{Delay} = \sqrt{LC}$ per LC-section
  (ideal TDL $T_{del.} = \sqrt{LC} \cdot z$, z = length)

* $Z_{in} = \frac{j\omega L}{2}\left[1 \pm \sqrt{1 - \frac{4}{\omega^2 LC}}\right]$

$\Rightarrow \omega_{cutoff} = \frac{2}{\sqrt{LC}}$ ← cutoff frequency

* choose L & C for
  - → min. loss & attenuation
  - → $\omega_{cut\text{-}off}$ > required BW
  - → desired T_{Delay}
  - → constant group delay (min. dispersion)

* for a lossy line, constant G.D. ⇒ $RC = GL$

$\Rightarrow \frac{L}{R} = \frac{C}{G}$ equal time constants