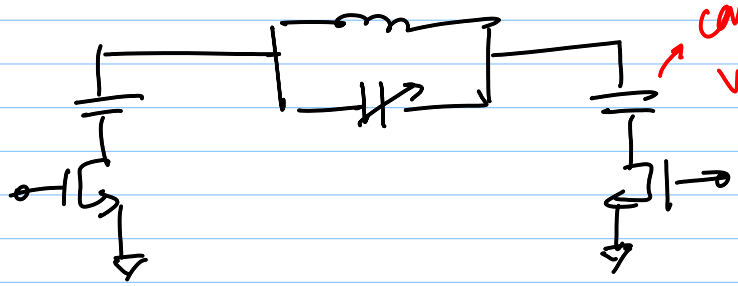
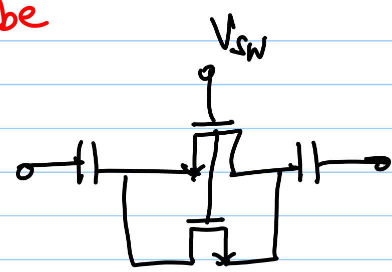
Lecture 33: VCO Design (cont.)

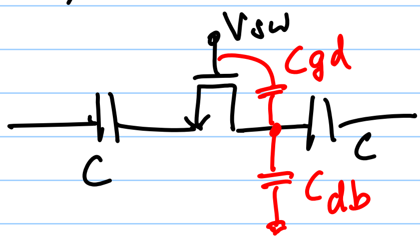


can also be varactors

⇒



(in case there is S/D asymmetry)



$$\left.\begin{aligned} C_{max} &= C \quad (V_{SW} = ON) \\ C_{min} &= C \text{ series } (C_{gd} + C_{db}) \\ &\approx C_{gd} + C_{db} \quad (V_{SW} = OFF) \end{aligned}\right\}$$

$C_{par.} \propto W$

$Q \propto W$

⇒ trade-off between Q & Tuning range

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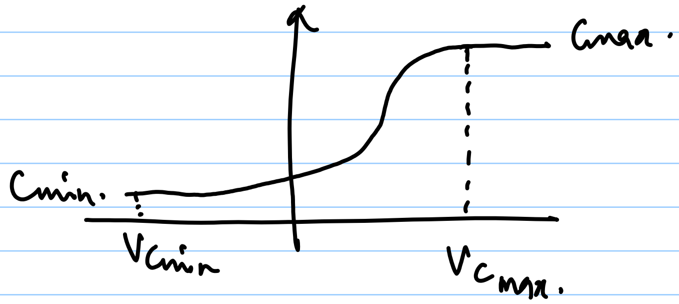
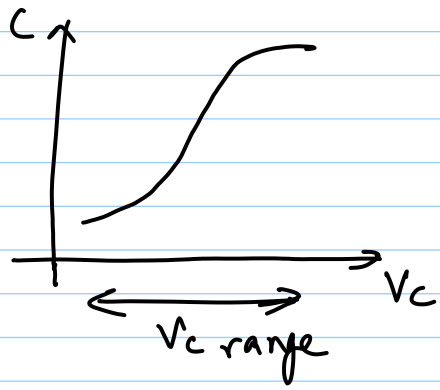
* Varactor may require re-biasing

e.g. from $\Delta V = (V_{DD} - V_C)$ to $(V_B - V_C)$

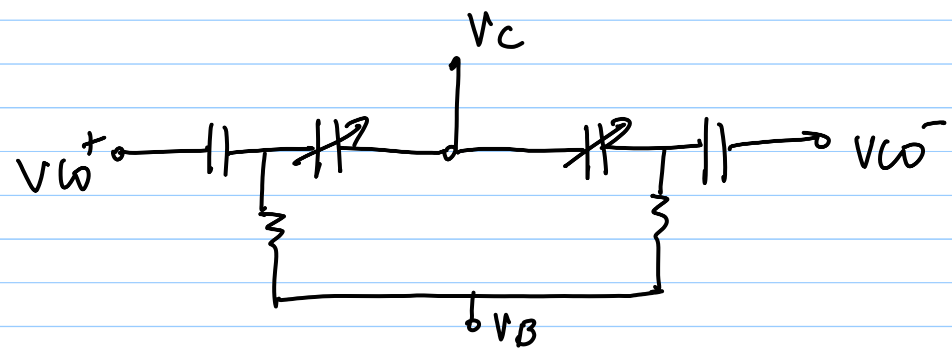


but we want }

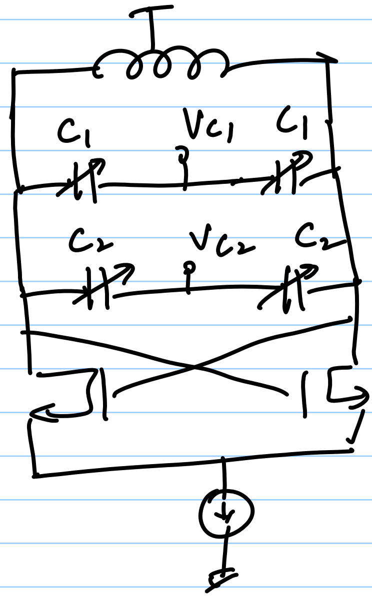


← −ve voltages are undesirable

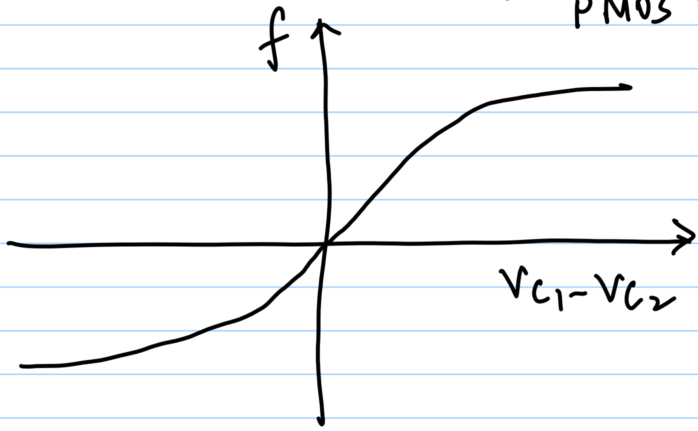
⇒



* differential Tuning also possible

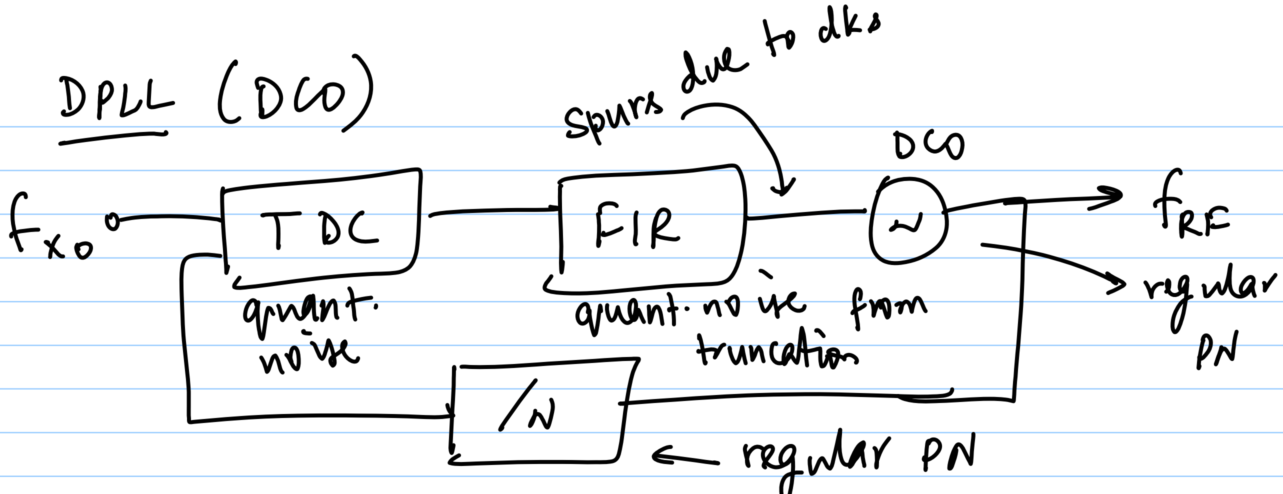


e.g. use NMOS & PMOS varactors



* larger linear V_c range
* C_1, C_2 slopes are different
  $\Rightarrow$ non-linearities

DPLL (DCO)



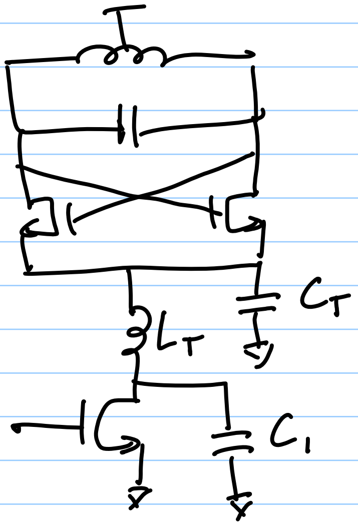
* No analog tuning
* f_{RF} needs very fine tuning
  $\Rightarrow$ extremely small switchable C needed

e.g. 2kHz resolution @ 3.6GHz

$C_{tank} = 4.5pF$, $L = 0.5nH \Rightarrow \Delta C = 5aF$ $(5\times10^{-18}F)$

Tail current filtering

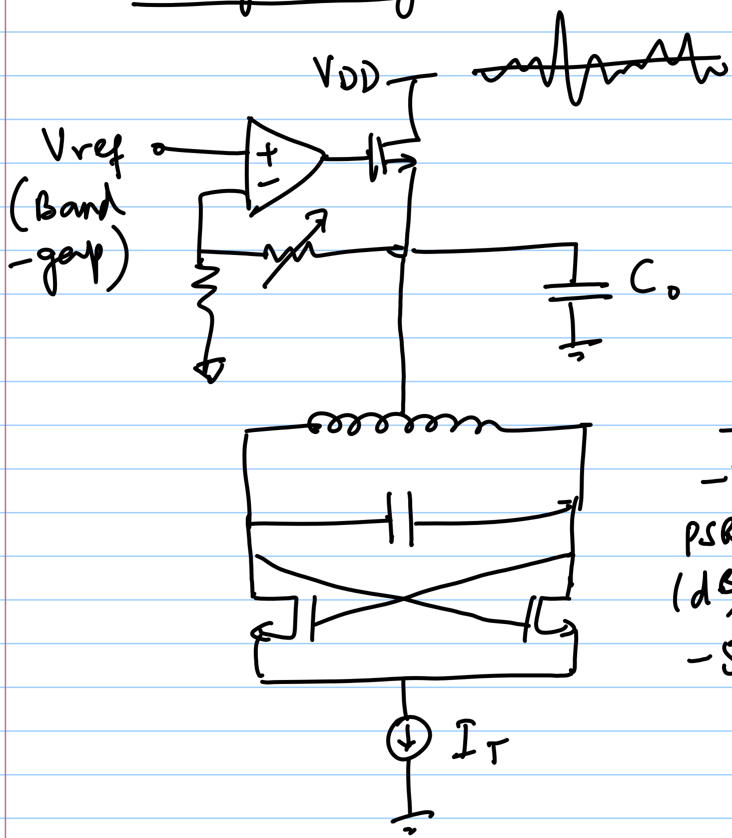
* popular technique, many variations

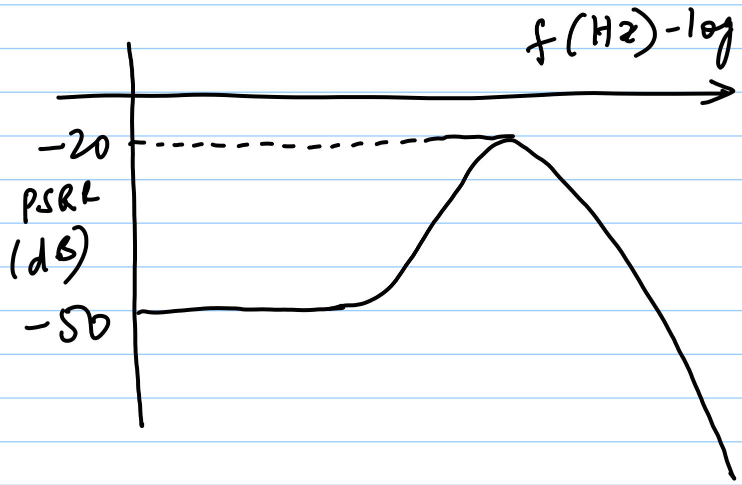


* resonate L_T, C_T @ $2\omega_0$
  → high impedance @ $2\omega_0$
  → filters out noise folding down from $2\omega_0$
* C_1 = large
  → filters out bias noise
* extra L_T needed

Voltage Regulator

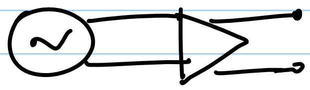
DC-DC converter has large noise, spurs

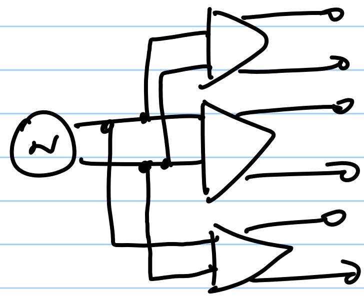




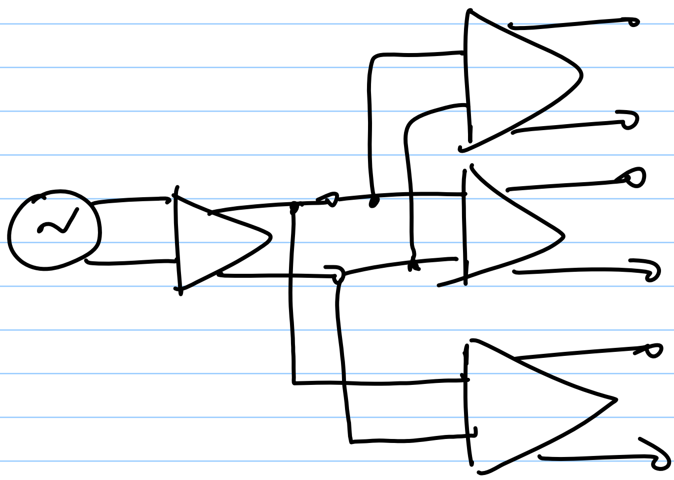
* Ensure regulator does not deteriorate PN
(i.e. VCO - regulator co-design)
* Regulator power consumption must be kept low

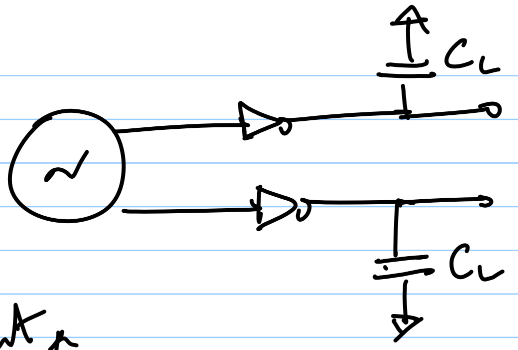
__Buffers__ - several configs possible


single set of diff outputs


3 sets of outputs
* extra cap loading on VCO
⇒ tuning range reduced

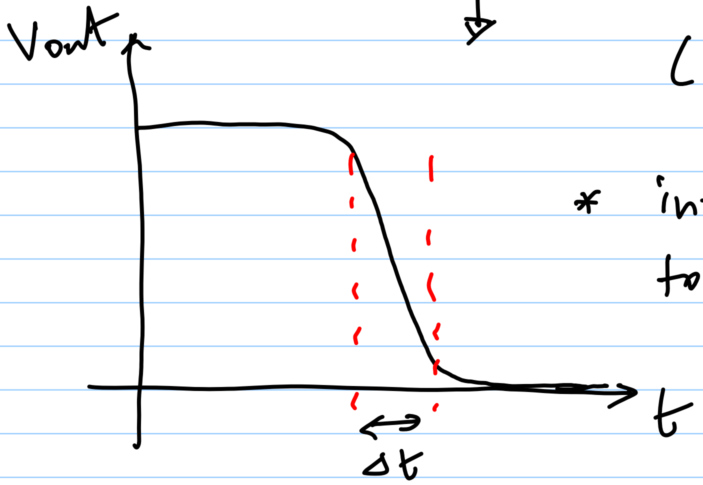
very long routings or many in parallel
⇒ use 2-stage


* also reduces kickback from load ckt>ry (e.g. dividers)



* pseudo-differential
* low-noise
* 0 - V_{DD} outputs

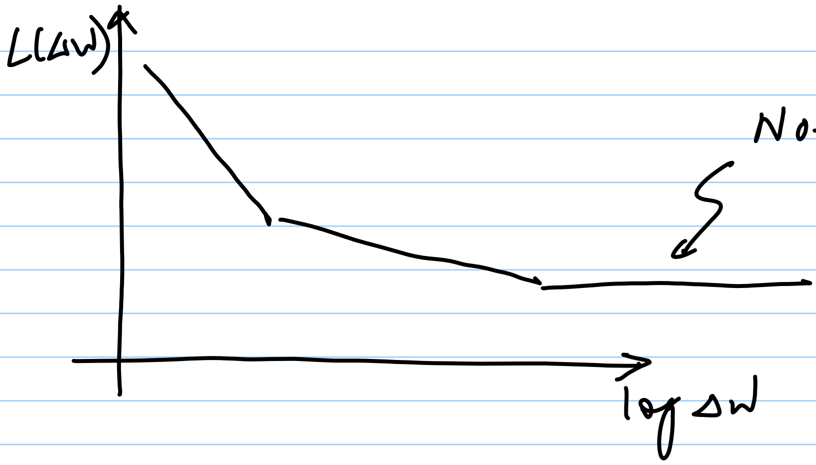
(dividers are often digital)



* inverter is most sensitive to noise during Δt

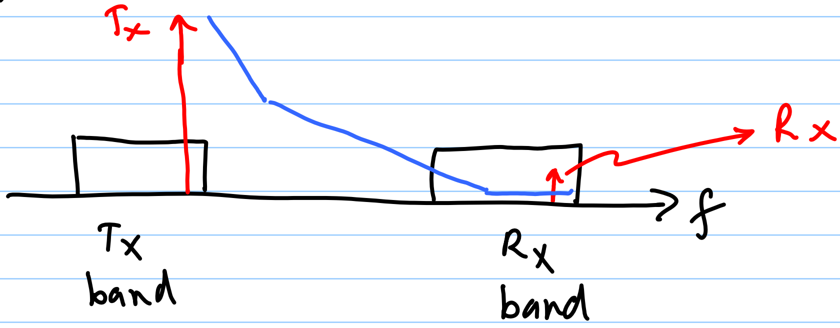
large C_L + narrow Δt ⇒ large inverters

⇒ high P_{diss}.

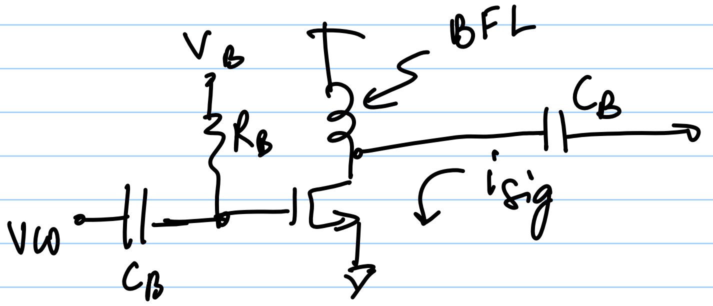


Noise floor dominated by buffer noise

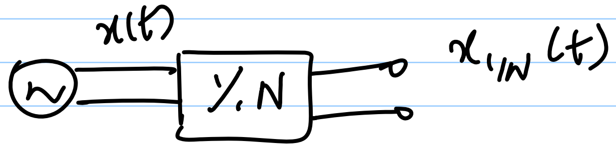
e.g. WCDMA (duplex, Rx, Tx on at same time)



high-freq. VCOs: may need "open-drain" buffers



Effect of freq. division on PN



* freq. & phase have a linear relationship

$$f \Rightarrow f/N \Rightarrow \varphi = \varphi/N$$

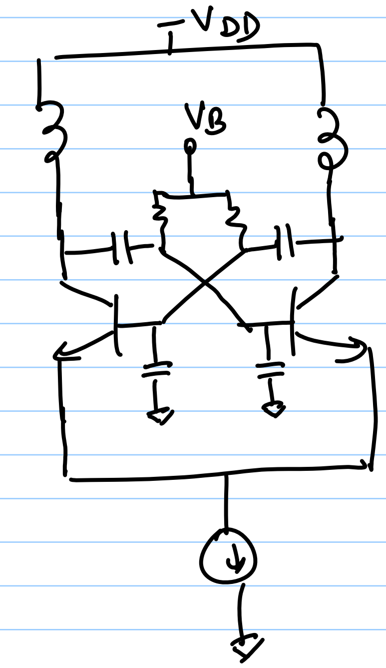
$$x(t) = A\cos(\omega_0 t + \varphi_n(t))$$

$$x_{1/N}(t) = A\cos\left(\frac{\omega_0}{N}t + \frac{\varphi_n(t)}{N}\right)$$

$\Rightarrow$ PN magnitude at a given offset $\rightarrow 1/N$

$\Rightarrow$ PN power $\rightarrow 1/N^2$ $\{$narrowband FM approx.$\}$

Bipolar VCOs



* bipolar $V_{BE} \sim 0.7V$
→ cap. divider allows larger swings @ o/p
* feedback also possible using Xfmrs.

VCO Design

1) Maximise Tank Q (i.e. highes R_p)
2) Maximise output swing, but don't saturate VCO {choose I_T carefully}
3) Startup gain of ~ 2-3
4) Use minimum lengths to maximise tuning range (but keep $1/f^3$ noise in mind)

5) $R_p = \omega_0 L Q$ & $V_0 = \frac{2}{\pi} I_T R_p$

$\Rightarrow$ maximise L & Q at the same time for min. PN & min P_{Diss}

6) Choose between

NMOS-only

PMOS-only

Complementary

Colpitts (differential)

Hybrid structures