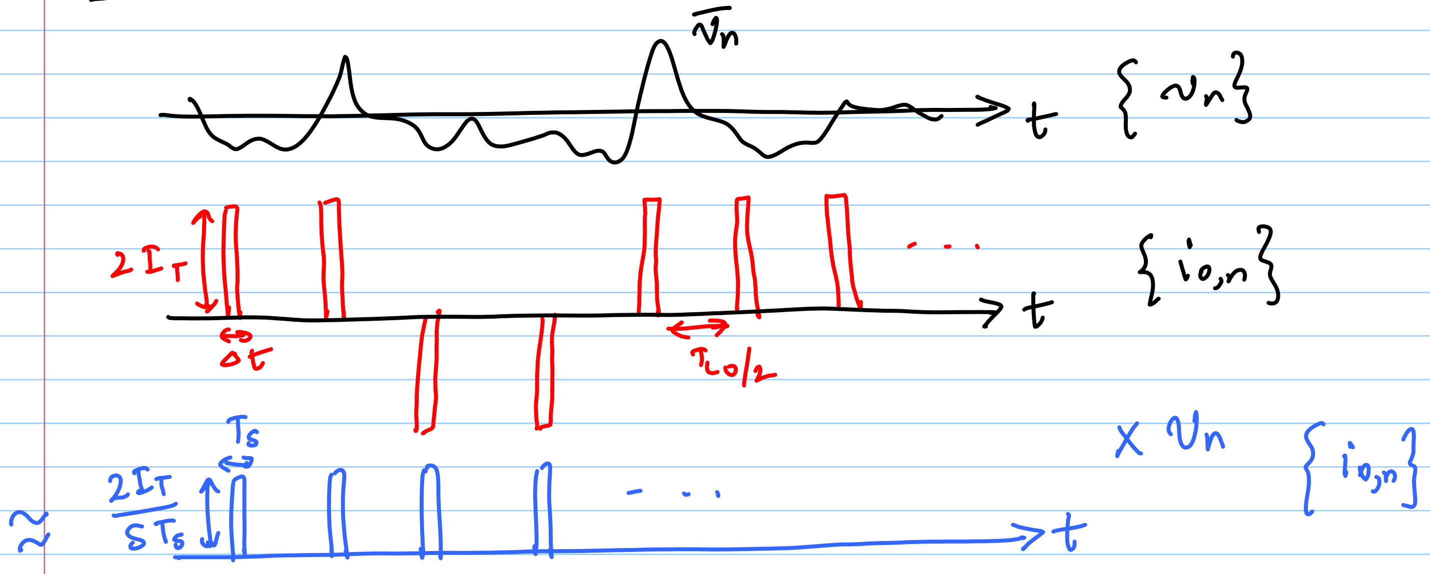
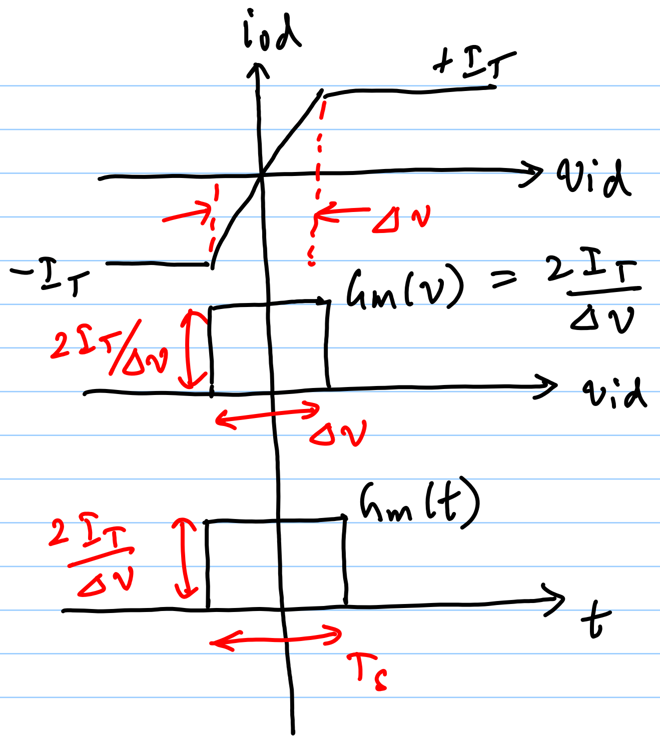
Lecture 23: Noise in Mixers (contd.); other linearization techniques

Switch Thermal noise



T_s = time when both switches are on



piecewise linear approx.

← applies to any transconductor

$\Delta V \ll V_{LO}$

$v_{id} = 2V_{LO} \sin \omega_{LO} t$

$\Rightarrow G_m = G_m(t)$ also

$$T_s = \frac{\Delta V}{S} = \frac{\Delta V}{2V_{LO}\omega_{LO}}$$

$$G_m = \frac{2I_T}{\Delta V} = \frac{2I_T}{S T_s}$$

$$\widehat{V_n^2} = \frac{4kT\gamma}{G_m}$$

It can be shown that:

$$\overline{i_{on}^2} = \frac{2}{T_{LO}} \cdot \left(\frac{2I_T}{S}\right)^2 \cdot \frac{1}{T_S} \cdot \widehat{V_n^2}$$

$$= \frac{4I_T}{S \cdot T_{LO}} \cdot \frac{2I_{\cancel{T}}}{S\cancel{T}_S} \cdot \frac{4kT\gamma}{\cancel{G}_m}$$

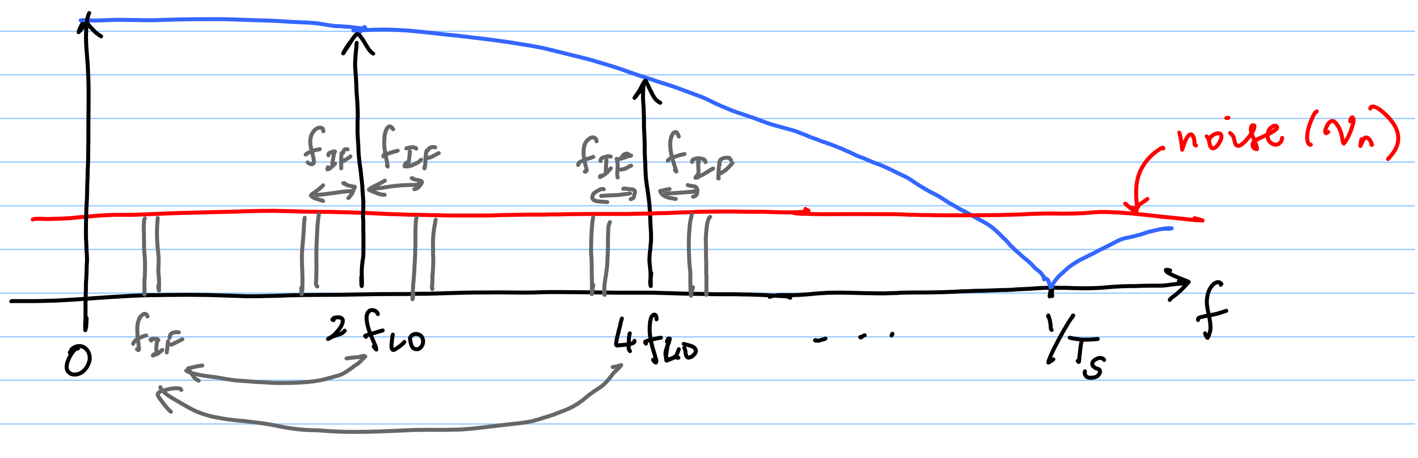
$$= 4kT\gamma \cdot \frac{4I_T}{ST_{LO}} \quad \left\{ \text{We want } S \text{ to be large} \right\}$$

$$= 4kT\gamma \cdot \frac{I_T}{\pi V_{LO}} \quad \left\{ \text{for a sinusoidal LO} \right\}$$

* does not depend on transistor size!

switch size ↑ ⇒ T_S ↓ ⇒ wider sampling BW

but as switch size ↑ ⇒ input referred noise ↓



$$\overline{v_{o,n,sw}^2} = 8kT\gamma \cdot \frac{I_T}{\pi V_{LO}} \cdot R_L^2$$

If other white noise sources are present at the LO port (e.g. LO buffer noise) ⇒ adjust γ

Total noise

$$\overline{v_{on}^2} = \overline{v_{on,R_L}^2} + \overline{v_{on,g_m}^2} + \overline{v_{on,sw}^2}$$

$$= 8kTR_L + 4kT\gamma g_m R_L^2 + 8kT\gamma R_L^2 \cdot \frac{I_T}{\pi V_{LO}}$$

$$= 8kTR_L \left\{ 1 + \frac{\gamma g_m R_L}{2} + \gamma \frac{R_L I_T}{\pi V_{LO}} \right\} \quad //$$

Noise optimisation

Rewrite

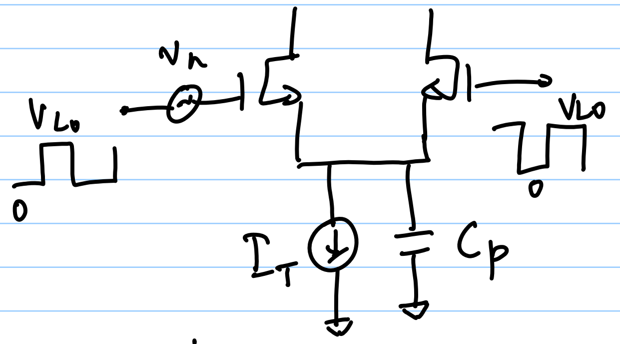
$$\overline{v_{on}^2} = 8kTR_L \left\{ 1 + \gamma \frac{R_L I_T}{\pi V_{LO}} + \gamma \frac{R_L \cdot I_T}{2(V_{GS} - V_T)} \right\}$$

* relative contribution of switch and transconductance stages is:

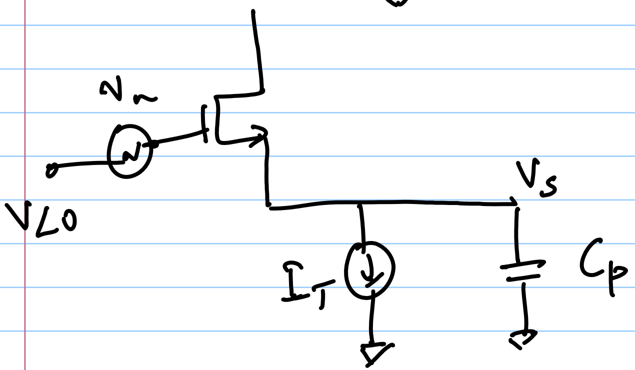
$$\frac{2(V_{GS} - V_T)}{\pi V_{LO}}$$

⇒ as $(V_{GS} - V_T) \sim V_{LO}$, they contribute comparable noise ← noise-linearity tradeoff

b) Indirect switch noise

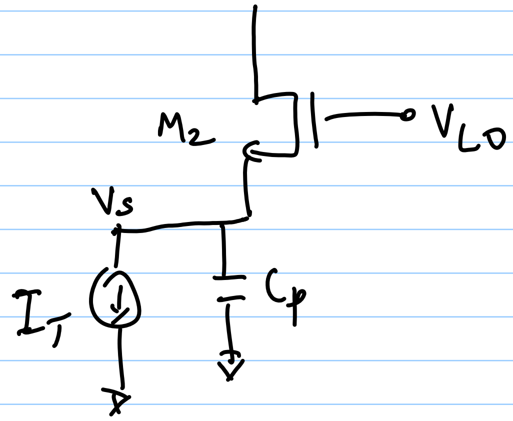


$\equiv$



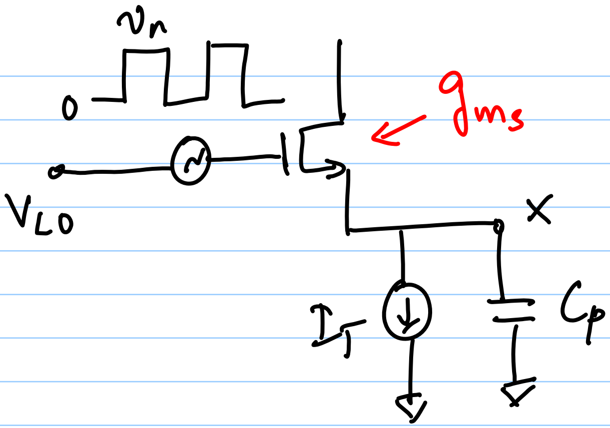
1st half cycle

+



2nd half cycle

$\equiv$

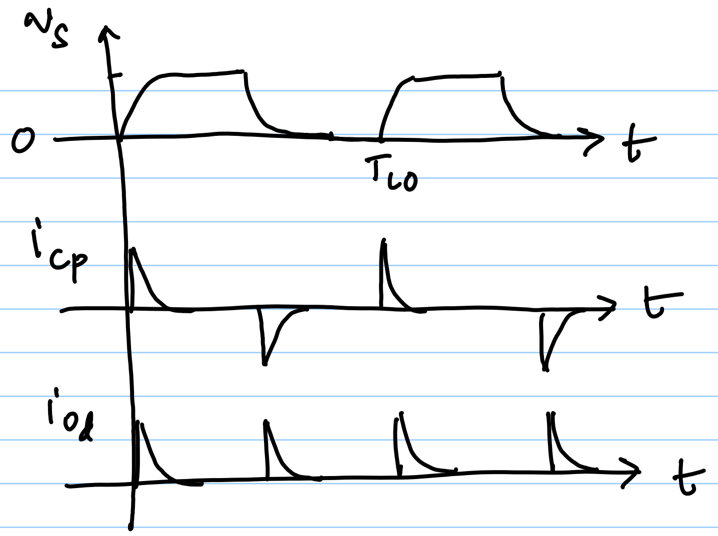


$\leftarrow$ single source follower with switching v_n

$v_n << V_{LO} \Rightarrow$ <u>linear</u> assumption is valid

time constant @ $x = \dfrac{C_p}{g_{ms}} << T_{LO}$

$\Rightarrow$ V_s charges & discharges exponentially every period



$\leftarrow$ freq. $= f_{LO}$, $i_{cp}(DC) = 0$

$\leftarrow$ freq. $= 2 f_{LO}$

i_{od} commutates between $\pm i_{cp}$

$\Rightarrow$ non-zero DC value

$\Rightarrow$ Flicker noise is present @ output!

$$\bar{i}_{on} = \frac{2}{T_{LO}} \int_0^{T_{LO}/2} i_{cp}(t)\, dt = \frac{2}{T_{LO}} \int_0^{T_{LO}/2} C_p \left[\frac{dv_s(t)}{dt} \right] dt$$

$$= \frac{2}{T_{LO}} C_p \left[V_s(T_{LO}/2) - V_s(0) \right]$$

$$= \frac{2}{T_{LO}} C_p V_n$$

$$G_c(\text{flicker noise, indirect}) = \frac{2 C_p}{T_{LO}} = 2 f_{LO} C_p$$

$\rightarrow$ increases with f_{LO}

$\rightarrow$ usually smaller than direct mechanism

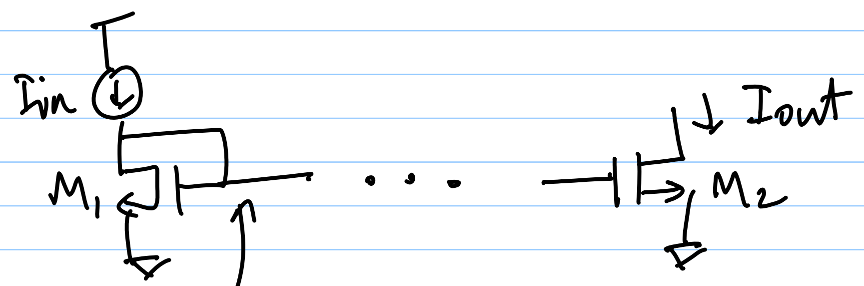
$$\rightarrow \text{SNR} = \frac{\frac{2}{\pi} \cdot g_m}{2 f_{LO} C_p} \cdot \frac{V_{in}}{V_n} \leftarrow \text{minimise } C_p$$

If $C_p \sim \underset{(g_m)}{C_{gs}}$, $\text{SNR} \approx 2 \frac{f_T}{f_{LO}} \cdot \frac{V_{in}}{V_n} \leftarrow$ max. f_T

Additional linearisation techniques

1) Predistortion

simplest example = current mirror

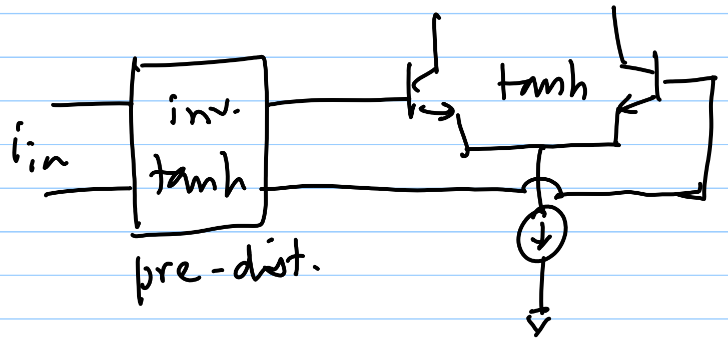


$$V_{GS} = V_{T_1} + \sqrt{\frac{2 I_{in}}{K_1'\left(\frac{W_1}{L_1}\right)}} \leftarrow \text{square root function}$$

$$I_{out} = \frac{K_2'}{2}\left(\frac{W_2}{L_2}\right)\left(V_{GS_2} - V_{T_2}\right)^2 \leftarrow \text{square function}$$

$$I_{out} = \frac{k_2'}{2}\left(\frac{W_2}{L_2}\right)\left\{\sqrt{\frac{2 I_{in}}{K_1'\left(\frac{W_1}{L_1}\right)}} + \left(V_{T_1} - V_{T_2}\right)\right\}^2$$

* $I_{out} \leftrightarrow I_{in}$ depends on matching



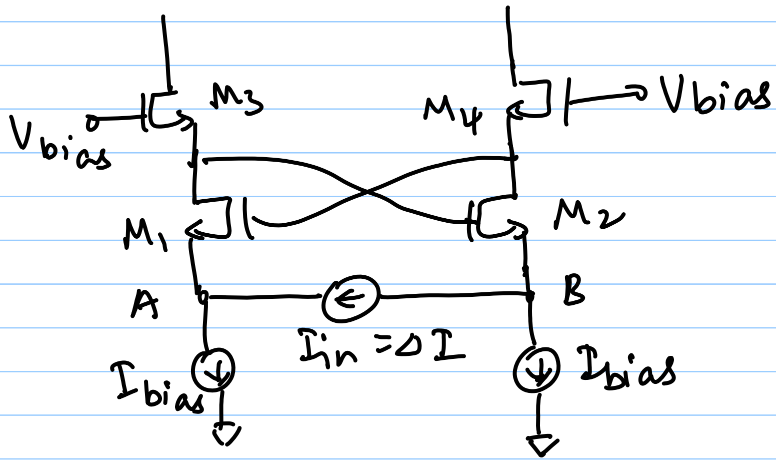
overall ckt. is linear

2) Piecewise approximation

e.g. multi-tanh (already covered in class)

3) Feedback

MOSFET cross-quad (Tektronix)



Goal: synthesise short-ckt. between A & B (+ve feedback)

$$I_2 = I_4 = I_{bias} + \Delta I$$

$$I_1 = I_3 = I_{bias} - \Delta I$$

$$\Rightarrow \quad V_{GS_2} = V_{GS_4} = V_{GS} + \Delta V_{GS}$$

$$V_{GS_1} = V_{GS_3} = V_{GS} - \Delta V_{GS}$$

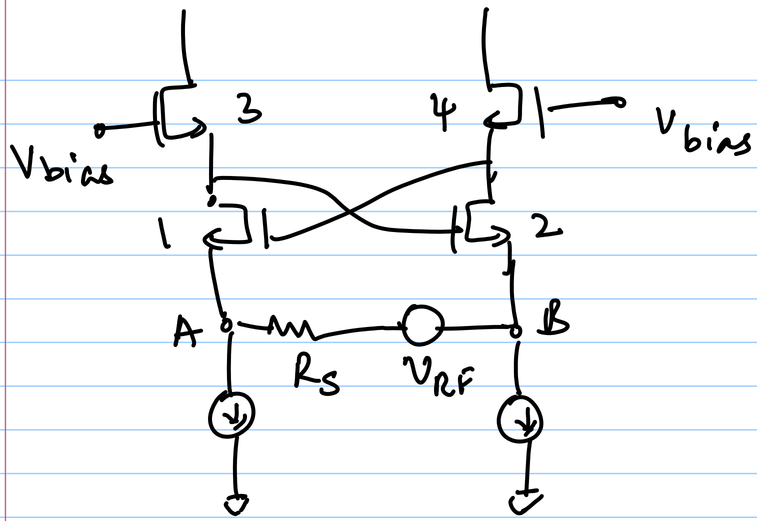
* assume same W/L ratios
* assume ΔV_{GS} is linear with ΔI

$$V_{AB} = (V_{bias} - V_{GS_4} - V_{GS_1}) - (V_{bias} - V_{GS_3} - V_{GS_2})$$

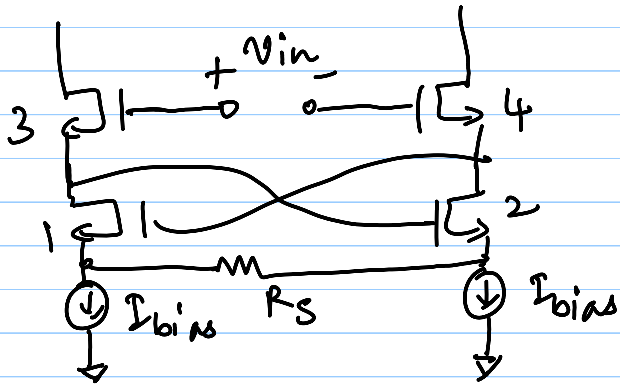
$$= (V_{GS_2} - V_{GS_4}) + (V_{GS_3} - V_{GS_1})$$

$$= \underline{\underline{0}}$$

$$R_{AB} = \frac{V_{AB}}{\Delta I} = 0 \quad \leftarrow \text{ideal short ckt.}$$



$\Delta I = \dfrac{V_{rf}}{R_S}$ (very linear)



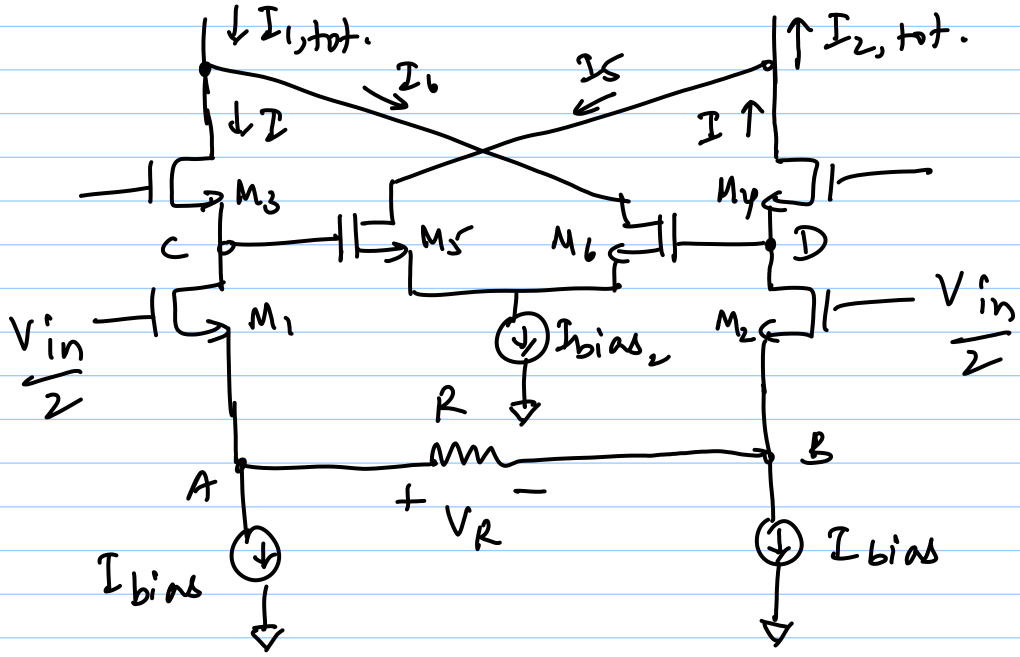
<u>alternative version</u>

* inputs applied to M_3-M_4 gates

$G_{m_{eff.}} = 1/R_s$

4) <u>Feedforward</u> — no BW, stability limitations

<u>Cascomp topology</u> (Tektronix)



M_5-M_6 = error amplifier

$$V_R = V_{AB} = \left(\frac{V_{in}}{2} - V_{GS_1}\right) - \left(-\frac{V_{in}}{2} - V_{GS_2}\right)$$

$$= V_{in} - (V_{GS_1} - V_{GS_2})$$

$$\Delta V_{GS_{1,2}} = V_{GS_1} - V_{GS_2}$$

$$= \sqrt{\frac{2(I_{Bias} + \Delta I)}{k'(W/L)}} - \sqrt{\frac{2(I_{Bias} - \Delta I)}{k'(W/L)}}$$

$$= \sqrt{\frac{2 I_{bias}}{k'(W/L)}} \left\{ \sqrt{1 + \frac{\Delta I}{I_{bias}}} - \sqrt{1 - \frac{\Delta I}{I_{bias}}} \right\}$$

$$\approx (V_{GS} - V_T) \left\{ \left(1 + \frac{\Delta I}{2 I_{bias}}\right) - \left(1 - \frac{\Delta I}{2 I_{bias}}\right) \right\}$$

$$\approx (V_{GS} - V_T)_{1,2} \cdot \frac{\Delta I}{I_{bias}}$$

$$I = \frac{V_R}{R} = \frac{V_{in}}{R} - \underbrace{\frac{\Delta V_{GS_{1,2}}}{R}}_{\text{error term}}$$

* Voltage gain from

$+\frac{V_{in}}{2}$ to C $= -1 \Rightarrow V_C = -\frac{V_{in}}{2}$

$-\frac{V_{in}}{2}$ to D $= -1 \Rightarrow V_D = \frac{V_{in}}{2}$

$$I_6 = g_{m_6} \frac{V_{in}}{2} = g_{m_5} \frac{V_{in}}{2}$$

$$I_5 = -g_{m_5} \frac{V_{in}}{2}$$

$$I_{1,tot.} = I + I_6$$

$$= \frac{V_{in}}{R} - \frac{\Delta V_{GS_{1,2}}}{R} + g_{m5}\frac{V_{in}}{2}$$

$$I_{2,tot.} = I - I_5$$

$$= \frac{V_{in}}{R} + \underbrace{\frac{\Delta V_{GS_{1,2}}}{R} - g_{m5}\frac{V_{in}}{2}}_{\text{set this term} = 0 \text{ by design}}$$