Lecture 18: LNA Design (contd.)

Note Title 7/26/2011

Last class:

1) Input match
2) Output match

} may require iteration

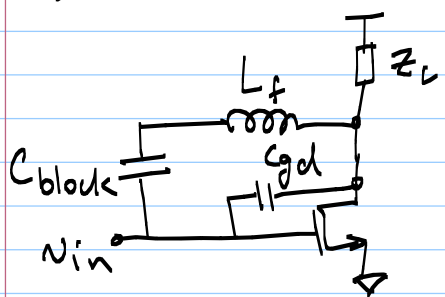
* g_m & C_{gd} will cause input & output matches to depend on each other — Iteration
* Input matching is quantified by S_{11} (also called 'return loss')

$$S_{11} = 20\log\left|\frac{Z_{in}-R_s}{Z_{in}+R_s}\right|$$

* Similarly, output matching is quantified by S_{22}

3) Stability: Circuit Techniques to improve stability (i.e. decrease C_{gd} and increase S_{12})

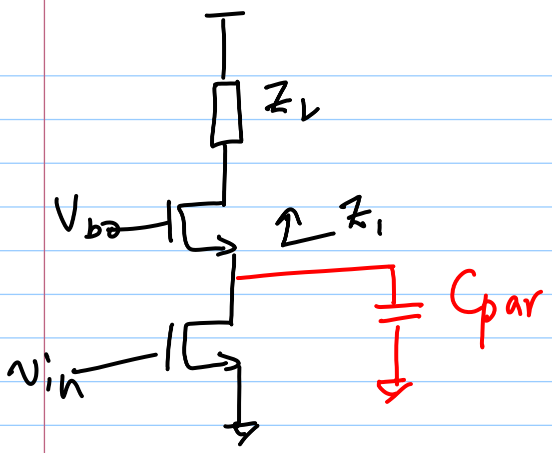
A) Neutralisation:



* L_f and C_{gd} resonate @ desired frequency
* L_f & C_{block} parasitics load input node
* area intensive (L_f)

B) Cascode: * reduces effect of C_{gd}

* reduces interaction between input & output tuned ckts.



$$Z_1 = \frac{1}{g_m + g_{mb}} + \frac{Z_L}{(g_m + g_{mb})\, r_o}$$

assume r_o is large, $g_m >> g_{mb}$

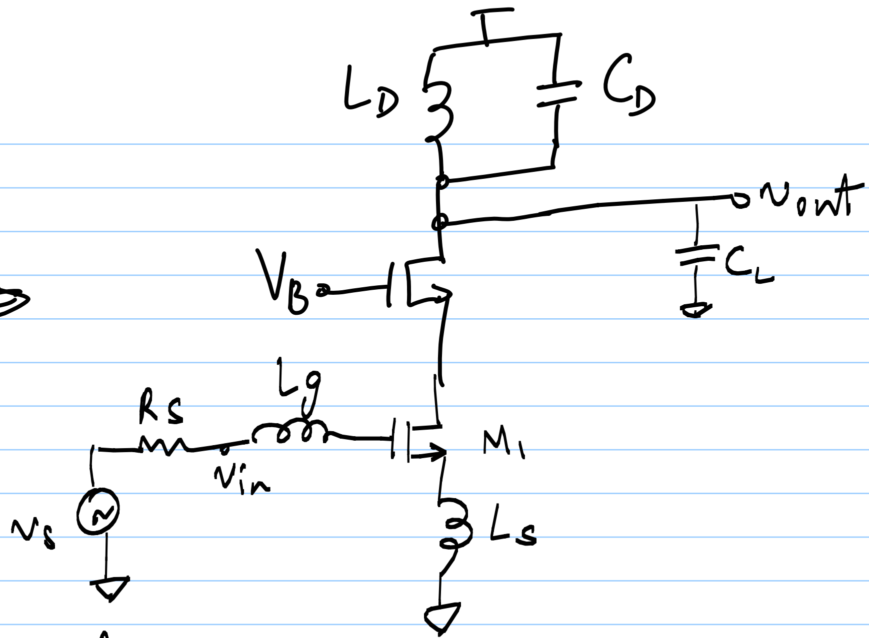
$$\Rightarrow Z_1 \approx \frac{1}{g_m}$$

* parasitic cap can cause some loss of signal and degrade NF at high freq.

* short-channel MOS – r_{out} is finite, so may want to use $L > L_{min}$.

→ This will increase C_{par}

Cascode LNA ⇒



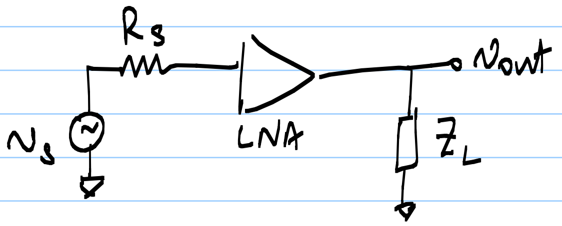
4) Voltage gain A_V

$$A_V = \frac{v_{out}}{v_{in}} = G_m R_p$$

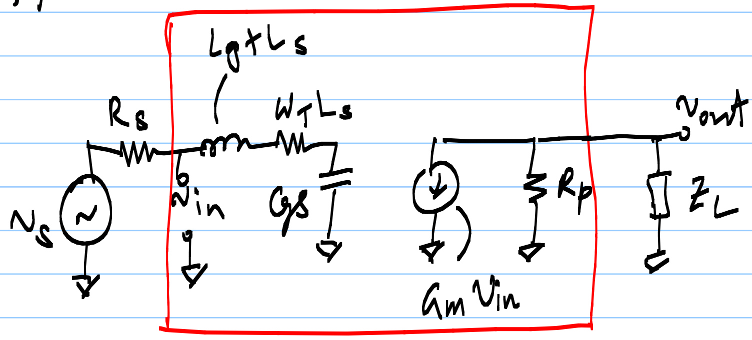
$$\Rightarrow \boxed{A_V = 2 Q_{in} g_{m1} R_p}$$

* neglect r_{ds} (we will typically use a cascode)

5) Transducer Power gain G_T



$\Rightarrow$



$$G_T = \frac{\text{Power delivered to load}}{\text{Power available from source (max)}} = \frac{P_{load}}{P_{avl,s}}$$

$$P_{avl,s} = \frac{|v_{in}|^2}{2R_S} \quad \left\{ \begin{array}{l} \text{assume } v_{in}, v_{out} \text{ etc. are} \\ \text{peak values} \end{array} \right\}$$

Let $Y_L = \frac{1}{Z_L} \Rightarrow G_L = \mathrm{Re}(Y_L) = \mathrm{Re}\left(\frac{1}{Z_L}\right)$

$$P_{load} = \frac{|v_{out}|^2}{2} \cdot G_L = \frac{|v_{out}|^2}{2} \cdot \mathrm{Re}\left(\frac{1}{Z_L}\right)$$

$$= \frac{1}{2}\mathrm{Re}\left(\frac{1}{Z_L}\right) \cdot \left|G_m (R_p \| Z_L)\right|^2 \cdot |v_{in}|^2$$

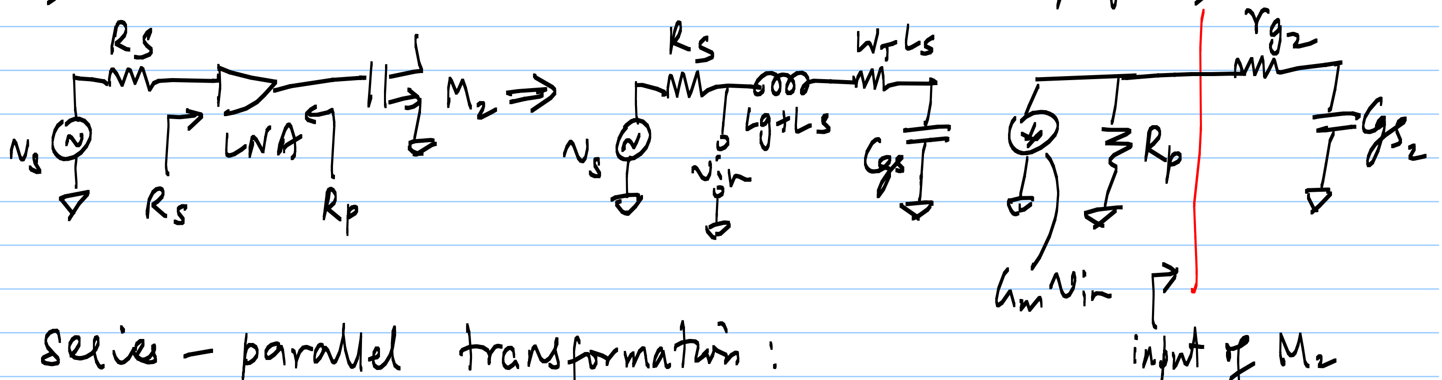
$$\Rightarrow \boxed{G_T = \left|G_m (R_p \| Z_L)\right|^2 \cdot R_S \cdot \mathrm{Re}\left(\frac{1}{Z_L}\right)}$$

a) LNA drives off-chip component (e.g. filter)

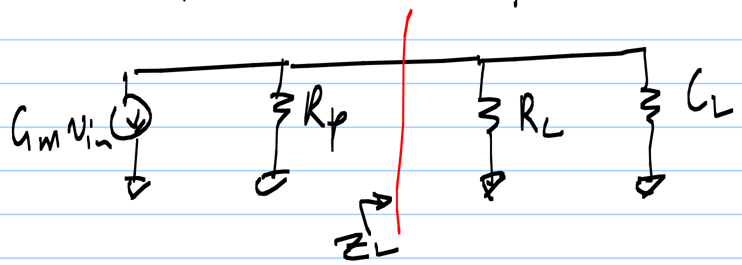
$\rightarrow$ Z_L is matched to R_p in that case

$$G_T = \left|G_m \frac{R_p}{2}\right|^2 \cdot R_S \cdot \frac{1}{R_p} = \frac{G_m^2 R_S R_p}{4}$$

b) LNA drives mixer (or another amplifier)



series - parallel transformation:



$R_L \approx Q_2^2 \, r_{g_2}$

$C_L \approx C_{g_2}$

$Q_2 = \dfrac{1}{w_0 \, r_{g_2} \, C_{gs_2}}$

* MOSFET with good layout $\Rightarrow r_{g_2}$ is very small
* Ideally $r_{g_2} \to 0 \Rightarrow Q_2 \to \infty \Rightarrow R_L \to \infty$

* C_L is usually absorbed into C_p (output tuning network of LNA)

$\Rightarrow \quad Z_L \approx R_L = Q_2^2 \, r_{g_2}$

$$G_T = |G_m (R_p \| R_L)|^2 \cdot \frac{R_S}{R_L}$$

$G_T \to 0$ as $R_L \to \infty$

what does this mean?

→ ideal MOSFET M_2 has purely capacitive gate

→ no <u>real</u> power consumed @ input

$\Rightarrow P_{load} \to 0 \Rightarrow A_T \to 0$

6) Available power gain A_p

$$A_p = \frac{\text{Power available from LNA output}}{\text{Power available from source}} = \frac{P_{av,LNA}}{P_{av,s}}$$

$P_{av,LNA} \equiv$ power delivered to load under matched condition (same as 4(a))

$$\boxed{A_p = \frac{G_m^2 R_s R_p}{4}}$$

How about Power Dissipation?

Power-constrained noise optimization:

* Minimize F given a specific bound on P_{diss}.

* For full details, see Thomas Lee pp 380-384

From 2-port noise theory,

$$F = F_{min.} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2\right]$$

* define

$$\frac{G_{opt}}{\omega C_{gs}} = \alpha\sqrt{\frac{\delta}{5\gamma}(1-|c|^2)} = Q_{opt}.$$

$$Q_s \equiv \frac{1}{\omega C_{gs} R_s}$$

* Rewrite $F = F_{min.} + \left[\frac{\gamma}{\alpha g_m R_s}\right]\left[1 - \frac{Q_{opt}^2}{Q_s^2}\right]$

* optimum Q_{sp} turns out to be $\approx \underline{\underline{4.5}}$

* $W_{opt,p} = \frac{3}{2} \frac{1}{\omega L C_{ox} R_s Q_{sp}} \approx \frac{1}{3 \omega L C_{ox} R_s}$

* $F_{min,p} \approx 1 + 2.4 \frac{\gamma}{\alpha} \left[\frac{\omega}{\omega_T} \right]$

* $F_{min.} \approx 1 + 2.3 \left[\frac{\omega}{\omega_T} \right]$

$\gamma = 2,\ \delta = 4,\ \alpha = 0.85$

ω_T / ω	F_{min}	$F_{min,p}$
20	0.5	1.1
15	0.6	1.4
10	0.9	1.9
5	1.6	3.3

basic design procedure:

1) Determine $W_{opt,p}$ as above
2) Choose I_{bias} based on power constraint
3) Determine L_s (with R_{in}, ω_T known)
4) Calculate $NF_{min,p}$
5) Choose L_g for desired f_o
6) Choose L_D to maximize R_p (highly dep. on process) and ∴ gain

Note: you will probably need to iterate at each step and also between steps

* Noise vs. linearity tradeoff

as $I_{bias} \uparrow \Rightarrow (V_{GS} - V_T) \uparrow \Rightarrow IIP_3 \uparrow$

but $\longrightarrow$ increased short-channel effects

$\Rightarrow \alpha \left(\text{i.e. } \frac{g_m}{g_{d0}} \right) \downarrow \Rightarrow F \uparrow$