ADAPTIVE EQUALIZATION AT MULTI-GHZ DATARATES

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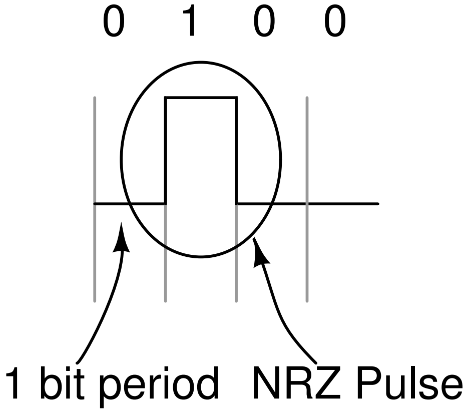
Outline

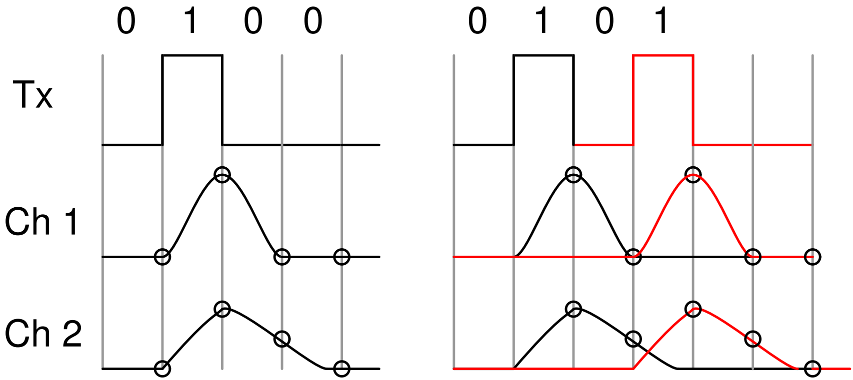
- Introduction.
- Approaches to electronic mitigation
  - ADC & Digital FIR Filter.
  - Analog Traveling Wave and Transversal Equalizers.
- Problems and prospects of analog adaptive filters.
- Conclusions

Non-Return-to-Zero (NRZ) Data Transmission

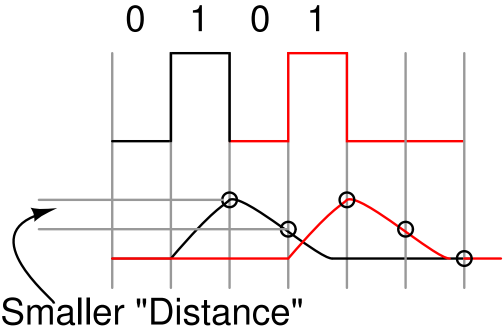


At 10 Gbps, 1 Bit period is 100 picoseconds

What is Inter-Symbol-Interference ?

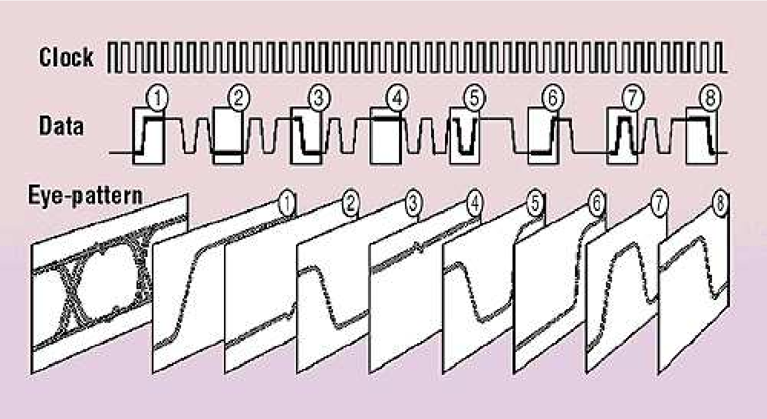


Why is ISI Bad ?



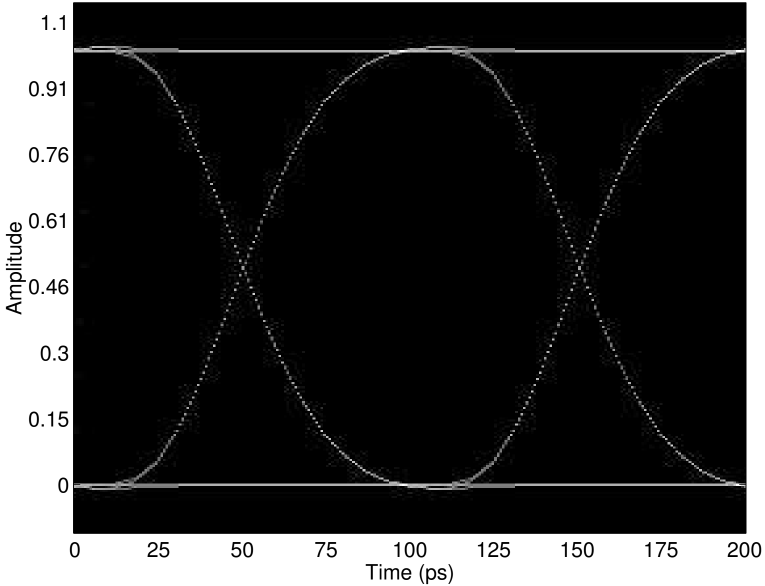
- Smaller separation, more likely to make an error

What is an Eye Diagram ?

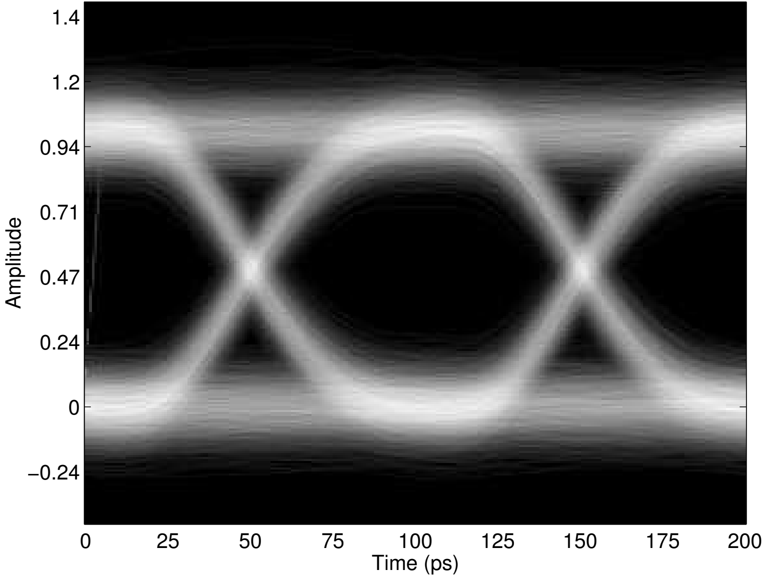


Graphics Source : Electronic Design Magazine

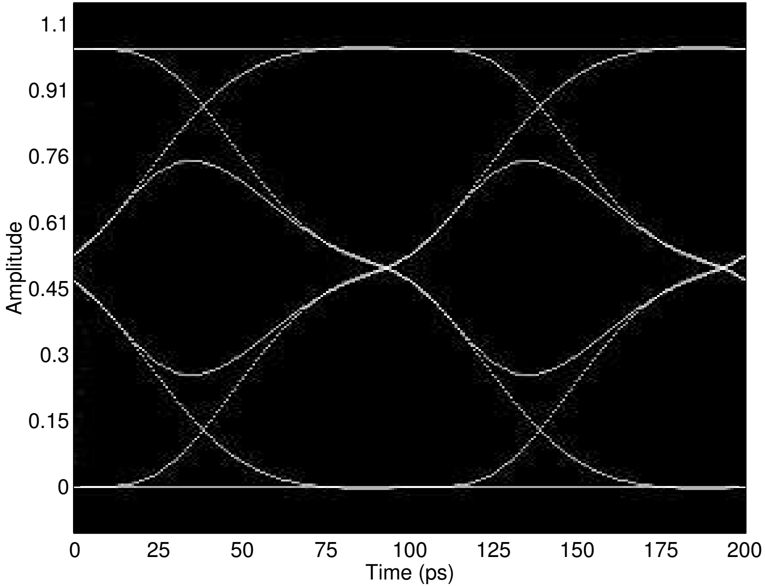
Eye Diagram : No ISI, no noise



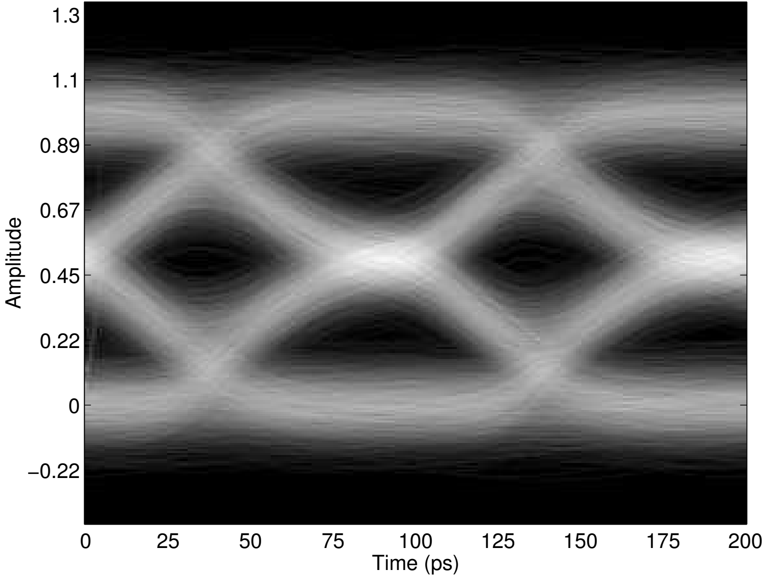
Eye Diagram : No ISI, with noise



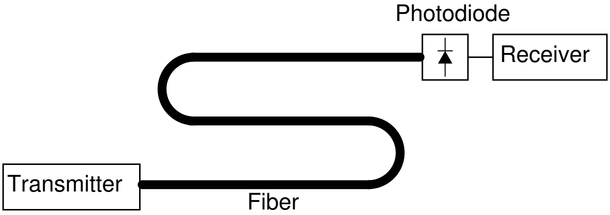
Eye Diagram : With ISI, no noise



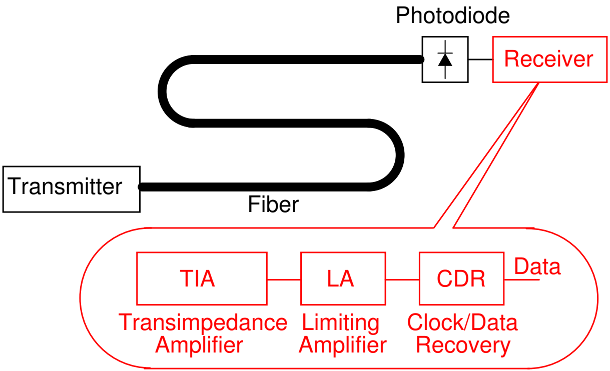
Eye Diagram : With ISI, with noise



Typical Optical Fiber Data Link



Typical Optical Fiber Data Link



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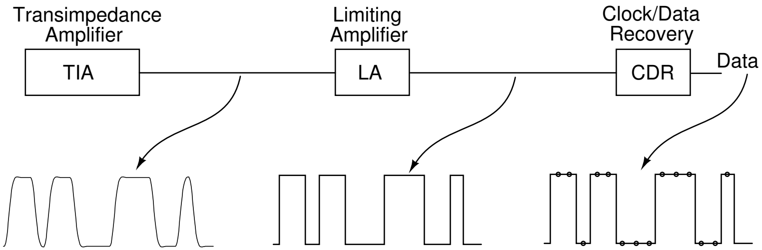
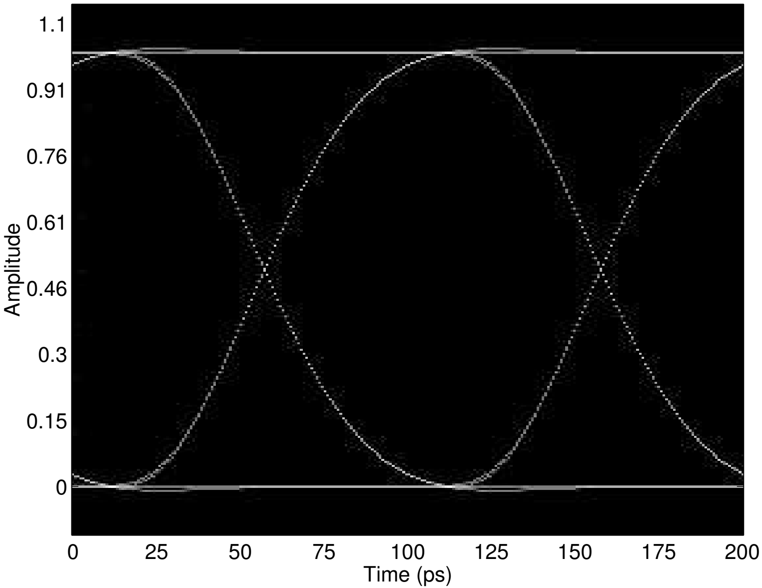


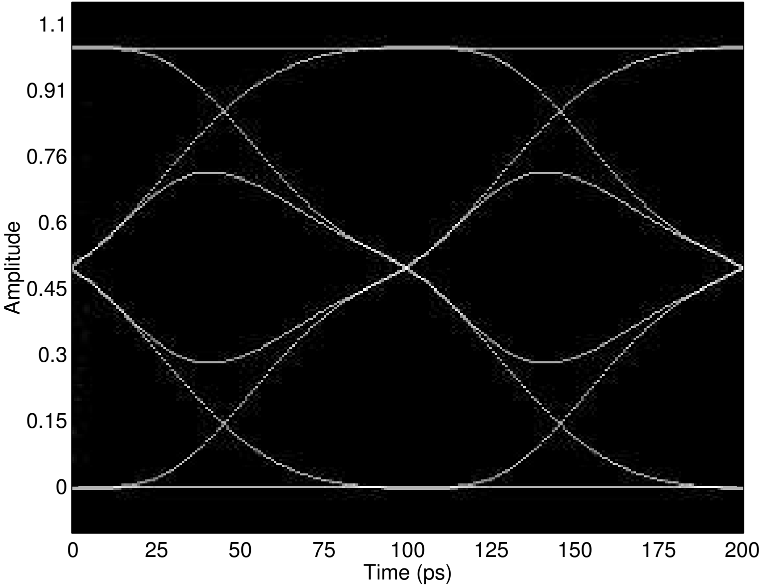
ISI in Optical Links

- Dispersion in fiber due to manufacturing tolerances
- Polarization Mode Dispersion in Single Mode Fiber
- Impulse Response : $\alpha\delta(t) + (1 - \alpha)\delta(t - T_d)$
- α is called the Power Split
- T_d is called the Differential Group Delay (DGD)
- Two paths with different delays and gains
- Much worse (many more paths, greater spread) in multi-mode fibers

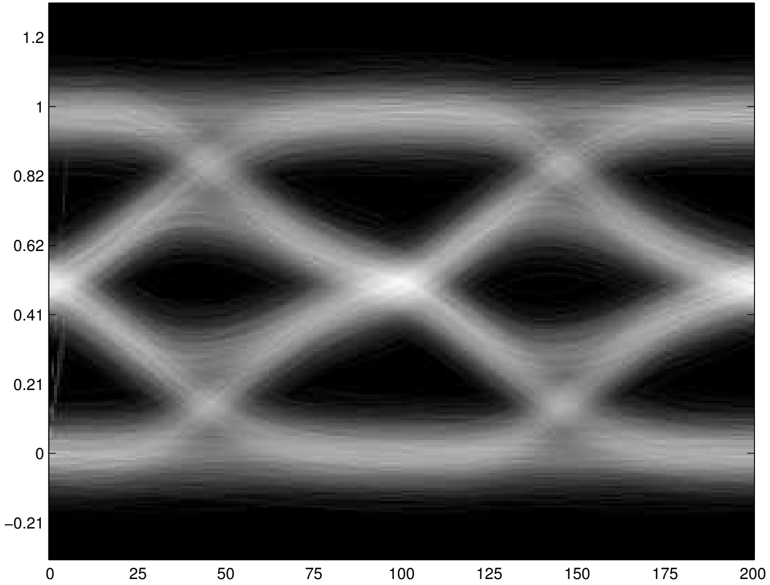
Example Eye : No ISI, Finite Tx Bandwidth



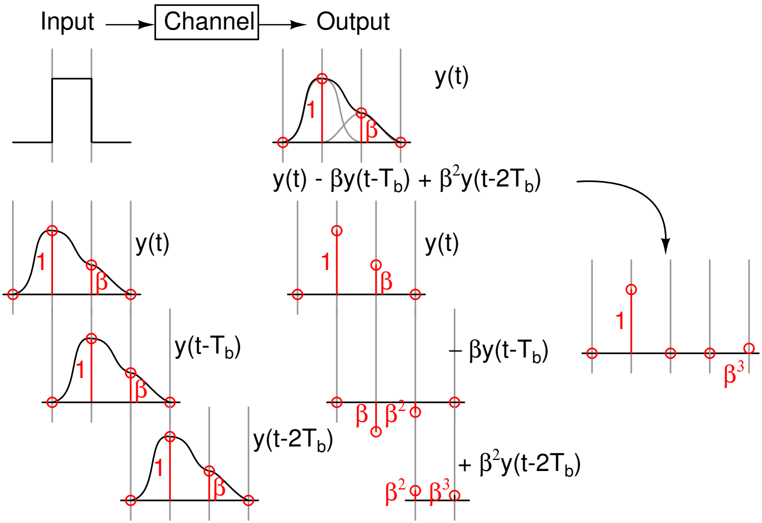
PMD, Finite Tx BW, DGD = 75 ps



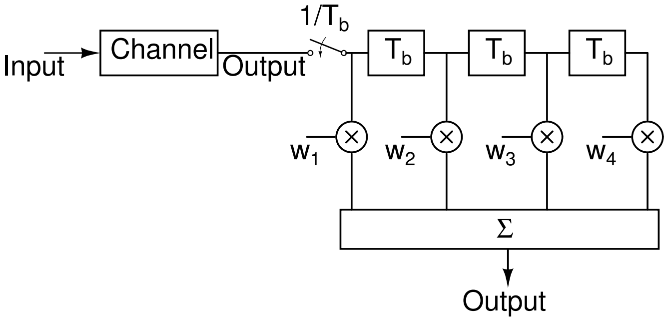
PMD, Finite Tx BW, DGD = 75 ps & Noise



Mitigating ISI



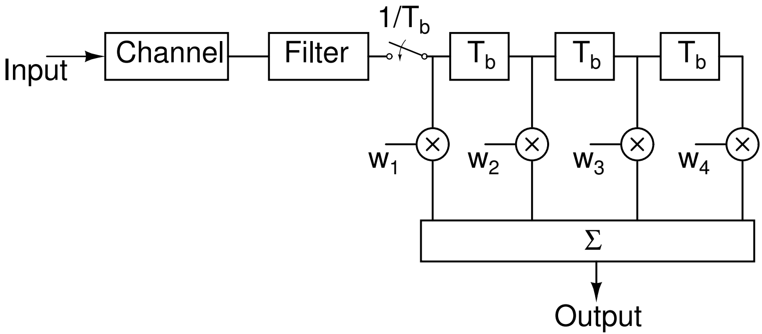
Mitigating ISI : Equalization



$$Output(nT_b) = \sum_{k=0}^{k=N-1} w_k y(nT_b - kT_b) \qquad (1)$$

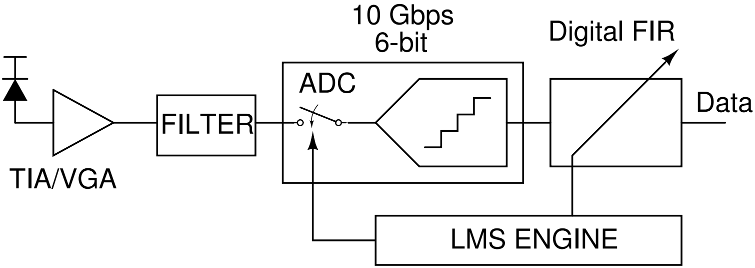
- Tapped-delay line Equalizer
- Weights need to be adaptive, since channel is varying (slowly) with time

Mitigating ISI : Equalization



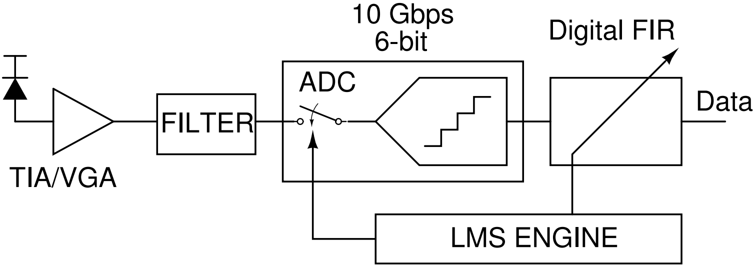
- 4 “tap" adaptive equalizer
- Need a filter before sampling
- Called the “matched filter"

Digital Receiver : Baud Spaced Equalizer (BSE)



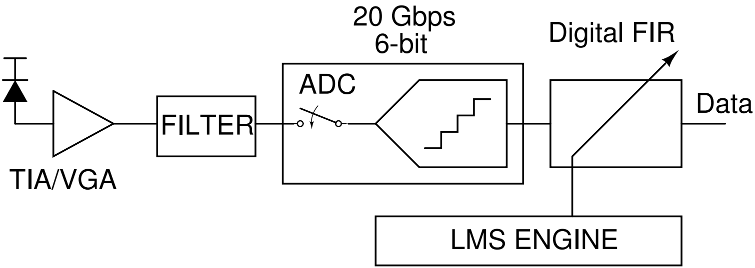
- Timing Phase sensitivity in a BSE
- High speed (10 Gbps), 6-bit ADC
- Example : Bell Labs (2003) - 6-bit 10 G ADC
  - 3.5 W and yields 4 effective bits
  in 0.18μm SiGe BiCMOS Technology (state of the art)
- Parallelism in the equalizer - more area

Digital Receiver : Baud Spaced Equalizer (BSE)



- Too much power / area
- ADC is a big project in itself

Digital Receiver : Fractionally Spaced Equalizer (FSE)

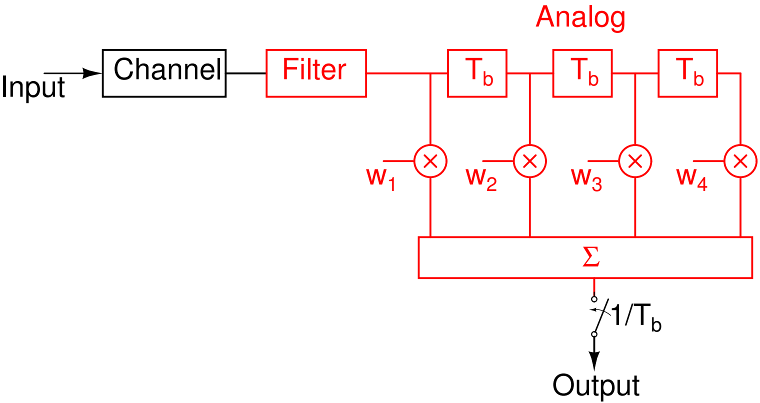


- Insensitive to timing phase
- High speed (20 Gbps), 6-bit ADC!
- Parallelism in the equalizer

Digital Implementation : Summary

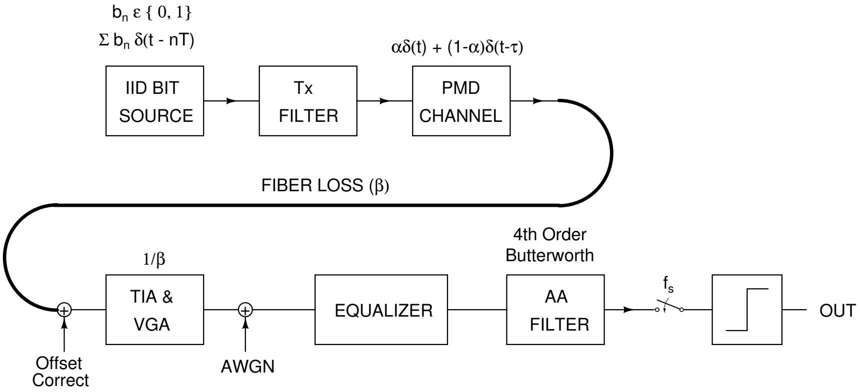
- Power hungry !
- ADC *may be* doable 10Gbps
- Solution doesnt scale well to higher speeds (40 Gbps)

Analog Implementation

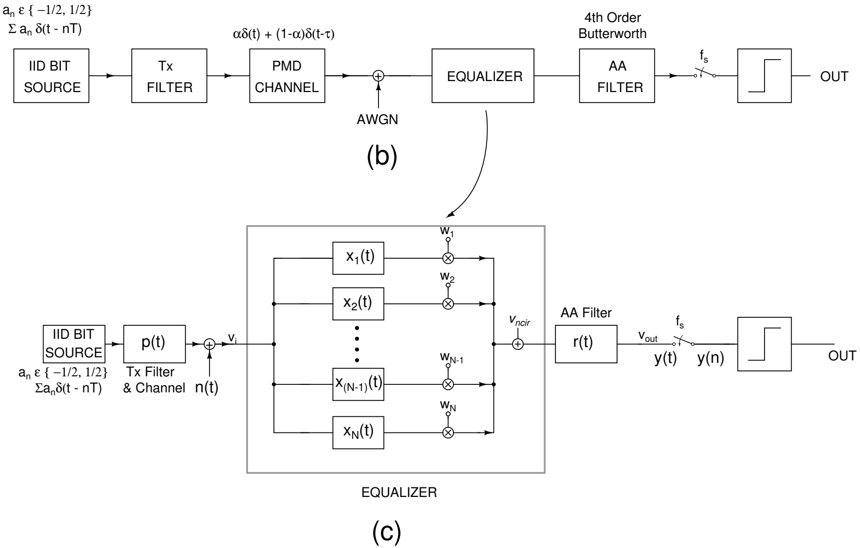


- Sampling after equalization
- Delays implemented using transmission lines
- FSE 10Gbps : Each delay line is 50 ps long

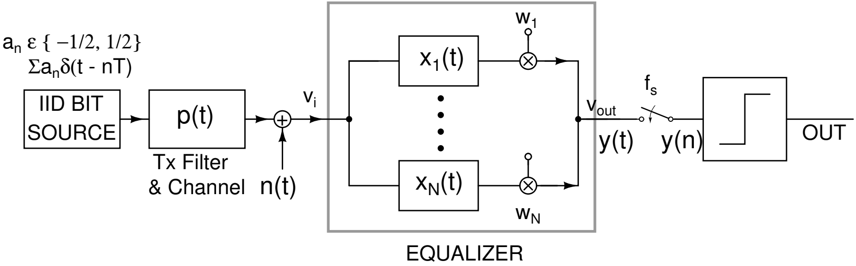
System Model



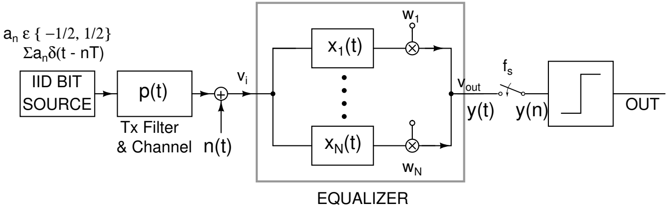
System Model



System Model



MMSE solution



$$c_i(t) = p(t) * x_i(t)$$

$$y(t) = \sum_{i=1}^{N} \sum_{k=-\infty}^{\infty} w_i\, a(k)\, c_i(t-kT) + \sum_{i=1}^{N} w_i\, n(t) * x_i(t)$$

$$y(n) = \sum_{i=1}^{N} \sum_{k=-\infty}^{n} w_i\, a(k)\, c_i(nT-kT) + \sum_{i=1}^{N} w_i\, (n(t) * x_i(t))|_{t=nT}$$

MMSE solution

$$y(n) = \sum_{i=1}^{N} \sum_{k=-\infty}^{n} w_i \, a(k) \, c_i(nT - kT) + \sum_{i=1}^{N} w_i \, (n(t) * x_i(t))|_{t=nT}$$

$$y(n) = \mathbf{a}^T(n) \begin{bmatrix} c_1(0.T) & c_2(0.T) & \dots & c_N(0.T) \\ c_1(T) & c_2(T) & \dots & c_N(T) \\ \vdots & \vdots & \ddots & \vdots \\ c_1(L.T) & c_2(L.T) & \dots & c_N(L.T) \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \\ \vdots \\ w_N \end{bmatrix} + \eta^T(n) \begin{bmatrix} w_1 \\ w_2 \\ \vdots \\ w_N \end{bmatrix}$$

$$\begin{aligned} \mathbf{a}^T(n) &= [a(n) \; a(n-1) \; \cdots \; a(n-L)] \\ \eta^T(n) &= \left[(n(t) * x_1(t))_{|t=nT} \; (n(t) * x_2(t))_{|t=nT} \; \cdots \; (n(t) * x_N(t))_{|t=nT}\right] \end{aligned}$$

Equalizer output is

$$y(n) = \mathbf{a}^T(n)\mathbf{C}\mathbf{w} + \eta^T(n)\mathbf{w}$$

MMSE solution

Equalizer output & desired outputs are

$$\begin{aligned} y(n) &= \mathbf{a}^T(n)\mathbf{C}\mathbf{w} + \boldsymbol{\eta}^T(n)\mathbf{w} \\ y_d(n) &= a(n-\delta) = \mathbf{a}^T(n)\,\mathbf{h}_\delta \end{aligned}$$

The error at the output of the equalizer is

$$\begin{aligned} e(n) &= y(n) - \mathbf{a}^T(n)\mathbf{h}_\delta \\ &= \mathbf{a}^T(n)\left(\mathbf{C}\mathbf{w} - \mathbf{h}_\delta\right) + \boldsymbol{\eta}^T(n)\mathbf{w} \end{aligned}$$

$$E\left[|e(n)|^2\right] = (\mathbf{C}\mathbf{w} - \mathbf{h}_\delta)^T\, E\left[\mathbf{a}(n)^T\mathbf{a}(n)\right](\mathbf{C}\mathbf{W} - \mathbf{h}_\delta) + \mathbf{w}^T E\left[\boldsymbol{\eta}^T(n)\boldsymbol{\eta}(n)\right]\mathbf{w}$$

$$E\left[\mathbf{a}(n)^T\mathbf{a}(n)\right] = \sigma_a^2\,\mathbf{I}, \text{ where } \quad \sigma_a^2 = E[|a(n)|^2].$$

MMSE solution

$$E\left[\eta^T(n)\eta(n)\right] = \mathbf{M} = \frac{N_o}{2}\begin{bmatrix} \int_0^\infty x_1(t)x_1(t)dt & \dots & \int_0^\infty x_1(t)x_N(t)dt \\ \int_0^\infty x_2(t)x_1(t)dt & \dots & \int_0^\infty x_2(t)x_N(t)dt \\ \vdots & \ddots & \vdots \\ \int_0^\infty x_N(t)x_1(t)dt & \dots & \int_0^\infty x_N(t)x_N(t)dt \end{bmatrix}$$

so that

$$E\left[|e(n)|^2\right] = \sigma_a^2(\mathbf{Cw} - \mathbf{h}_\delta)^T(\mathbf{Cw} - \mathbf{h}_\delta) + \mathbf{w}^T\mathbf{Mw}$$

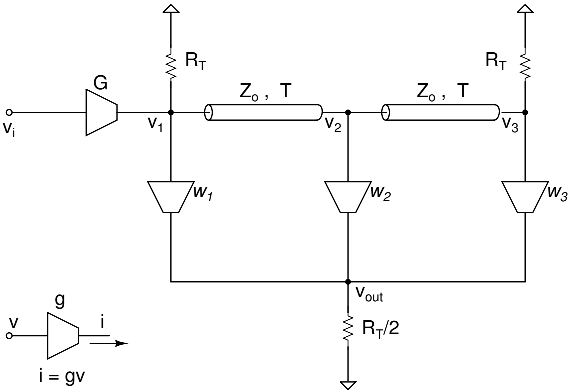
It can be shown that

$$\begin{aligned} \mathbf{w_{opt}} &= \mathbf{A}^{-1}\mathbf{C}^T\mathbf{h}_\delta \\ \mathbf{MMSE} &= \sigma_a^2\,\mathbf{h}_\delta^T(\mathbf{I} - \mathbf{CA}^{-1}\mathbf{C}^T)\mathbf{h}_\delta \end{aligned}$$

where

$$\mathbf{A} = \mathbf{C}^T\mathbf{C} + \mathbf{M}/\sigma_a^2$$

Tapped Delay Line Filters : Transversal

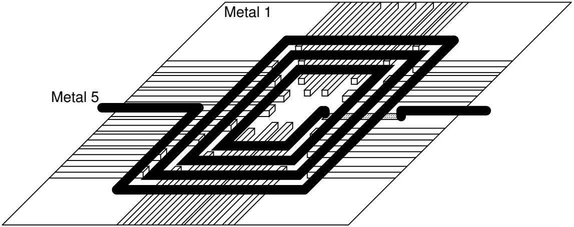


- Delay Elements are passive
- Tap weights : variable gain amplifiers (Differential pair)
- Summation : Kirchoffs Current Law

Choices for On-chip Delay Lines : Microstrip

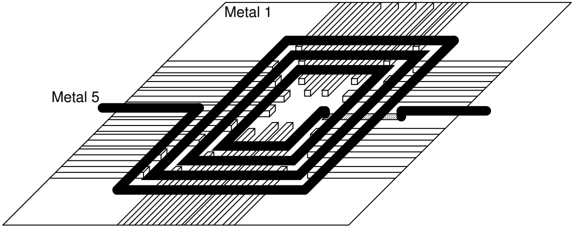
- Wideband
- Need 50 ps delay
- Velocity of light   150 μm/ps
- 50 ps $\Rightarrow$ 7.5 mm ! (and we need several of them)
- Conclusion : No good
- What can we do to make the delay line smaller ?

Spiral Delay Lines



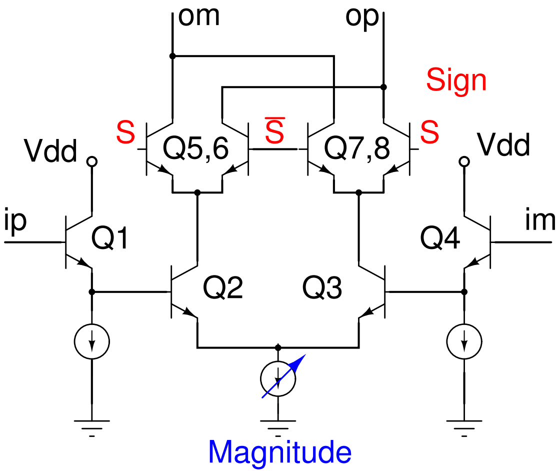
- Spiral : reduces size
- Use metal interconnect layers
- Mutual coupling results in increased inductance

Spiral Delay Lines



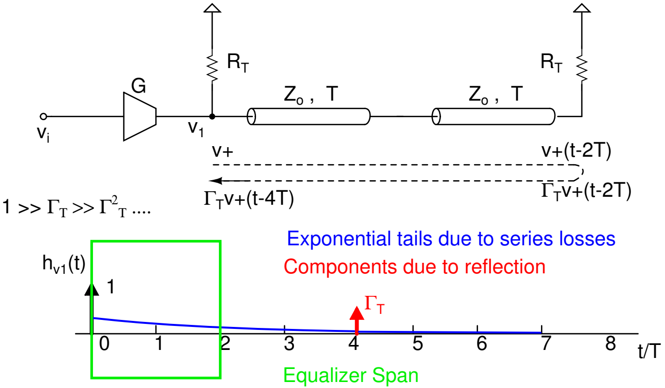
- Ground plane is broken to avoid image currents
- Attempt to distribute capacitance uniformly across the inductor
- Typical size - 300μm on a side
- Accurate model through EM Simulations

Tunable Weights



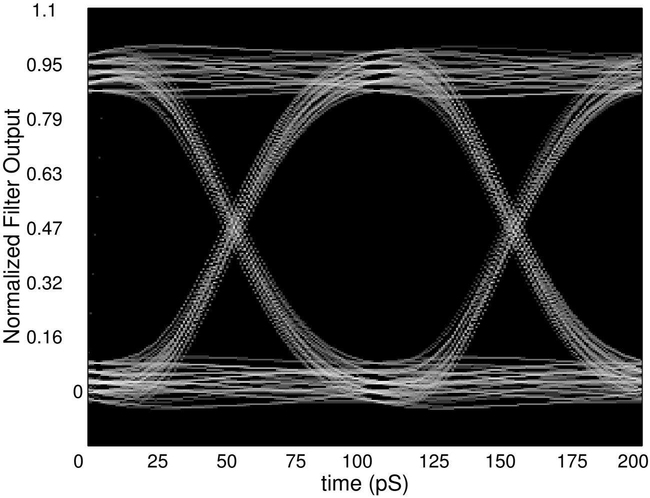
- Example of a tunable tap weight implementation

Problems with Transversal Filters



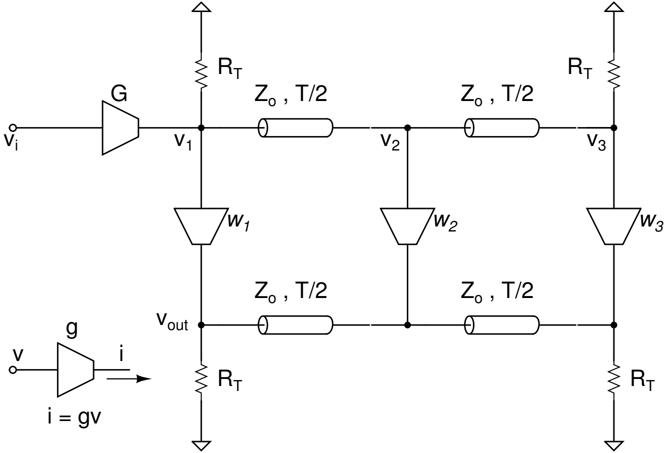
- Mistermination & Loss in the delay lines
- Tap responses have components outside equalizer span
- “ISI" within the equalizer ! Degrades performance

Problems with Transversal Filters



- Eye diagram at the first tap output

Traveling Wave Amplifier (TWA) FIR Filter



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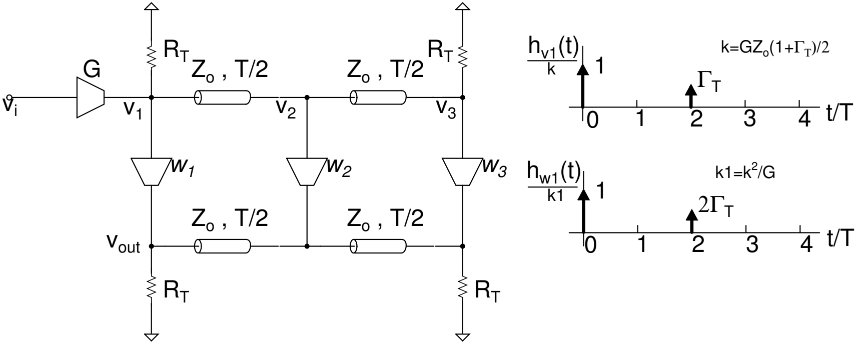
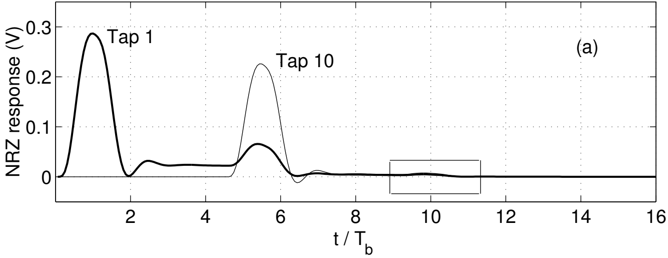
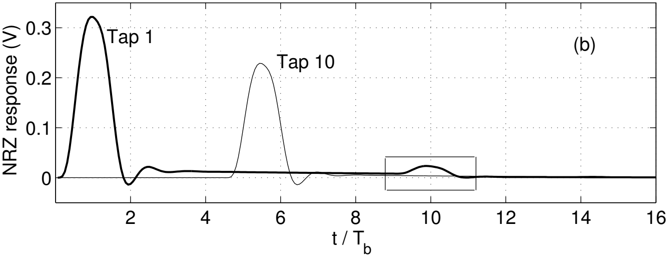


TWA FIR Filters : Comments

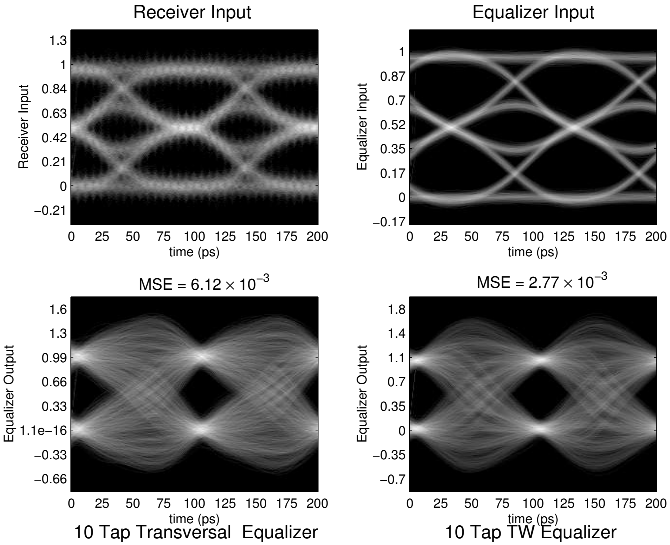
- Improvement over a transversal filter
- Robust with mistermination and series loss
- Used in several commerical equalizer ICs
- Two doubly terminated lines
  - Tap weights need to be larger by a factor of 2

Traveling Wave versus Transversal Equalizers





Traveling Wave versus Transversal Equalizers



Summary-1

- TWA FIR Filters represent the state-of-the-art in high speed equalization
- Signal attenuation due to double termination
- Need for an “anti-alias" filter
- Delay cells are large and occupy space
- Example : A fully differential 10 tap TWA equalizer has 36 inductors ! (each being about 300μm on a side
- Capacitive loading of lines reduces cut-off frequency of the delay lines
- TWA filters are not amenable to LMS adaptation

Summary-2

- DFE used alongwith an FFE in “tough channels” - e.g. multimode channels.
- Timing recovery is an important issue.
- In simple channels, common to use an upfront timing recovery module that works with the receiver input.
- In more complicated channels, the FFE output can be used to derive the timing error.
- Joint timing recovery/equalization without a training sequence is a challenge.

Conclusions

- High speed equalization at multi-GHz datarates involves signal processing, circuit design and electromagnetics.
- The challenge is to implement well known signal processing techniques at such high data rates.
- Many problems to be solved - e.g. efficient LMS implementation at several GHz speeds.
- Lots of work to do !

Selected References

- Wu et. al, *Integrated transversal equalizers in high-speed fiber-optic systems,* IEEE JSSC, December 2003.
- Sewter et. al, *A 3-tap FIR filter with cascaded distributed tap amplifiers for equalization up to 40 Gb/s*, IEEE JSSC, August 2006.
- Pavan et. al, *Nonidealities in Traveling Wave and Transversal FIR Filters Operating at Microwave Frequencies*, IEEE TCAS-1, January 2006.