

Resource Constraints

Note Title

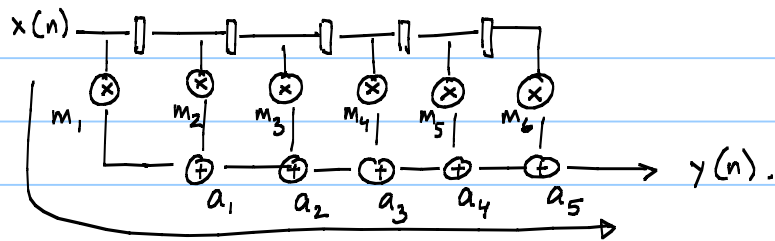
2/25/2010

References

- VLSI Digital Signal Processing
 - K. K. Parhi, Wiley, 1999
- Synthesis & Optimization of Digital Circuits
 - G. de Micheli, TMH, 1993.

6 - tap FIR filter.

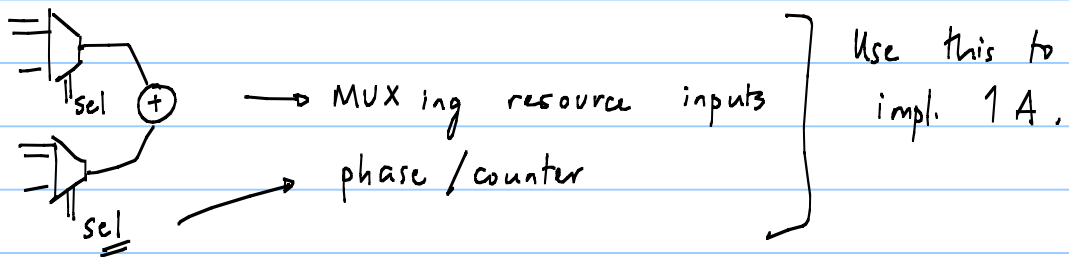
Coefficients : $h_0 \dots h_5$



Assume : mult, add each take 1 cycle

Critical path : $m_1 - a_1 - a_2 - a_3 - a_4 - a_5 = 6$ cycles

Cycle #	Ops.	Resources
1:	m_1 m_2 m_3 m_4 m_5 m_6	6 M
2:	a_1	1 A
3:	a_2	1 A
4:	a_3	1 A
5:	a_4	1 A
6:	a_5	1 A



Resource utilization: What % of time is resource used.

eg. 1A: 6 clock cycles \Rightarrow max 6 additions

Here we do 5 \Rightarrow Utilization = $5/6 = 83\%$

Multipliers: 6 M, 6 cycles \Rightarrow 36 mults.

Utilization = $6/36 = 16.67\%$

m_1, m_2 must be in cycle 1, else a_1 cannot be in 2.

But other mults can move to later. cycles.

1:	m_1	m_2	$2M$	
2:	a_1	m_3	m_4	$2M, 1A$
3:	a_2	m_5	m_6	$2M, 1A$
4:	a_3			$1A$
5:	a_4			$1A$
6:	a_5			$1A$

Overall : # mults = max over all cycles # mults in that cycle.
 $= 2M$

adds = $1A$

Utilization : Add : $5/6 = 83.33\%$

Mult : $6/12 = 50\%$ (prev. 16.67%).

Tighter resource constraint: 1M, 1A.

1: m_1

2: m_2

Util: Mult: $6/7 \approx 84\%$

3: a_1 m_3

Add: $5/7 = 73\%$

4: a_2 m_4

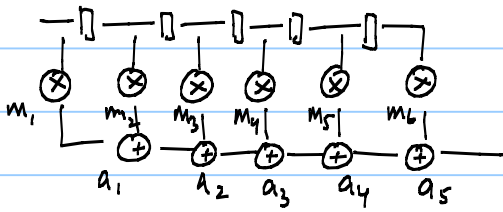
5: a_3 m_5

6: a_4 m_6

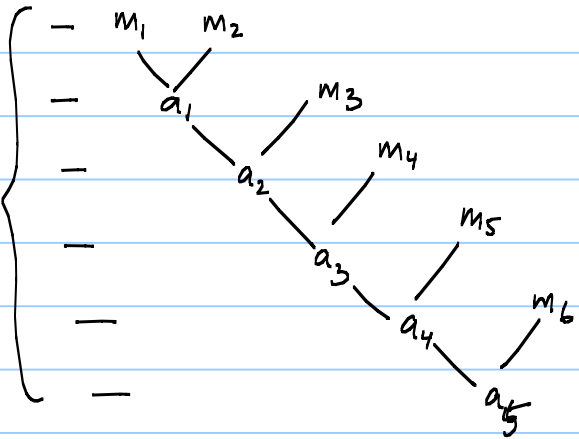
7: a_5

(Delays)

Registers can be removed while understanding dependencies

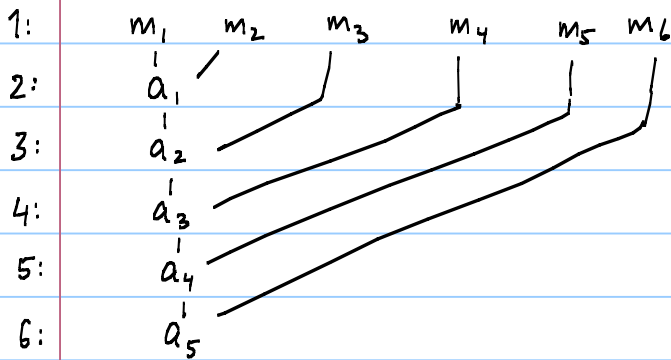


min 6
cycles.



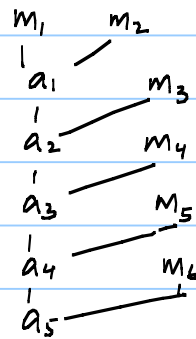
As Soon As Possible schedule

ASAP



As Late As Possible

ALAP



Mobility : $ALAP_{time} - ASAP_{time}$ for each function

eg. Mobility $(m_1) = 1 - 1 = 0$

$(m_3) = 2 - 1 = 1$

$(m_6) = 5 - 1 = 4$

Time bound (theoretical) = $\frac{\text{Total \# of ops of a type}}{\text{\# resources of that type.}}$

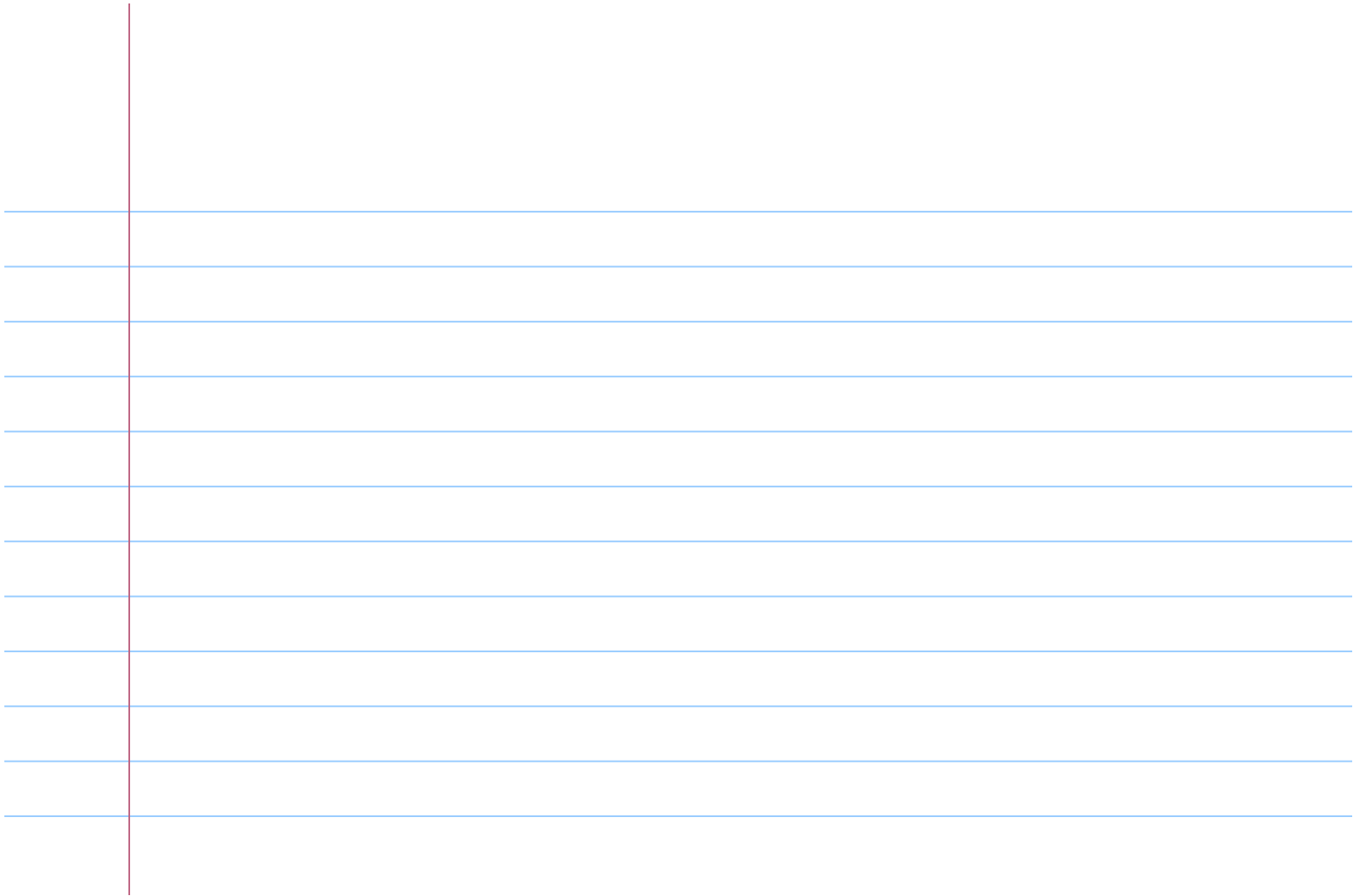
System bound = max over all types of resources

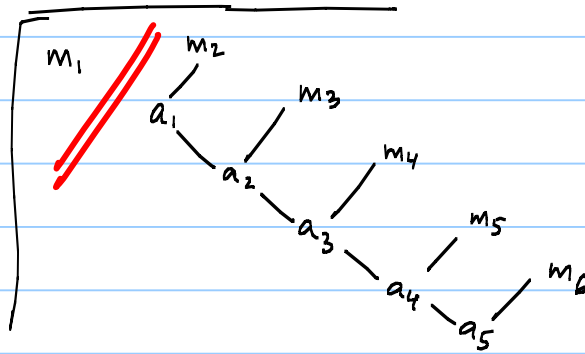
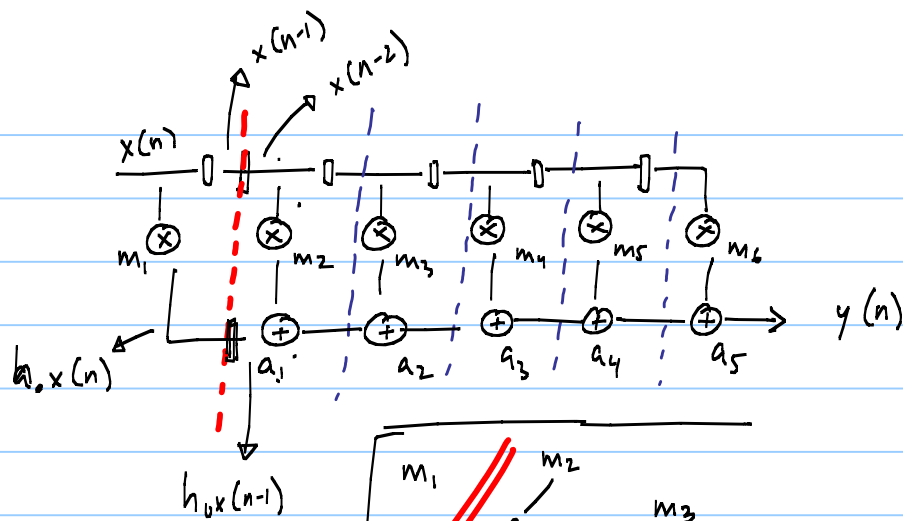
eg: 6 Mults, 2 M \Rightarrow min 3 time units.

1 M \Rightarrow min 6 time units.

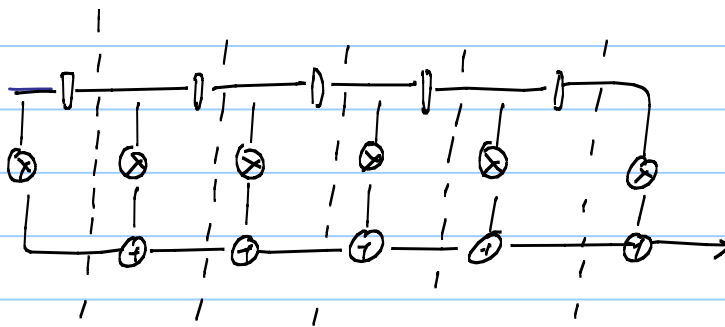
Addition 1 A \Rightarrow min 5 time units

If resource constraint = (1M, 1A) \Rightarrow $\max(6, 5) = \underline{\underline{6}}$ time units



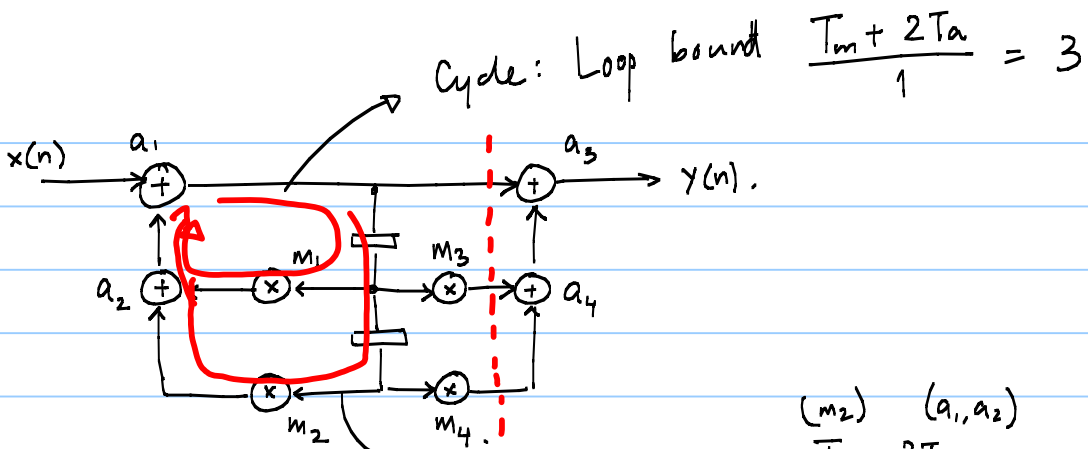


1:	m_2		} Iteration/ Sample
2:	a_1	m_3	
3:	a_2	m_4	
4:	a_3	m_5	
5:	a_4	m_6	
6:	a_5	<u>m_1</u>	



m_1	m_2	m_3	m_4	m_5	m_6
	a_1	a_2	a_3	a_4	a_5

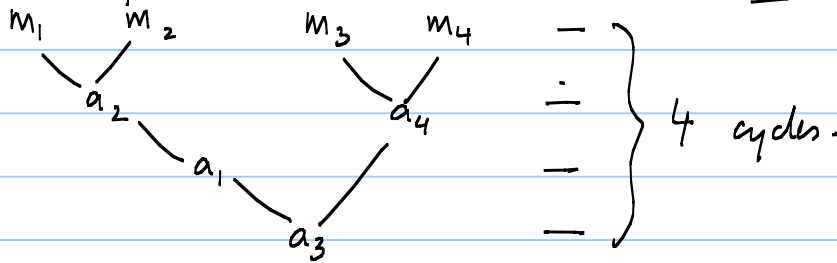
If $GM, 5A \Rightarrow$ all mults in cycle 1, all adds in 2.
2 cycles sufficient

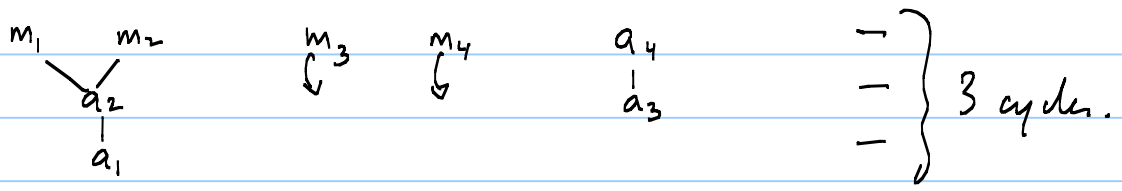


Cycle: Loop bound $\frac{T_m + 2T_a}{1} = 3$

Loop bound: $\frac{(m_2) (a_1, a_2) T_m + 2T_a}{2} = 1.5$

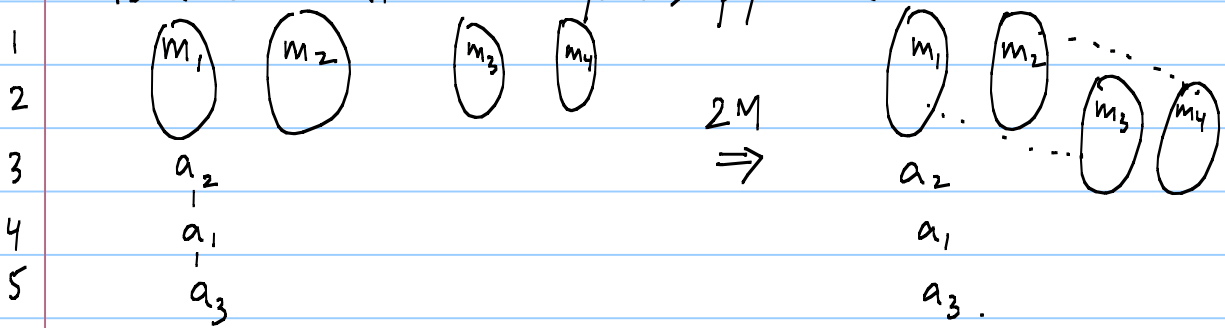
Iteration period bound = $\max(3, 1.5) = \underline{\underline{3}}$





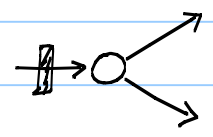
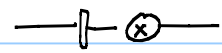
2 mults 1: m_1 m_2 a_4
 2 addrs 2: m_3 m_4 a_2 a_3
 3: a_1

Assume mult = 2 cycles, pipelined.

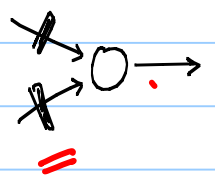
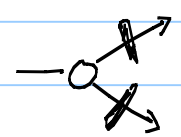




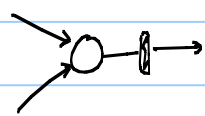
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Retiming - extension of pipelining

