Phase locked loop frequency synthesizers
SMDP Instructional Enhancement Program

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13-24 Nov 2006
Local oscillator requirements

- Generate equally spaced frequencies from an input reference frequency
- Waveform shape not very important
- Spurious output must be sufficiently low
- Noise must be sufficiently low
Digital frequency divider can generate multiple frequencies
Frequencies not equally spaced
Reference frequency higher than output frequencies
Voltage multiplier

voltage difference zero, at steady state

\[ V_{\text{out}}/N = V_{\text{ref}} \text{ at steady state} \]

- A controlled source to generate the output voltage
- Divided output voltage subtracted from the reference to generate error
- Output source controlled by the integral of the error
A controlled source to generate the output frequency
  - A voltage controlled oscillator

Divided output frequency subtracted from the reference frequency to generate error

Output source controlled by the integral of the frequency error

\[ f_{\text{out}} / N = f_{\text{ref}} \text{ at steady state} \]
Phase and frequency

- Sinusoid $\cos(\theta(t))$
- Phase: $\theta(t)$
- Instantaneous frequency $f_i = \frac{1}{2\pi} \frac{d\theta(t)}{dt}$
- Typically expressed as $f_i = f_o + f_e(t)$ where $f_o$ is the average frequency and $f_e$ is the instantaneous frequency error
- Phase $\theta(t) = 2\pi f_o t + \Phi_o + 2\pi \int f_e(t)dt$
- Phase $\theta(t) = 2\pi f_o t + \Phi_o + \phi(t)$
  - $\Phi_o$: phase offset
  - $\phi(t)$: instantaneous phase
Frequency multiplier

\[ \cos(2\pi f_{\text{ref}} t) \]  
\[ \text{frequency measure} \]  
\[ f_{\text{ref}} \]  
\[ K_2 \int dt \]  
\[ \Sigma \]  
\[ V_{\text{ctl}} \]  
\[ K_{\text{vco}} V_{\text{ctl}} + f_0 \]  
\[ \cos(2\pi f_{\text{out}} t) \]  

\[ \cos(2\pi f_{\text{ref}} t) \cos(2\pi f_{\text{out}} t) \cos(2\pi f_{\text{out}}/N t) \]

\[ f_{\text{out}}/N = f_{\text{ref}} \text{ at steady state} \]

- Integration before subtraction
- Integral of the frequency is phase
- Integrator+subtractor measures phase difference between the reference input and the divided output (feedback)

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Use a phase detector to generate the control voltage

\[ V_{\text{ctl}} = K_{pd}(\phi_{\text{ref}} - \phi_{\text{out}}/N) \]

\[ f_{\text{out}}/N = f_{\text{ref}} \text{ at steady state} \]
Voltage controlled oscillator

\[ f_{\text{out}} = K_{\text{vco}} V_{\text{ctl}} + f_0 \]

\[ f_{\text{vco}} = f_0 + K_{\text{vco}} V_{\text{ctl}} \]

\[ \theta_{\text{vco}} = 2\pi f_0 t + 2\pi K_{\text{vco}} \int V_{\text{ctl}} \, dt \]

\[ K_{\text{vco}}: \text{VCO gain in Hz/V} \]
Phase detector

$\phi_1$  \hspace{5cm} $K_{pd}(\phi_1 - \phi_2)$  \hspace{5cm} $\phi_2$

\textbf{K}_{pd}: phase detector gain

- $K_{pd}$: Phase detector gain in V/radian
- Ideal phase detector: assumed to have an output
  
  $V_{pd} = K_{pd}(\phi_1 - \phi_2)$
At steady state, $f_{\text{ref}} = f_{\text{out}}/N$; $V_{\text{ctl}} = \Phi_{\text{ref}} - \Phi_{\text{out}}/N$

- Modelled in terms of phases of signals
- At steady state (lock), $V_{\text{ctl}}$ is a constant $\Rightarrow f_{\text{ref}} = f_{\text{out}}/N$.
- The loop locks with $V_{\text{ctl}} = K_{pd}(\Phi_{\text{ref}} - \Phi_{\text{out}}/N) = (Nf_{\text{ref}} - f_{o})/K_{vco}$—This is the “operating point” of the circuit
An increment $\phi_{ref}$ in the input phase causes increments $\phi_{out}$, $V_{ctl}$
An increment \( \phi_{\text{ref}} \) in the input phase causes increments \( \phi_{\text{out}}, v_{\text{ctl}} \)

Type-I loop—One integrator in the loop
Phase locked loop model—frequency domain

\[ \phi_{\text{ref}}(s) \rightarrow + \sum \rightarrow K_{pd} \rightarrow V_{\text{ctl}}(s) \rightarrow \frac{2\pi K_{vco}}{s} \rightarrow \phi_{\text{out}}(s)/N \rightarrow 1/N \rightarrow \phi_{\text{out}}(s) \]

- Loop gain \( L(s) = \frac{2\pi K_{pd} K_{vco}}{N} \)
- Transfer function \( \frac{\phi_{\text{out}}(s)}{\phi_{\text{ref}}(s)} = \frac{N}{1 + Ns/(2\pi K_{pd} K_{vco})} \)
- Type-I loop—One integrator in the loop
Phase error when locked ($f_{out} = Nf_{ref}$):

$$\Phi_{ref} - \Phi_{out}/N = (Nf_{ref} - f_o)/K_{vco}K_{pd}$$

$$-\pi < \Phi_{ref} - \Phi_{out}/N < \pi \Rightarrow$$

$$f_o - \pi K_{pd}K_{vco} < f_{out} < f_o + \pi K_{pd}K_{vco}$$

Lock range limited by periodicity of phase detector (period of all phase detectors not necessarily $\pm \pi$)

$K_{pd}K_{vco}$ large for wide lock range
XOR phase detector

\[ \Delta \Phi = \Phi_{\text{ref}} - \Phi_{\text{div}} \]

Average value = \( 2\Delta \Phi / \pi - 1 \)

Output periodic at \( 2f_{\text{ref}} \)

\[
V_{\text{out}}(f) = \frac{2}{\pi} \left( \Delta \Phi - \frac{\pi}{2} \right) \delta(f) + \frac{4\Delta \Phi}{\pi} \sum_{n=1}^{\infty} \text{sinc} \left( \frac{n\Delta \Phi}{\pi} \right) e^{-jn\Delta \Phi} \delta(f - 2nf_{\text{ref}})
\]

\[
V_{\text{out}}(t) = \frac{2}{\pi} \left( \Delta \Phi - \frac{\pi}{2} \right) + \frac{4\Delta \Phi}{\pi} \sum_{n=1}^{\infty} \text{sinc} \left( \frac{n\Delta \Phi}{\pi} \right) \cos(4\pi nf_{\text{ref}} t - n\Delta \Phi)
\]
XOR phase detector

- Output average value: \( \frac{2\Delta \Phi}{\pi} - 1 = \frac{2}{\pi}(\Delta \Phi - \frac{\pi}{2}) \)
  - \( K_{pd} = \frac{2}{\pi} \)
  - Phase detector offset: \( \frac{\pi}{2} \)
- Loop locks with: \( \frac{\Phi_{\text{ref}} - \Phi_{\text{out}}}{N} = \frac{\pi}{2} \)
  for \( Nf_{\text{ref}} = f_o \)
- Output range: \( \pm \frac{\pi}{2} \) around an offset of \( \frac{\pi}{2} \)
- PLL lock range: \( f_o - \frac{\pi}{2K_{pd}K_{vco}} < f_{\text{out}} < f_o + \frac{\pi}{2K_{pd}K_{vco}} \)
- Output contains \( 2f_{\text{ref}} \) and its harmonics
- Output: \( \frac{2}{\pi}(\Delta \Phi - \frac{\pi}{2}) + \sum_n a_n \cos(4\pi nf_{\text{ref}}t + \alpha_n) \)
- Periodic signal in addition to \( K_{pd}\Delta \Phi \)
- All real phase detectors have a periodic “error” in addition to the “dc” term proportional to phase error
XOR phase detector-Error spectrum

\[ \phi_{\text{ref}} - \phi_{\text{div}} = \pi/2 \]

\[ \phi_{\text{ref}} - \phi_{\text{div}} = \pi/4 \]
PLL with XOR phase detector

$$\sum_n a_n \cos(4\pi f_{ref} t + \alpha_n) \text{ ("error")}$$

- Error $E(t)$ added to the input of the phase detector
- Disturbances in the VCO phase $\phi_{out}(t)$, even with a perfect reference ($\phi_{ref}(t) = 0$)
- VCO output: $\cos(2\pi N f_{ref} t + N \Phi_{ref} - \pi/2 + \phi_{out}(t))$
- VCO output not periodic at $N f_{ref}$
PLL with XOR phase detector

Graph showing ideal phase, error, and phase with error over a range of phase values from 0 to 10.
PLL with XOR phase detector—frequency domain

\[ E(s) = \sum_n a_n e^{j\alpha_n} \delta(f-2nf_{\text{ref}}) \]

\[ \phi_{\text{ref}}(s) = 0 \text{ for a perfectly periodic reference} \]

- Transfer function from the error to the output
  \[ \frac{\phi_{\text{out}}(s)}{E(s)} = \frac{\phi_{\text{out}}(s)}{\phi_{\text{ref}}(s)} = \frac{N}{1} + \frac{Ns}{(2\pi K_{\text{pd}} K_{\text{vco}})} \]
- \[ E(j2\pi f) = \sum_n a_n \exp(j\alpha_n) \delta(f - 2nf_{\text{ref}}) \]
Type-I PLL

\[
\frac{\phi_{out}(s)}{E(s)} = \frac{\phi_{out}(s)}{\phi_{ref}(s)} = \frac{2\pi K_{pd} K_{vco} / Ns}{1 + 2\pi K_{pd} K_{vco} / Ns} \quad (2)
\]

\[
= \frac{1}{1 + \frac{sN/2\pi K_{pd} K_{vco}}{1}} \quad (3)
\]

Loop gain

\[
L(s) = \frac{2\pi K_{pd} K_{vco}}{Ns} \quad (5)
\]

Closed loop bandwidth

\[
f_{-3dB} = \frac{K_{pd} K_{vco}}{N} \quad (6)
\]
Type I PLL

\[ |L| = 2\pi K_{pd} K_{vco}/N \]

\[ |\phi_{out}/\phi_{ref}| \]

\[ 20\log(N) \]

\[ (\text{loop bandwidth}) \]

\[ \omega \]

\[ \text{dB} \]

\[ \text{loop gain } |L| \]
Feedback system

In our system,

\[ \frac{\phi_{out}(s)}{E(s)} = N \frac{2\pi K_{pd} K_{vco} / Ns}{1 + 2\pi K_{pd} K_{vco} / Ns} \]  \hspace{1cm} (7)

In general, in a feedback system with a loop gain \( L(s) \)

\[ H_{closed\ loop}(s) = H_{ideal}(s) \frac{L(s)}{1 + L(s)} \]  \hspace{1cm} (8)

\[ H_{closed\ loop}(s) = H_{ideal}(s) \frac{L(s)}{1 + L(s)} \]  \hspace{1cm} (9)

Where \( H_{ideal}(s) \) is the ideal closed loop gain (with \( L = \infty \)). This can be approximated as

\[ H_{closed\ loop}(s) = H_{ideal}(s) L(s) \quad |L| \ll 1 \]  \hspace{1cm} (10)

\[ = H_{ideal}(s) \quad |L| \gg 1 \]  \hspace{1cm} (11)
Output phase error (constant phase offsets ignored)

\[
\phi(j2\pi f) = \sum_{n} a_n H(j4\pi nf_{\text{ref}}) \exp(j\alpha_n) \delta(f - 2nf_{\text{ref}}) \quad (12)
\]

\[
= \sum_{n=1}^{\infty} b_n \exp(j\beta_n) \delta(f - 2nf_{\text{ref}}) \quad (13)
\]

\[
\phi(t) = \sum_{n=1}^{\infty} b_n \cos(4\pi nf_{\text{ref}} t + \beta_n) \quad (14)
\]

\[
V_{\text{out}}(t) = \cos(2\pi Nf_{\text{ref}} t + \sum_{n=1}^{\infty} b_n \cos(4\pi nf_{\text{ref}} t + \beta_n)) \quad (15)
\]
PLL with XOR phase detector—Output signal

Considering only the term at $2f_{\text{ref}}$, and $b_1 \ll 1$

$$V_{\text{out}}(t) = \cos(2\pi N f_{\text{ref}} t + b_1 \cos(4\pi f_{\text{ref}} t + \beta_1))$$

$$= \cos(2\pi N f_{\text{ref}} t) \cos(b_1 \cos(4\pi f_{\text{ref}} t + \beta_1))$$

$$- \sin(2\pi N f_{\text{ref}} t) \sin(b_1 \cos(4\pi f_{\text{ref}} t + \beta_1))$$

$$\approx \cos(2\pi N f_{\text{ref}} t) - b_1 \cos(4\pi f_{\text{ref}} t + \beta_1) \sin(2\pi N f_{\text{ref}} t)$$

$$= \cos(2\pi N f_{\text{ref}} t) - b_1 / 2 \sin(2\pi (N + 2) f_{\text{ref}} t + \beta_1)$$

$$- b_1 / 2 \sin(2\pi (N - 2) f_{\text{ref}} t + \beta_1)$$

- Spurious tones in the output at $2f_{\text{ref}}$ from the desired frequency
- Reference feedthrough
- In general, spurious tones will be present at $n f_{\text{ref}}$ from the desired PLL output
\[ b_1 = a_1 |H(j4\pi f_{\text{ref}})| \quad (22) \]
\[ = a_1 N \left| \frac{K_{pd}K_{\text{vco}}/j2Nf_{\text{ref}}}{1 + K_{pd}K_{\text{vco}}/j2Nf_{\text{ref}}} \right| \quad (23) \]
\[ \approx a_1 N \left| \frac{K_{pd}K_{\text{vco}}}{j2Nf_{\text{ref}}} \right| \quad (24) \]
\[ \frac{4}{\pi} N \frac{f_{-3dB}}{2f_{\text{ref}}} \quad (25) \]
To generate 1 GHz from 1 MHz reference
- $b_1 = 10^{-2}$ (spurious tones 46 dB below the oscillation level)
- $N = 10^3$

$$f_{-3dB}/f_{ref} = \frac{\pi}{2} \times 10^{-5} \Rightarrow f_{-3dB} = 5\pi \text{ Hz}$$

Lock range $= \pi N f_{-3dB} \approx 50 \text{ kHz}$

Lock range is too small; It can’t switch to the next channel which is 1 MHz away!
Relationship between magnitude and phase [Bode]

-20dB/dec
-40dB/dec
-60dB/dec

\[ \text{dB} \]

\[ \omega \]

\[ p_1 \quad p_2 \quad z_1 \quad p_3 \]

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Phase locked loop frequency synthesizers
All poles and zeros of the network assumed to be real and in the left half plane.

- The magnitude plot (log-log) consists of segments of slope $20k$ dB/decade
- Poles and zeros form breakpoints between segments
- At each pole the slope increments by $-20$ dB/decade
- At each zero the slope increments by $+20$ dB/decade
- Phase at poles/zeros will be $m\pi/4$ radians
- Derivative of phase is positive at a zero and negative at a pole
Stability criteria for negative feedback loops

Phase locked loop frequency synthesizers

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Stability criteria for negative feedback loops

All poles and zeros of the loop gain function assumed to be real and in the left half plane.

- Phase margin should be greater than a specified amount (assume 45°)
- Phase lag at $\omega_u$ should be less than 125°
- At $\omega_u$, the Bode plot should have a slope of -20 dB/decade
Increasing the lock range of the phase detector

- Increase $K_{pd}K_{vco}$ at all frequencies
- Causes increased reference feedthrough
Increasing the lock range of the phase detector-II

- Increase $K_{pd}K_{vco}$ only at dc (steady state phase error reduces)
- In the limit, use an integrator $K_{pd,I}/s \Rightarrow$ steady state phase error reduces to zero
- Two integrators in a loop $\Rightarrow$ unstable system
- Increased attenuation slope can reduce reference feedthrough

- Decrease reference feedthrough
- $2\pi K_{pd,I}K_{vco}/Ns^2$
- $2\pi K_{pd}K_{vco}/Ns$
- $|\Phi_{vco}/\Phi_{ref}|$
- $20\log(N)$
- $0dB$
- $\omega$
- $\omega_{ref}$
- $2\pi K_{pd,I}K_{vco}/N$ 
- $(2\pi K_{pd,I}K_{vco}/N)^{1/2}$
- $L/(1+L)$
- $0dB, \text{loop gain}$

In the limit, use an integrator $K_{pd,I}/s \Rightarrow$ steady state phase error reduces to zero

Two integrators in a loop $\Rightarrow$ unstable system

Increased attenuation slope can reduce reference feedthrough

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Increasing the lock range of the phase detector-III

- Increase $K_{pd}K_{vco}$ only at dc (steady state phase error reduces)
- In the limit, use an integrator $K_{pd,I}/s \Rightarrow$ steady state phase error reduces to zero
- Maintain $-20$ dB/decade slope at unity loop gain $\Rightarrow$ introduce a zero before $\omega_u$
- Introduce a pole beyond $\omega_u$ to increase attenuation of reference feedthrough
Type II PLL—with two poles and a zero

At steady state, reference input and divider output have the same frequency and phase

The integrator’s output stabilizes to the value required to make the VCO to oscillate at \( Nf_{\text{ref}} \)

At steady state, \( V_{\text{ctl}} = (Nf_{\text{ref}} - f_{\text{o}})/K_{\text{vco}} \)
Type II PLL—Additional attention poles

At steady state, $f_{\text{ref}} = f_{\text{out}} / N$; \( \Phi_{\text{ref}} - \Phi_{\text{out}} / N = 0 \);

- Additional poles beyond the unity loop gain frequency to reduce reference feedthrough
Type II PLL—Frequency domain

\[ p_1 > 2\pi K_{pd}K_{vco}/N \]

more poles can be used

\[ \phi_{ref}(s) \rightarrow \sum \rightarrow K_{pd} \rightarrow + \rightarrow v_{ctl}(s) \rightarrow \sum \rightarrow \frac{1}{1+s/p_1} \rightarrow V_{ctl} \rightarrow \frac{2\pi K_{vco}}{s} \rightarrow \phi_{out}(s) \]

\[ \phi_{out}(s)/N \rightarrow 1/N \rightarrow \phi_{ref}(s) \]

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Type II PLL—Implementation

- XOR gate with a current output ($\pm I_{cp}$)
  - Integral term $K_{pd} \cdot I / s$: Current flowing into a capacitor $C_1$
  - Proportional term $K_{pd}$: Current flowing into a resistor $R_1$
  - Series RC to obtain the sum

- Additional capacitor $C_2$ to introduce the second pole
Type II PLL with an XOR phase detector

- Loop locks with $\pi/2$ offset between $\phi_{ref}$ and $\phi_{vco}/N$ for all frequencies.

- Periodic error $E(t)$ is a 50% duty cycle square wave at $2f_{ref}$.

$$E(t) = 2 \sum_{n=1}^{\infty} \text{sinc} \left( \frac{n}{2} \right) \cos(4\pi n f_{ref} t - n\pi/2)$$
Type II PLL with an XOR phase detector-Frequency domain

\[ E(j2\pi f) = \sum_n a_n e^{j\alpha_n} \delta(f - 2nf_{\text{ref}}) \]

\[ E(s) \]

\[ \frac{K_{pd,I}}{s} \]

\[ \frac{2\pi K_{vco}}{s} \]

\[ \phi_{\text{ref}} \]

\[ \phi_{\text{out}} / N \]

\[ \phi_{\text{out}} \]

In-phase

Quadrature

Phase

Gain

VCO

Phase locked loop frequency synthesizers
Type II PLL with an XOR phase detector

- Lock range is not limited by phase detector
- Large error signal even under lock $\Rightarrow$ significant reference feedthrough
- XOR output sensitive to duty cycle of inputs
- Better to have a phase detector with zero output for zero phase error
- Better to have a phase detector sensitive only to the edges
- Loop bandwidth can be widened while maintaining low reference feedthrough
Tri state phase detector

Output $+1, -1, 0$

- $+1$ if reference leads divider output
- $-1$ if reference lags divider output
- $0$ if reference coincides with divider output

$$\text{output} = Q_A - Q_B$$
Tri state phase detector-waveforms

\[ \Delta \Phi = \Phi_{\text{ref}} - \Phi_{\text{div}} \]

- A leading B
- A lagging B

Flip flops assumed to be reset instantaneously
Tri state phase detector-reset path delay

\[ \Delta \Phi = \Phi_{\text{ref}} - \Phi_{\text{div}} \]

A leading B
- \( Q_A \) and \( Q_B \) simultaneously high for a short duration
- \( Q_A \) – \( Q_B \) proportional to \( \Delta \Phi \)

A lagging B


- $Q_A$ and $Q_B$ drive a charge pump
- Average current driven into the loop filter is $I_{cp} \Delta \Phi / 2\pi$
Tri state phase detector implementation

D latch with reset and D="1"

(S input with "1" implicit)

Realization using SR latches

Realization using NOR gates

- D flip flops with reset implemented using SR latches
Tri state phase detector-Current source mismatch

- Ideally $\Delta \Phi = 0$ under lock in a type-II loop $\Rightarrow$ no reference feedthrough (loop filter input $= 0$)
- Mismatch between top and bottom current sources causes a non zero $\Delta \Phi = 0$ and reference feedthrough
Type-II PLL: transfer functions

\[ L(s) = \frac{2\pi K_{pd,1} K_{VCO}}{Ns^2} \left(1 + \frac{sK_{pd}}{K_{pd,1}}\right) \quad (26) \]

\[ \frac{\phi_{out}(s)}{\phi_{ref}(s)} = N \frac{1 + \frac{sK_{pd}}{K_{pd,1}}}{s^2 \frac{N}{2\pi K_{pd,1} K_{VCO}} + s \frac{K_{pd}}{K_{pd,1}} + 1} \quad (27) \]

\[ \frac{\phi_{out}(s)}{V_{n,ctl}(s)} = \frac{N}{K_{pd}} \frac{sK_{pd}}{s^2 \frac{N}{2\pi K_{pd,1} K_{VCO}} + s \frac{K_{pd}}{K_{pd,1}} + 1} \quad (28) \]

\[ \frac{\phi_{out}(s)}{\phi_{VCO}(s)} = \frac{s^2 \frac{N}{2\pi K_{pd,1} K_{VCO}}}{s^2 \frac{N}{2\pi K_{pd,1} K_{VCO}} + s \frac{K_{pd}}{K_{pd,1}} + 1} \quad (29) \]
Type-II PLL: transfer functions

\[
\frac{L(s)}{1 + L(s)} = \frac{1 + s K_{pd} / K_{pd,I}}{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}} + s \frac{K_{pd}}{K_{pd,I}} + 1}
\]  

(30)

- 2 poles and a zero
- Zero \( z_1 = -K_{pd,I} / k_{pd} \)
- Natural frequency \( \omega_n = \sqrt{2\pi K_{pd,I} K_{vco} / N} \)
- Quality factor \( Q = \sqrt{NK_{pd,I} / 2\pi K_{vco} / K_{pd}} \), damping factor \( \zeta = 1 / 2Q = K_{pd} / 2 \sqrt{NK_{pd,I} / 2\pi K_{vco}} \)
- For well separated (real) poles, \( p_1 \approx -K_{pd,I} / k_{pd} \), \( p_1 \approx -2\pi K_{pd} K_{vco} / N + K_{pd,I} / k_{pd} \)
- Pole zero doublet \( p_1, z_1; p_1 \) at a slightly higher frequency than \( z_1 \)
Type-II PLL: Reference input

\[
\frac{\phi_{\text{out}}(s)}{\phi_{\text{ref}}(s)} = N \frac{1 + sK_{pd}/K_{pd,l}}{s^2 \frac{N}{2\pi K_{pd,l}K_{vco}} + s \frac{K_{pd}}{K_{pd,l}} + 1}
\]  

(31)

- Low pass response; Reference noise attenuated at high frequencies
- Low frequency gain of \(N\), -3 dB bandwidth of \(2\pi K_{pd}K_{vco}/N\)
- Pole zero doublet \(p_1 \approx z_1 = K_{pd,l}/kpd; p_1\) at a slightly higher frequency than \(z_1\)
Type-II PLL: Noise added to control node

$$\phi_{out}(s) \over V_{ctl}(s) = \frac{N}{K_{pd}} \cdot \frac{sK_{pd}/K_{pd,l}}{s^2 \cdot \frac{N}{2\pi K_{pd,l} K_{vco}} + s \cdot \frac{K_{pd}}{K_{pd,l}} + 1}$$

- radians/Volt
- Bandpass response
- Mid band gain of $N/K_{pd}$
- Lower cutoff at $K_{pd,l}/kpd$, Upper cutoff at $2\pi K_{pd} K_{vco}/N$
\[ \frac{\phi_{\text{out}}(s)}{\phi_{\text{vco}}(s)} = \frac{s^2 N}{2\pi K_{pd,I} K_{vco}} + s \frac{K_{pd}}{K_{pd,I}} + 1 \]  

- Second order highpass response
- Feedback loop effectively inactive beyond \( 2\pi K_{pd} K_{vco}/N \)
Type-II PLL phase noise example

$$S_\phi(f) \text{ dBC/Hz}$$

Due to vco

$$\frac{K_{pd,I}}{K_{pd}}$$

Due to reference oscillator

$$2\pi K_{pd} K_{vco} / N$$

Total phase noise

$$S_\phi(f) \text{ dBC/Hz}$$

Reference dominated

$$\frac{K_{pd,I}}{K_{pd}}$$

VCO dominated

$$2\pi K_{pd} K_{vco} / N$$

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Phase locked loop frequency synthesizers
Lossless LC resonator sustains a sinusoidal voltage indefinitely.

LC resonator loss modeled using a parallel resistance $R_p$.

Compensate the loss of a lossy LC resonator using a parallel negative resistance $G_N$.

Oscillation frequency $f_o = 1/2\pi \sqrt{LC}$.
LC resonator losses

\[ R_{p,L} = \frac{(\omega L)^2}{R_{s,L}} \cong Q_L^2 R_{s,L} \]

\[ R_{p,C} = \frac{1}{(\omega L)^2 R_{s,C}} \cong Q_C^2 R_{s,C} \]

- Capacitor and Inductor series resistances represented by equivalent parallel resistances
- Effective \( R_p \) is a parallel combination of losses from all components

\[ R_p = R_{p,L} || R_{p,C} \]
Negative resistance-implementation

Transconductor connected in positive feedback

Transconductance $G_N$ in positive feedback
Cross coupled differential pair

Negative conductance = $\frac{g_m}{2}$ where $g_m$ is the transconductance of each MOS device
Parallel LC tank with cross coupled differential pair

This and its variants are the most commonly used topologies of CMOS integrated oscillators
Complete switching of MOS devices assumed

Equivalent to a square wave current of amplitude $I/2$ driving the parallel LC tank
LC oscillator-amplitude

"bias" point

I/2

I/2

driving current

fundamental component

v(t)

sinusoid at f_0

fundamental component

v_P - v_n

differential voltage

M_1 off

M_2 on

M_1 on

M_2 off

I/2

I/2

I/2

I/2

T_0

2I/\pi

1/2

2I/\pi

1/2

2IR_P/\pi

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Phase locked loop frequency synthesizers
LC oscillator-amplitude

- Equivalent to a square wave current of amplitude $I/2$
driving the parallel LC tank
- All components except the fundamental filtered out
- Amplitude of the differential sinusoidal voltage $= 2IR_P/\pi$
LC oscillator-tunability

- Tunable using a varactor
- Reverse biased p-n junction
- MOS device in accumulation—larger tuning range; more popular in CMOS ICs
Accumulation MOS varactor

- nMOS in n-well
- Multi fingered structure to reduce gate, “channel” resistance
- $W \sim$ few microns
- $L > L_{\text{min}}$ to reduce parasitics
- Gate can be contacted at both ends to further reduce resistance

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MOS varactor with differential excitation

- Interdigitated fingers—alternate ones connected to $a_p$ and $a_n$
- Region between gates connected to $a_p$ and $a_n$ at 0 V due to symmetry
- All n+ contacts except the ones at the end can be removed [5]
- Smaller structure, lower series resistance, and smaller parasitic capacitances
On chip inductors

Planar inductor on one of the metal layers
Top level metal preferred
  - Farther from the substrate
  - Smaller parasitic capacitance
  - Lesser coupling to substrate, and hence, loss

Thicker top level metal (∼ 2 μm) available in mixed signal processes
Inductor loss mechanisms

- Winding resistance
  - $R_{\square} L/W$
  - Effective $R_{\square}$ larger due to skin effect
  - Copper: $2 \mu m$ skin depth ($\propto 1/\sqrt{f}$) at 1 ghz

- Capacitive coupling to substrate and its resistance
- Inductive coupling to (resistive) substrate
- Quality factors upto 15 possible, typically 8-10
- Use adequate thickness and number of vias during layout
Symmetrical differential inductor

- More compact for a given differential inductance
- Larger potential difference between turns ⇒ larger effect of interwinding parasitics

Symmetrically laid out single ended inductors

- Greater area
- Interwinding parasitic capacitance not very significant
Inductor simulation

- Some processes have scalable inductor library and models
- Typically needs to be simulated from process parameters—metal thickness, resistivity, intermetal spacing etc.
- Inductance value
  - FastHenry, Asitic etc.
  - Accurate estimation possible
- Quality factor
  - FastHenry, Asitic etc.
  - Harder to accurately estimate losses due to substrate coupling
- Parasitic capacitance
  - First order parallel plate estimation—OK for single ended inductors
  - FastCap etc.
  - Use distributed models for accuracy
Bias current is a function of tank losses and desired amplitude

- Maximize the inductance for a large amplitude from a small current

Transistors typically minimum length at high frequencies—longer to lower $1/f$ corner

Bias source: longer than minimum length to lower $1/f$ noise

Minimize all parasitics to maximize tuning range from the varactor

Transistor $W/L$ to get the desired $g_m$ for startup in the worst case

- Large $g_m \Rightarrow$ increased phase noise; So don’t go crazy!
- \( L = 4 \text{nH} \) and \( C = 0.25 \text{pF} \) (differential) chosen
- 6 turn inductor on top metal layer, \( \approx 140 \text{\mu m} \) square
- From inductor simulations, \( Q \approx 6 \)
- Minimum length transistors

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Phase locked loop frequency synthesizers
5GHz VCO layout
frequency vs Vctl curve

Vctl (V) vs frequency (in GHz)

VCO (higher freq. version)-measured f vs. V

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Phase locked loop frequency synthesizers
VCO-simulated phase noise

Phase Noise

Phase Noise (dBc/Hz)

Frequency offset from carrier (Hz)

-30 dB/decade

-20 dB/decade
Programmable divider-Synchronous counter

- All of the circuitry running at full speed
- Very high power dissipation
- Asynchronous operation preferred
Programmable divider-Pulse swallow architecture

Dual modulus prescaler $\div P/P + 1$

Divide by $P + 1$ for $A$ cycles

Divide by $P$ for $M - A$ cycles

Full cycle $= (P + 1)A + P(M - A) = MP + A$

Only the dual modulus prescaler running at full speed

Programmability using $M$ and $A$
References


