Special Manpower Development Program in VLSI Design
IEP : Radio Frequency Integrated Circuit Design

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1 MOSFET g_M vs $(V_{GS} - V_{T0})$

For a MOSFET, we usually use the equation

$$I_{DS} = \mu_n C'_{ox} \left(\frac{W}{2L}\right) (V_{GS} - V_{T0})^2 \quad (1)$$

which results in

$$g_m = \mu_n C'_{ox} \left(\frac{W}{L}\right) (V_{GS} - V_{T0}) \quad (2)$$

.This problem checks the validity of this for the UMC 0. 18 μm process that you are using. Use a minimum length device.

a. For a device operating in saturation with $V_{GS} = V_{DS}$, plot g_m as a function of $(V_{GS} - V_{T0})$.

b. It turns out that at high $(V_{GS} - V_{T0})$, the mobility of the carriers in the channel is reduced, and one way of modeling this is to write the drain current as

$$I_{DS} = \left(\frac{\mu_n}{1 + \Theta(V_{GS} - V_{T0})}\right) C'_{ox} \left(\frac{W}{2L}\right) (V_{GS} - V_{T0})^2 \quad (3)$$

From the curve you have generated in (a) above, estimate Θ.

2 PRELIMINARY LNA DESIGN

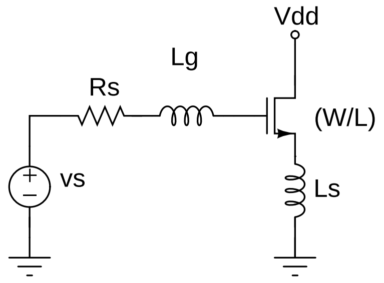

Figure 1: LNA input circuit.

Figure 5 shows the small signal picture of an LNA. The frequency band of operation is a few megahertz around 1.9 GHz. The amplifier input must be matched to 50 Ω. The input circuit must be resonant at 1.9 GHz, and the quality factor is to be 3.

a. Assume Vdd is 2 V. Design a bias circuit so that the current through the device is 1 mA.

b. Calculate the noise figure of the circuit, where the output of interest is the drain current of the transistor. Compare with simulation. Repeat for Q's of 6 and 9.

c. Simulate the IIP2 and IIP3 of the LNA for Q's of 3, 6 and 9. How do these change with Q ?

3 LNA Gm STABILIZATION

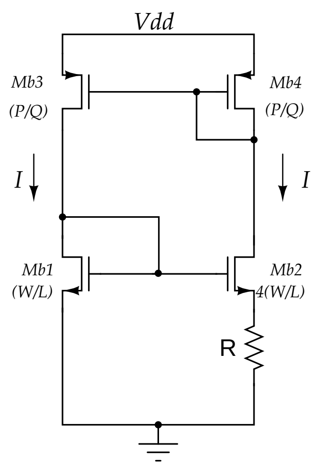

Figure 2: Basic fixed G_m bias circuits.

The input Q and S11 of the LNA depend on g_m. A fixed LNA bias current implies that g_m will vary with temperature. In practice, C_{gs} is fairly stable, so that one needs to take care of only the variation in g_m. Figure 2 shows a circuit that attempts to stabilize the transconductance of a transistor. It is one of many circuits that are called "fixed transconductance bias" circuits. The idea is to "servo" the g_m of a "master" device ($Mb1$ in the cases discussed below) to a stable external resistor R. Once this is done, all devices whose transconductance need stabilization are biased at the same operating point as the "master" device in the "servo" circuit. Use the circuit of Figure 4 to determine the transconductance of M1.

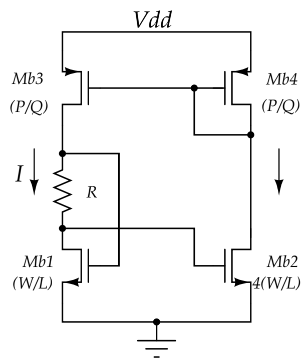

Figure 3: A fix for the body effect problem.

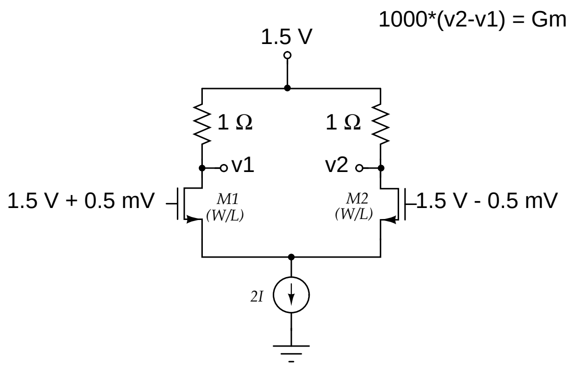

Figure 4: Measuring transconductance of M1.

a. First, analyze the circuit of Figure 2 (a). Assume that the bodies of all devices are tied to their sources and neglect output impedance of the devices. $\mathrm{V_{dd}}$ is 3.3 V. Find the current I and the transconductance of $Mb1$.

b. Simulate the circuit in SPICE. Choose minimum length for all NMOS devices. $\mathrm{V_{dd}}$ is 3.3 V. Choose R to be $1\,\mathrm{K\Omega}$, and the gate overdrive of $Mb1$ to be $V_{gs} - V_t = 250\,\mathrm{mV}$. Plot the $\mathrm{G_m}$ of $M1$ as temperature is varied from $0 - 70^o\,\mathrm{C}$. Next, keep temperature fixed at 300K and vary Vdd from 2.5-3.5 V. What is the variation in transconductance ?

c. A fix for the body effect problem is shown in Figure 3. Analyze this circuit and redo (b) for this circuit. What do you notice ?

4 DIFFERENTIAL LNA DESIGN

A differential LNA with the circuit topology shown in Figure 5 is to be designed. Assume $\mathrm{R_L} = 250\,\Omega$. $\mathrm{L_{package}}$ represents the bondwire inductances of the package, and each has a value of 3 nH. The pads have a capacitance of 25 fF each. Each input port of the LNA should be matched to 50 Ohms. The supply voltage is 3.3 V. The maximum tail current Ibias allowable is 2.5 mA. The LNA should be functional and must meet the following performance specifications over the entire commercial temperature range of 0-70 degree centigrade and a $\pm 10\%$ change in supply voltage. Design the appropriate biasing circuitry.

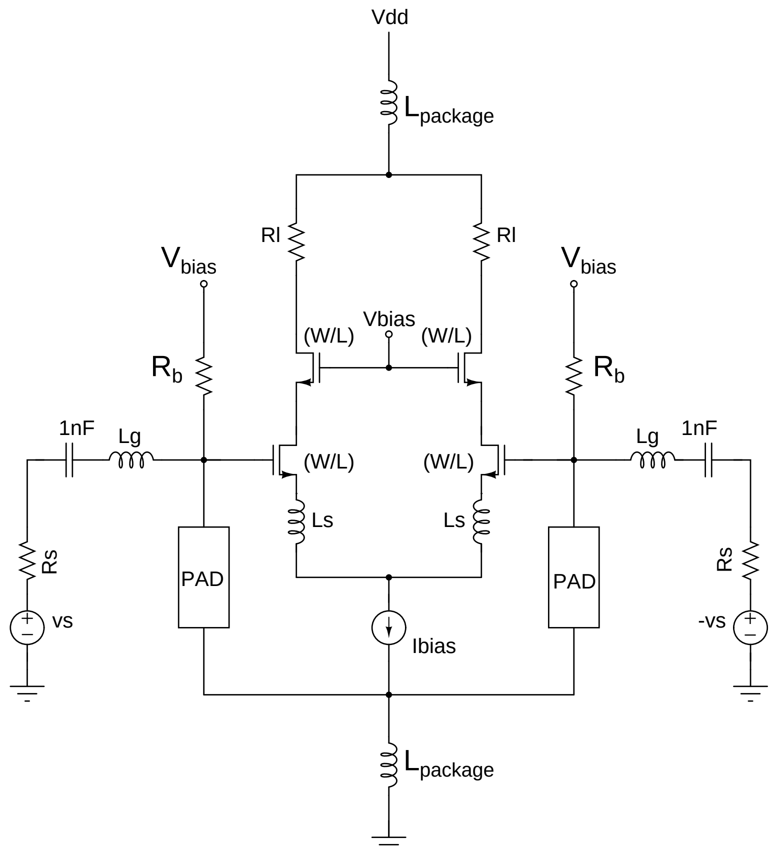

Figure 5: Fully differential LNA.

a. $|S_{11}|$ should be less than -12 dB.

b. Voltage gain (ratio of differential output to differential input source voltage) of 16 dB.

Determine the IIP3 of your LNA.