

**Indian Institute of Technology Madras
Global Initiative of Academic Network (GIAN) Programme**

Name	Mingoo Seok
Designation	Assistant Professor
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Title of the Course	Near/sub-threshold circuits and architectures for microprocessors
Content of the Course	
(a) <u>Overview of the Course:</u> In this course, we will introduce recent and important techniques for designing ultra-low-power computing hardware (e.g., microprocessors) in near/sub-threshold digital circuits for creating ultra-low-power Internet of the Things (IoT) devices. We will study techniques ranging across layers from transistors to gates to architectures. Those techniques aim to address three important challenges in near/sub-threshold voltage circuits, namely extreme variability, active leakage, and low computing throughput. The course consists of five three-hour lectures, assignments, and a final exam.	
(b) <u>Objectives of the course:</u> The goal of the course is to have students understand key challenges in designing near/sub-threshold voltage digital computing hardware and also learn techniques to address them.	
(c) <u>Syllabus and lecture-wise outline of the course:</u> The topics that will be covered in lectures are as follow. Lecture 1: motivations; near/sub-threshold voltage circuits; transistor characteristics in near/sub-threshold voltages Lecture 2: gate-level design; standard-cell design optimization Lecture 3: variability challenge overview: sensor-based adaptive design; adaptive design based on in-situ error detection and correction techniques part-1 Lecture 4: adaptive design based on in-situ error detection and correction techniques part-2 Lecture 5: pipeline and parallel architectures in near/sub-threshold voltage circuits.	
Prerequisites: Students are expected to be familiar with digital circuit design and logic design, and	

preferably also with microprocessor architectures, typically covered in senior-year undergraduate or first-year master programs.

Evaluation Pattern for the Course

Weightage (in %) for Assignments	50
Weightage (in %) for Examination(s)	50

