VLSI Data Conversion Circuits: Problem set 4

Note Title 3/14/2011

1) Design a single-bit continuous-time ΣΔ modulator for the following specifications. The quantizer levels are −1V & 1V. Assume an NRZ DAC.

1. Signal bandwidth = 1 MHz
2. Peak S&NR > 100 dB
3. Peak SNR (including thermal + quantization noise) > 84 dB
4. If your roll number is even, choose a CIFF loop filter. If it is odd, use a CIFB loop.

(a) Choose an appropriate order, sampling rate & NTF.

(b) Plot the NTF and analytically determine the in-band quantization noise.

(c) Using simulation, find the MSA & peak S&NR. Plot the spectrum for an input sinusoid of 250 kHz. There must be atleast 128 bins in the signal band.

(d) Now design a continuous-time loop filter that realizes the NTF. This consists of three sub steps.

i) Find the loop filter transfer function, assuming 1/2 clock cycle delay in the comparator.

2) Assuming active-RC integrators and ideal opamps,* draw the loop filter schematic, with all component values. You can use ideal gains of -1 to realize inversion where necessary.

* ideal opamps : VCCS with a <u>large</u> g_m.

3) Simulate the modulator and scale the components for dynamic range. You may assume that the integrating resistors of integrators other than the first are 8 times the input resistor.

4) Run a .AC simulation of the loop filter only, and plot the input referred noise spectral density, and show that the inband SNR spec is satisfied. (Assume OTAs are noiseless)

5) Verify the alias rejection property by plotting the CTDSM output spectra for

(a) a 100 mV peak input tone @ 250 kHz

(b) a 100 mV peak input tone @ (f_s + 250 kHz)

How does this compare with the theoretical rejection.

(c) Plot the theoretical NTFs when all capacitors deviate from their nominal values by $\pm$ 20 %. Compare these with the nominal NTF. The plots should be on a log scale.

(f) What white RMS jitter is needed on the clock to ensure that the in-band SNR does not worsen by more than 1 dB?