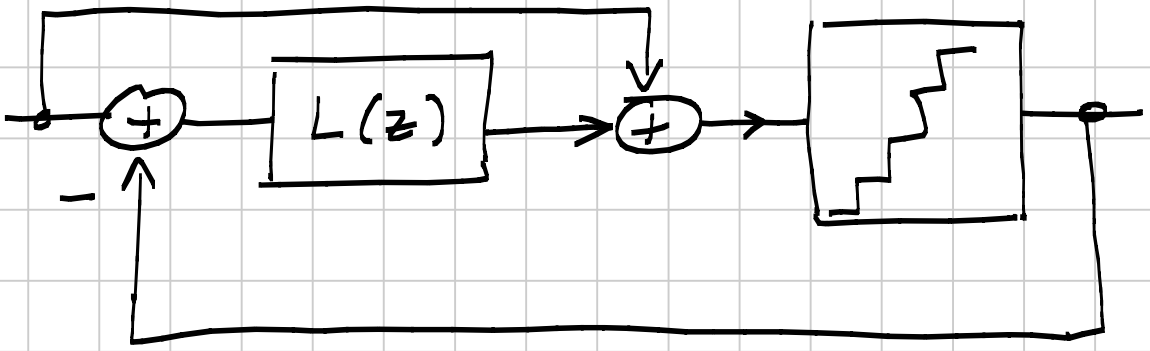
VLSI Data Conversion Circuits: Assignment 3

Note Title 2/20/2011

Problem 1: Design a fourth order NTF, based on a prototype Butterworth highpass filter, with all zeroes at $z = 1$. Assuming that the $\Sigma\Delta$ modulator architecture is as shown below,



(a) determine $L(z)$, if the OBG = 1.5

(b) What is the STF?

(c) Assuming a 5 level quantizer, with each step being $\Delta = 2$, analytically determine the inband quantization noise for an OSR = 64.

(d) Use the toolbox to put in a slow ramp as discussed in class, and evaluate the MSA.

(e) Simulate the modulator for a sinusoid at $\omega_{in} = \pi/4 \cdot OSR$, and an amplitude of 1db

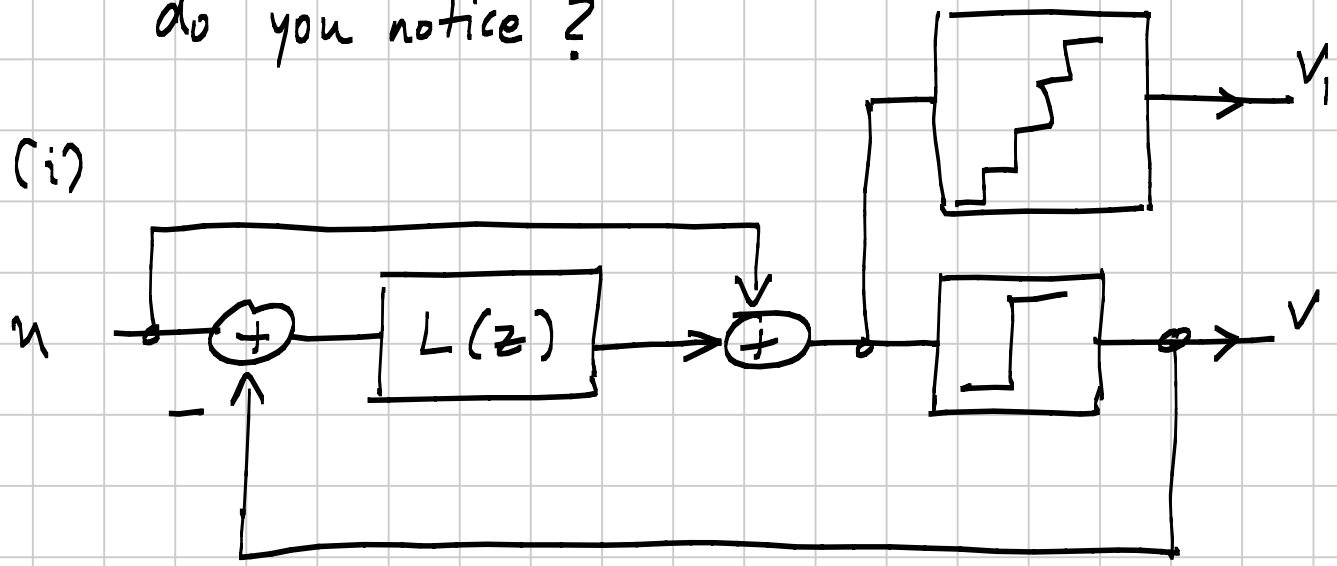
below the MSA. What is the simulated SQNR? How does it compare with your analytic estimate?

(f) Assume now that the quantizer is non ideal in that the ADC levels are displaced from their ideal values in the following manner. The error in each ADC threshold is a Gaussian random variable with $\sigma = 0.1$. Rerun the simulation of part (e) now - what is the degradation in the SNR?

(g) Assume now that the quantizer is non ideal in that the DAC levels are displaced from their ideal values in the following manner. The error in each DAC level is a Gaussian random variable with $\sigma = 0.1$. Rerun the simulation of part (e) now - what is the degradation in the SNR?

(h) The quantizer is now replaced with a single bit design, with output levels from -4 to 4. Determine the MSA, and repeat parts (e), (f) and (g). What do you notice?

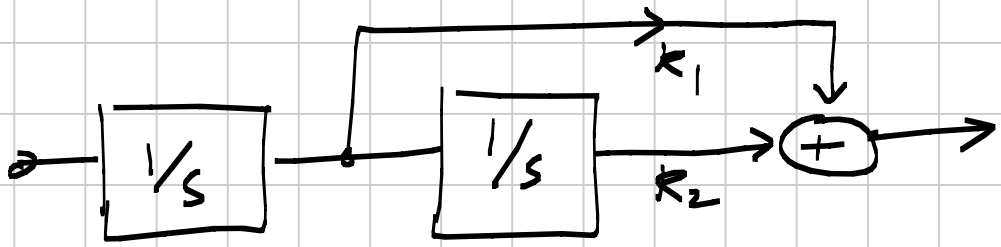
(i)



An improvement to the single bit design of part (g) is shown above, where both single bit and multibit quantizers are used. How will you process V & V_1 to increase SQNR? Again, repeat parts (e), (f) & (g) for this architecture.

Problem 2 :-

The architecture of the loop filter of a second order CTDSM is shown below



Determine k_1 & k_2 so that the NTF is $(1 - z^{-1})^2$ for the following DAC pulses

(a) Impulsive

(b) RZ pulse

As usual, the sampling rate is 1 Hz.