VLSI DATA CONVERSION CIRCUITS : PROBLEM SET 2

Problem 1

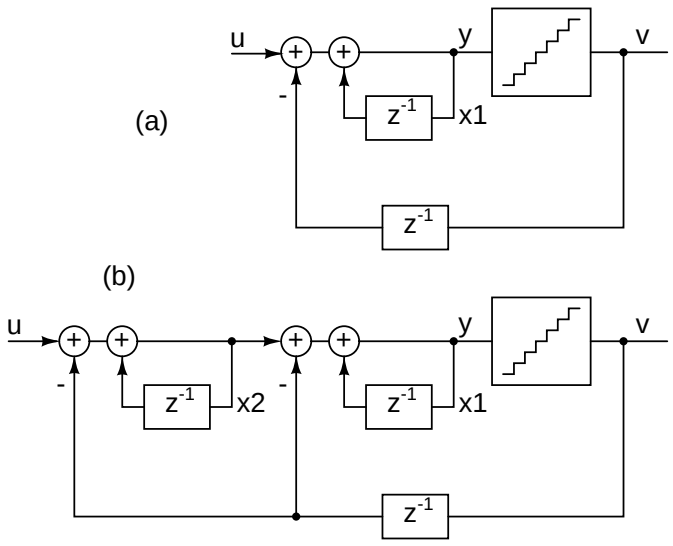

Figure 1: $\Delta\Sigma$ modulators for Problem 1.

Fig. 1 shows the block diagrams of first and second order $\Delta\Sigma$ modulators. Assume that the quantizer input range is [-1,1], and has a step size of 0.125. The analog input is a sinewave with 0.7 V amplitude, and a frequency of 1 kHz. $f_s = 256$ kHz.

1. Write MATLAB code to simulate both modulators. Run the code so that you obtain 2^{16} output samples. Include the code in your report.

2. Plot the PSD of the outputs of both modulators on the same graph. Use a 4096-point Hann windowed FFT in the PSD computations.

3. For the first order modulator, replace the quantizer with an additive uniformly distributed noise source in the range [-1/16,1/16]. Plot the PSD of v and compare with the PSD obtained when there was a quantizer in the loop. Why do you think this is happening ?

4. To avoid the problem seen in part (3) above, one can *dither* the quantizer input. Dither refers to adding a small random noise source at the quantizer input. Repeat part (2) above, now by adding Gaussian white dither with a standard deviation of 0.01 at the quantizer input. What do you observe about the PSD now, when compared to that you saw in part (2)?

Problem 2

Using a Butterworth highpass filter prototype, determine the NTF of a fourth order $\Delta\Sigma$ modulator with an Out of Band Gain (OBG) of three. All the zeros of the NTF are to be at the origin. Assuming that the Maximum Stable Amplitude (MSA) is 80% of the 5-bit (32-level) quantizer, and an OSR=16, determine the in-band peak SQNR in dB.

Problem 3

This problem investigates the benefits of complex NTF zeroes over an NTF with all zeroes at z=1. For a third order NTF with OBG=3, determine the optimal positions of the zeros that minimize the in-band quantization noise. How many dB improvement is this over a design with all zeroes at z=1? Assume a large OSR, so that the magnitude of the NTF denominator is constant in the signal band.

Problem 4

This problem examines how a poor decimation filter can mar performance of an oversampled ADC. Figure 2 shows the block diagram of a second order $\Sigma\Delta$ modulator, followed by a digital filter, and a downsampler. The $\Sigma\Delta$ modulator internally uses a quantizer with an RMS noise of e_{rms}.

1. Draw the spectra at all block outputs. For discrete time signals, mark the frequency axis in terms of the discrete time frequency variable ω.

2. The digital filter following the modulator has an impulse response as shown. What is its DC gain ? What is the noise power at $Vout$. How does this compare with the noise when an ideal brickwall filter with a cutoff frequency of π/OSR is used as the digital filter ?

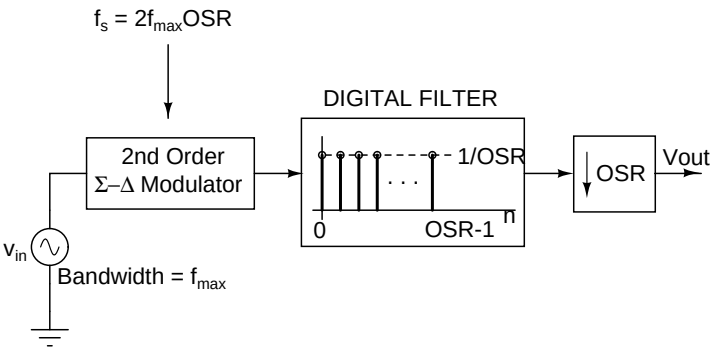

Figure 2: Diagram for Problem 4.