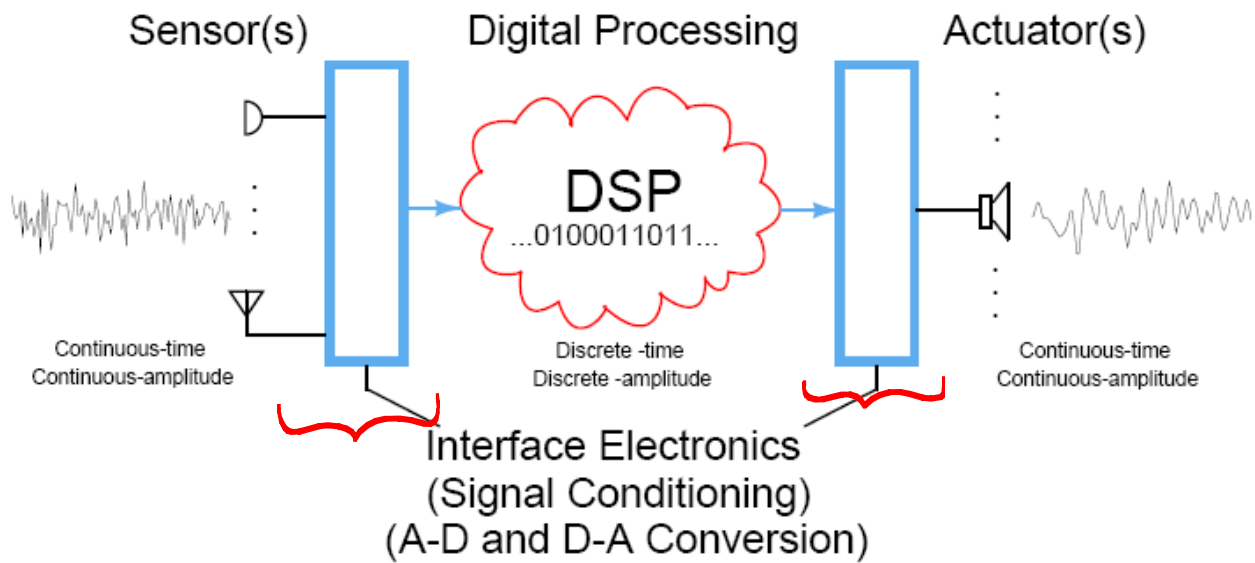


VLSI Data Conversion Circuits : Lecture 1

Note Title

02-12-2010



→ Continuous-time, Continuous Amplitude

Sampling



Quantization

→ Discrete time, → Discrete Amplitude
(levels $\rightarrow \infty$)

* Sampling

→ Analysis

→ Circuits

→ Characterize

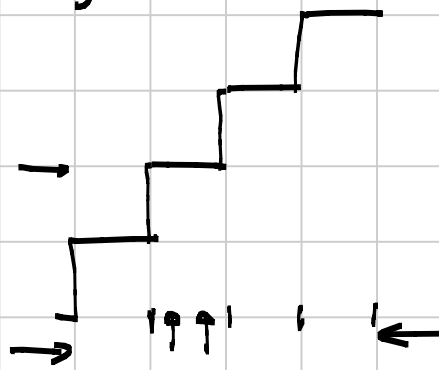
Nyquist Theorem

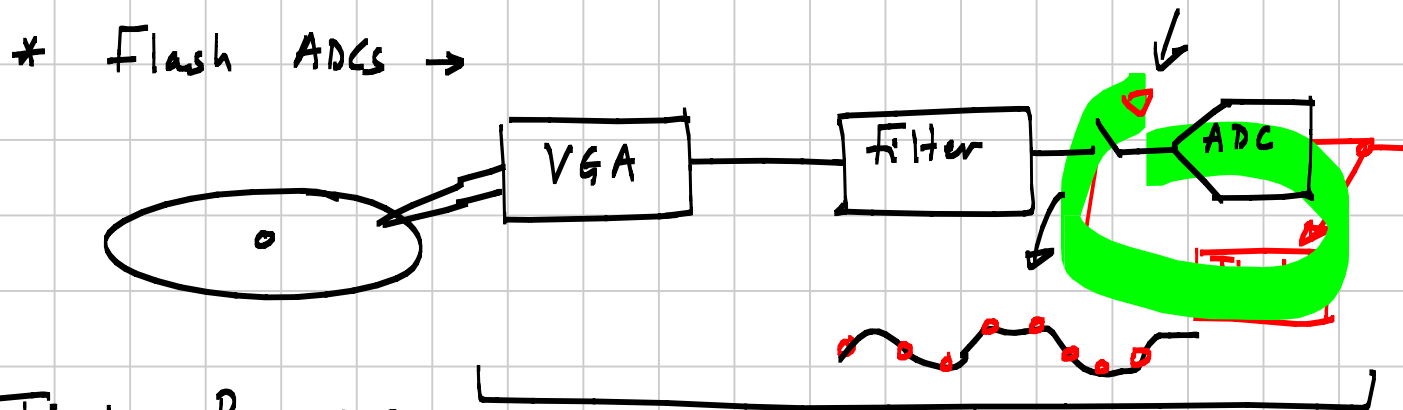
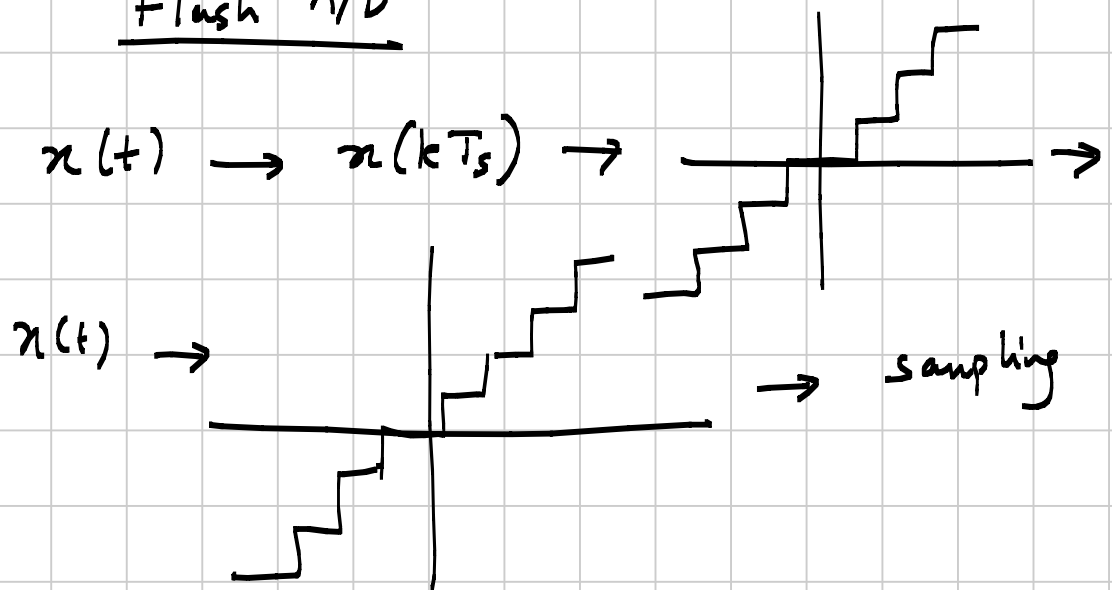
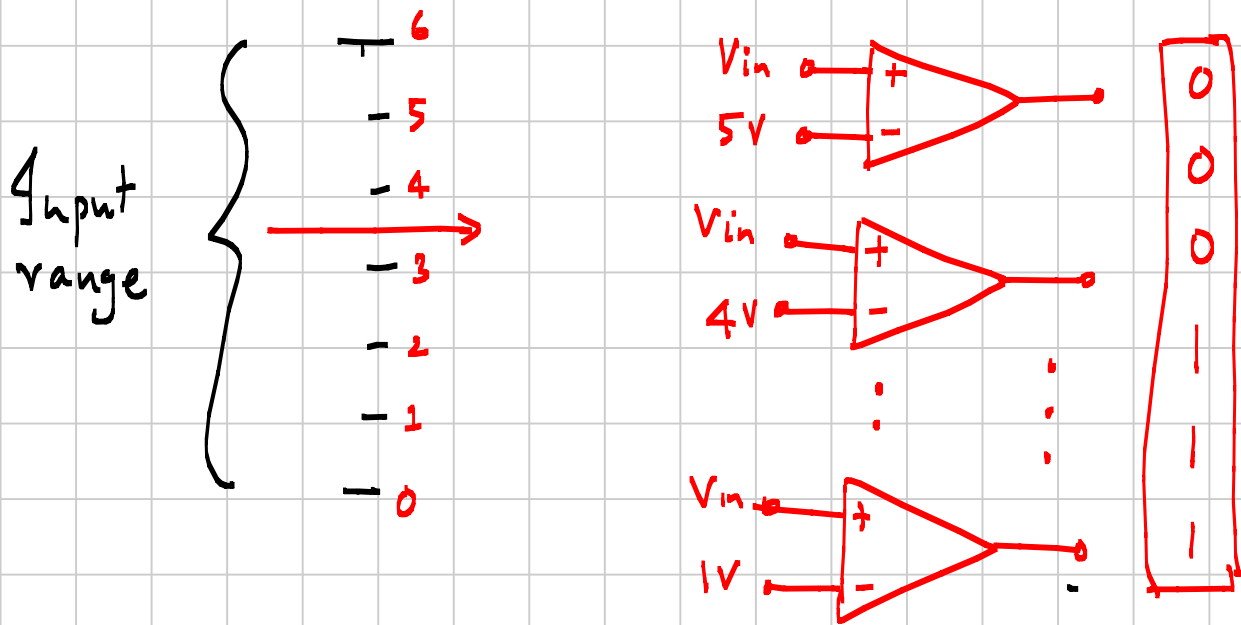
DSP, Analog, Devices, Control.

* Quantization

→ Design

→ Characterize





Timing Recovery

$\rightarrow$ Disk Drive Read Channel $\rightarrow$ 6 bit

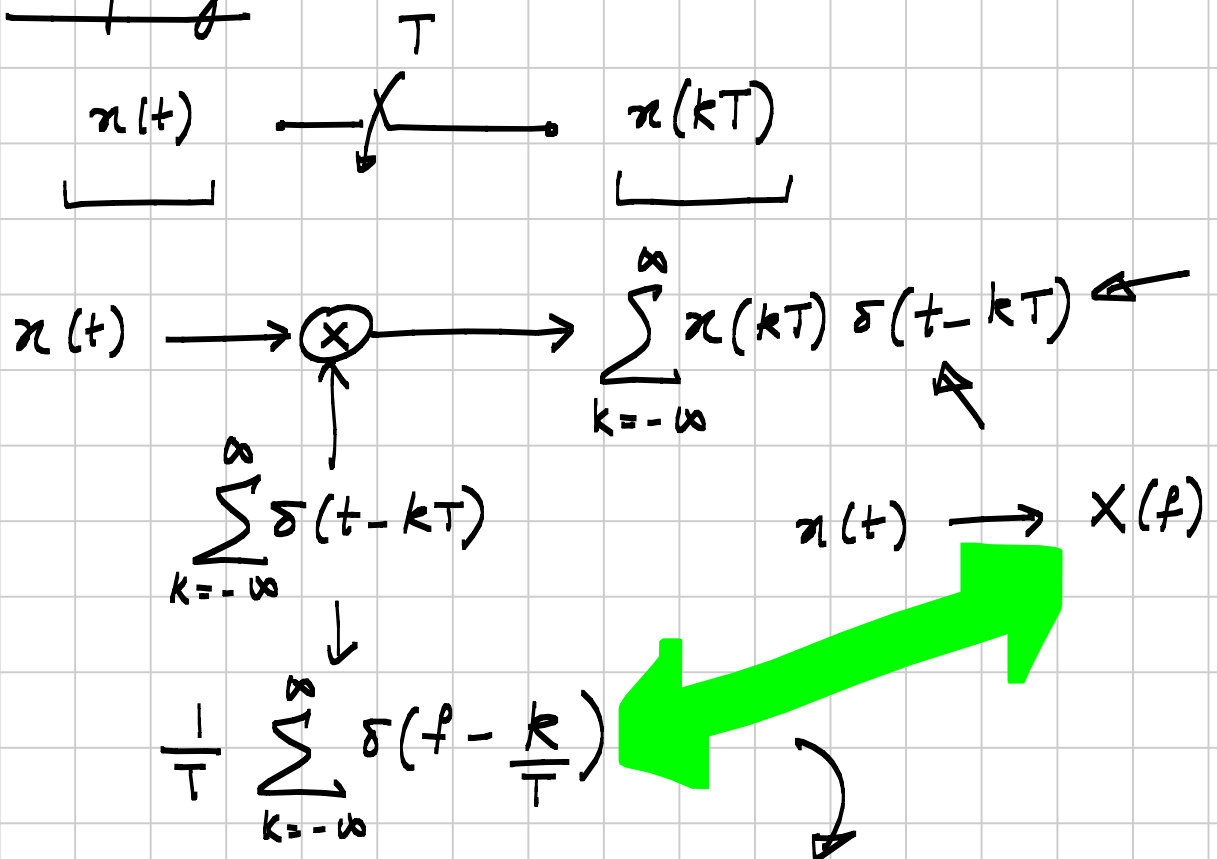
* D/A Conversion

$\rightarrow$ Design

$\rightarrow$ Characterize



Sampling:



$$\sum_{k=-\infty}^{\infty} x(kT) \delta(t - kT) \rightarrow \frac{1}{T} \sum_{k=-\infty}^{\infty} x\left(f - \frac{k}{T}\right)$$

$$\sum_{k=-\infty}^{\infty} x(kT) e^{-j2\pi f T k}$$

$$\sum_{k=-\infty}^{\infty} x(kT) e^{-j\omega k}$$

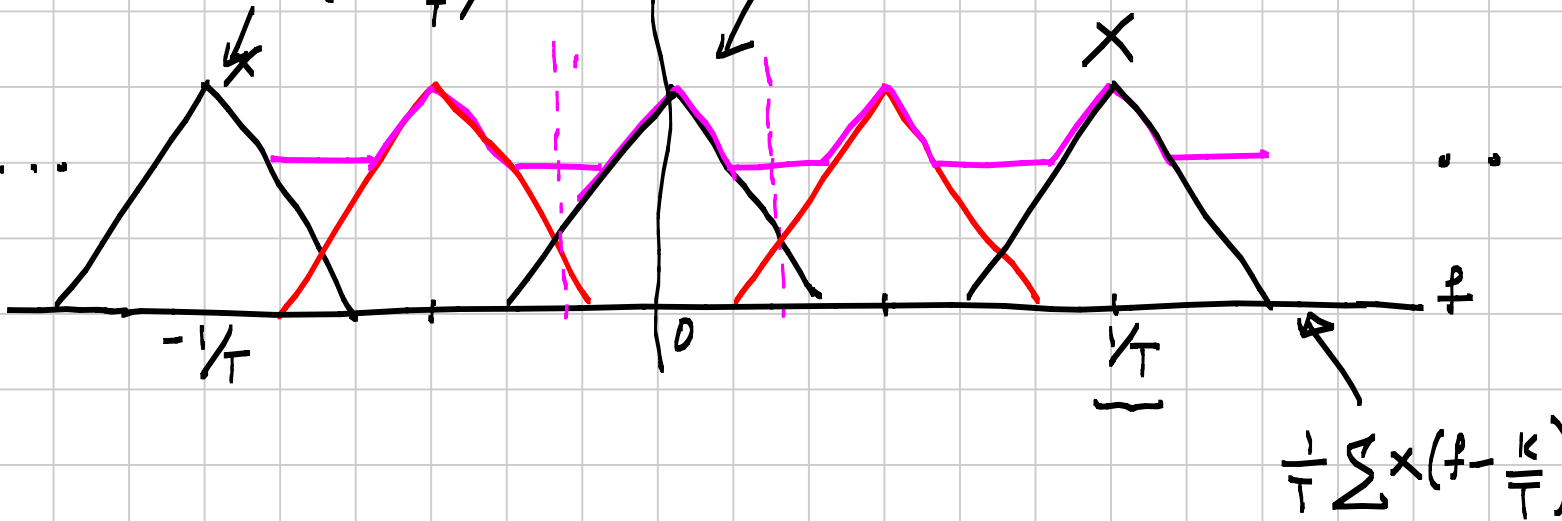
D.T. F.T of the sampled sequence

$$2\pi f T \rightarrow \omega$$

f	ω
0	0
$\frac{1}{T}$	2π
$\frac{1}{2T}$	π

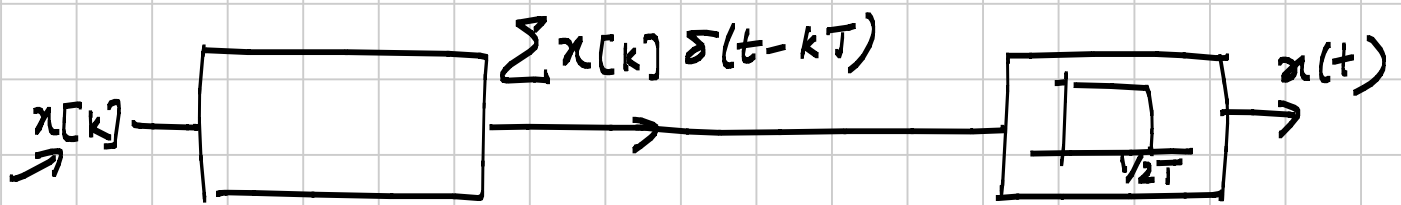
$$* \frac{1}{T} \sum_{k=-\infty}^{\infty} x\left(f - \frac{k}{T}\right)$$

$$x\left(f + \frac{1}{T}\right) \quad x(f) \quad x\left(f - \frac{1}{T}\right)$$



$$\frac{1}{T} \sum_{k=-\infty}^{\infty} x(kT) \delta(t - kT)$$

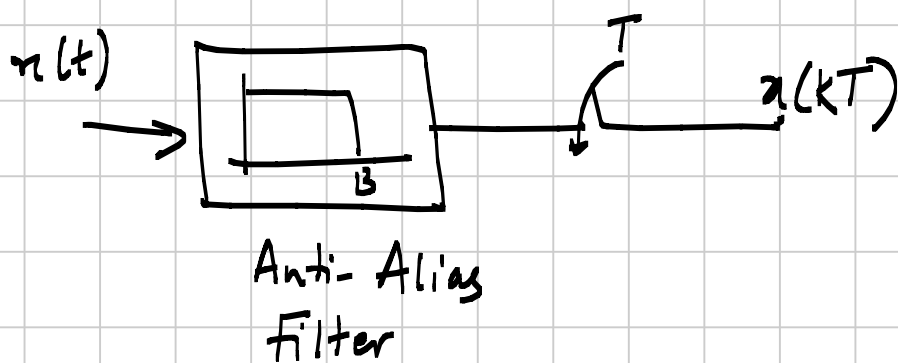
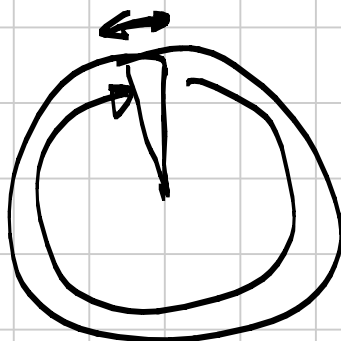
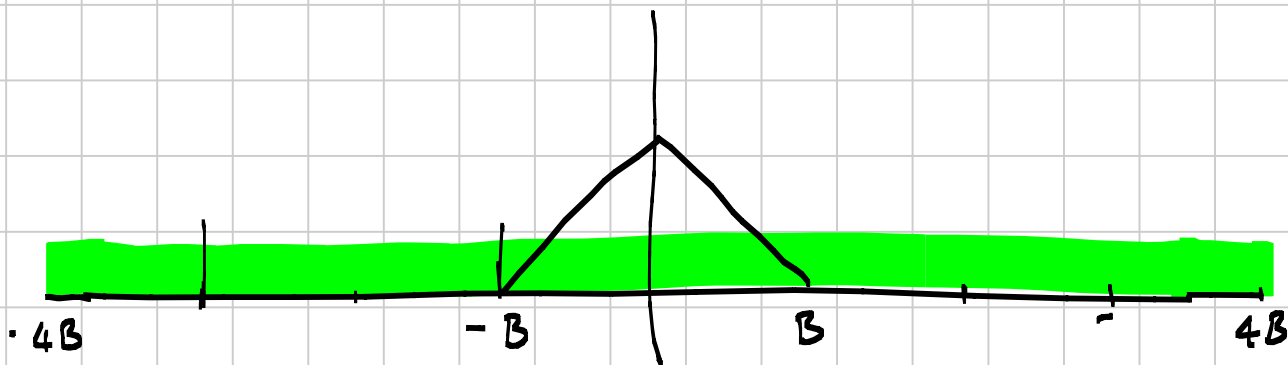
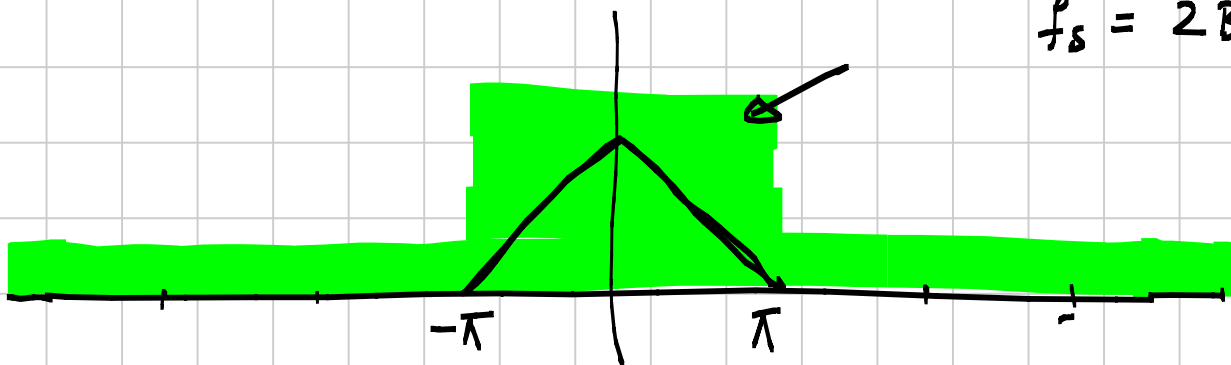
$$\sum_{k=-\infty}^{\infty} x(kT) \delta(t - kT) \leftarrow$$



* Signal bandwidth : B

f_s = sampling rate $\geq 2B$

$$f_s = 2B \rightarrow 2\pi$$



VLSI Data Conversion Circuits: Lecture 2

Note Title

03-12-2010

$$\begin{array}{ccc}
 x(t) & \xrightarrow{T} & x(kT) \\
 \uparrow & & \uparrow \\
 X_c(f) & & X_d(e^{j\omega}) = \sum_k x(kT) e^{-j\omega k}
 \end{array}$$

$$X_d(e^{j\omega}) \rightarrow \frac{1}{T} \sum_k X_c\left(f - \frac{k}{T}\right)$$

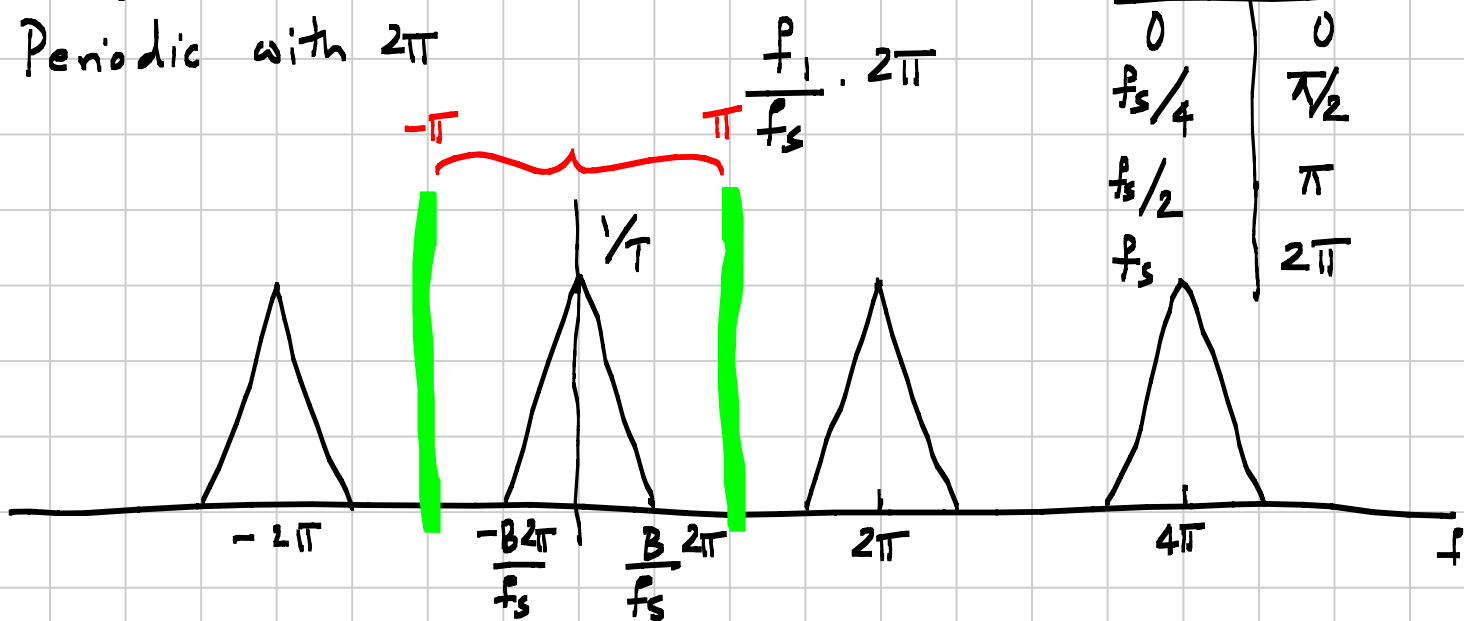
$$2\pi f T \rightarrow \omega$$

$$X_d(e^{j\omega}) = \frac{1}{T} \sum_k X_c\left(\frac{\omega}{T 2\pi} - \frac{k}{T}\right)$$

$$\frac{1}{T} \rightarrow f_s$$

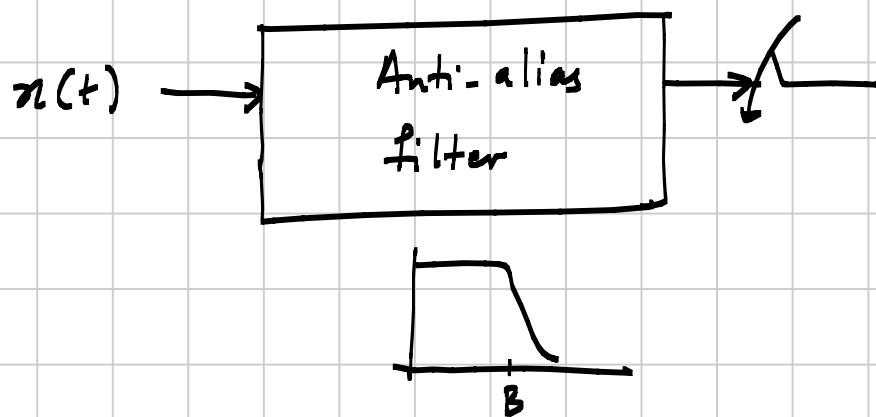
$$X_d(e^{j\omega}) = \frac{1}{T} \sum_k X_c\left(\frac{f_s}{2\pi} \{ \omega - 2\pi k \} \right)$$

Periodic with 2π

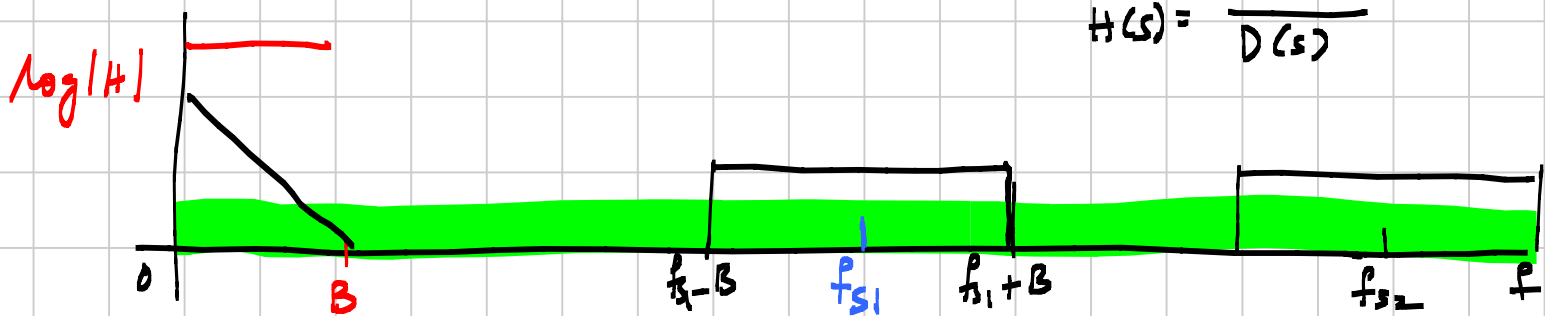
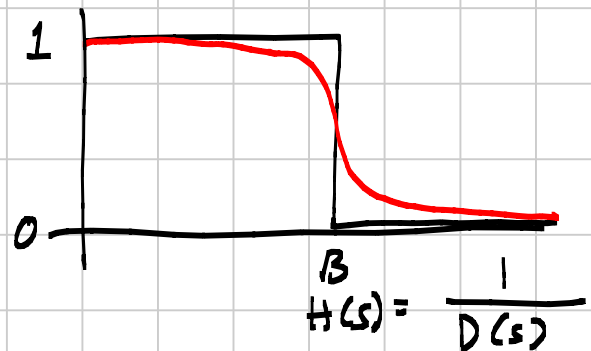


$$\left\{ \begin{array}{l} f_1 \rightarrow 2\pi \frac{f_1}{f_s} \\ f_1 + f_s \rightarrow 2\pi \left(\frac{f_1 + f_s}{f_s} \right) \rightarrow 2\pi \frac{f_1}{f_s} \end{array} \right.$$

$$f_1 + k f_s \rightarrow \frac{2\pi f_1}{f_s}$$



ideal A.A filter



- * Choice of sampling frequency relative to the Nyquist frequency ($2B$) has implications on Anti Alias filter.

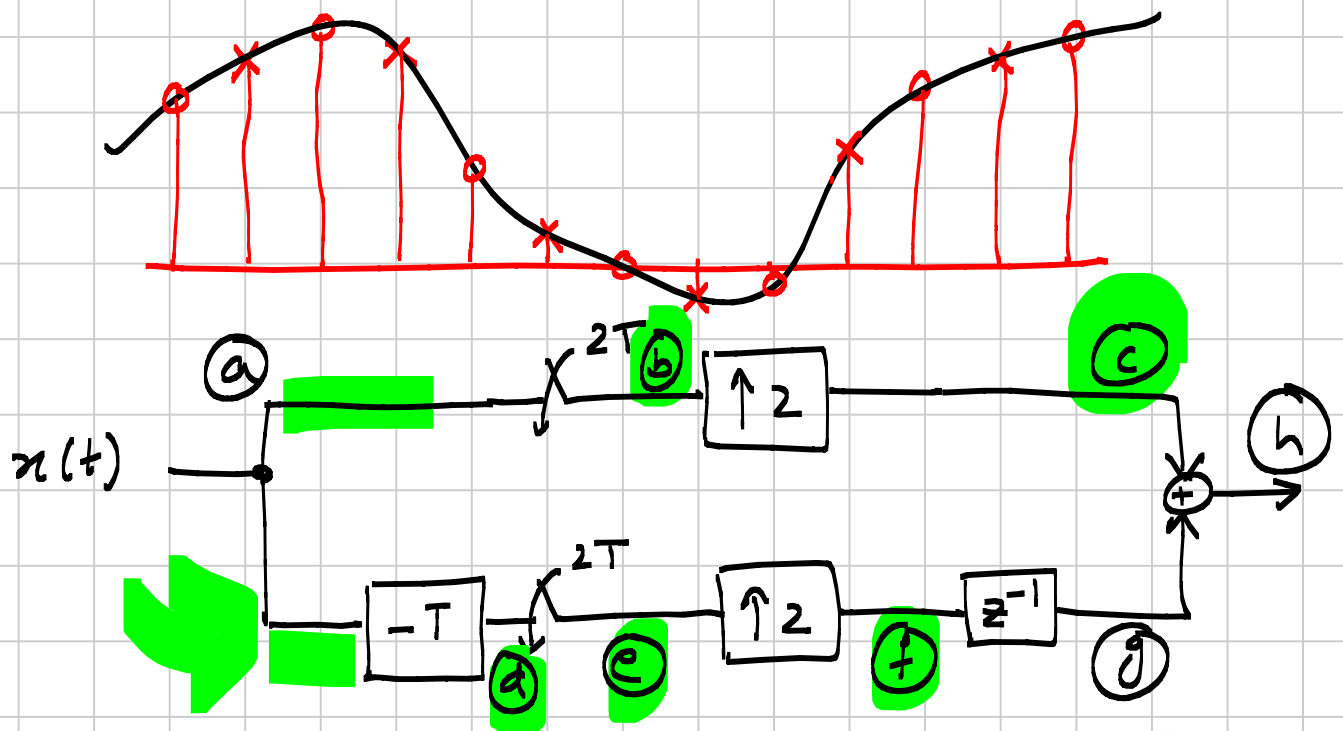
$$\frac{f_s}{2B} \rightarrow \text{Over Sampling Ratio (OSR)}$$

- * High OSR $\rightarrow$ AA filter need not be very sharp

Ex: $B = 24 \text{ kHz}$ $Nyq \rightarrow 48 \text{ kHz}$

$$f_s = 6.144 \text{ MHz} \rightarrow \text{OSR} = 128$$

Time-interleaving



$$(h) \rightarrow X_d(e^{j\omega}) = \frac{1}{T} \sum_k X_c\left(\frac{f_s}{2\pi} \left\{ \omega - 2\pi k \right\}\right)$$

$$(a) \rightarrow X_c(f) \quad (b) \rightarrow \frac{1}{2T} \sum_k X_c\left(\frac{f_s}{2\pi} \left\{ \frac{\omega}{2} - \pi k \right\}\right)$$

$$(c) \rightarrow \frac{1}{2T} \sum_k X_c\left(\frac{f_s}{2\pi} \left\{ \omega - \pi k \right\}\right)$$

$$(d) \rightarrow X_c(f) e^{j2\pi f T}$$

$$(e) \rightarrow \frac{1}{2T} \sum_k X_c\left(\frac{f_s}{2\pi} \left\{ \frac{\omega}{2} - \pi k \right\}\right) e^{j2\pi \left(\frac{\omega}{2} - \frac{k f_s}{2}\right) T}$$

$$\frac{1}{2T} \sum_k X_c\left(\frac{f_s}{2\pi} \left\{ \frac{\omega}{2} - \pi k \right\}\right) e^{j\left(\frac{\omega}{2} - k\pi\right)}$$

$$\textcircled{p} \quad \frac{1}{2T} \sum_k X_c \left(\frac{f_s}{2\pi} \{ \omega - \pi k \} \right) e^{j(\omega - k\pi)}$$

$$\textcircled{p} \quad \frac{1}{2T} \sum_k X_c \left(\underbrace{\frac{f_s}{2\pi} \{ \omega - \pi k \}} \right) e^{-jk\pi}$$

$$\textcircled{c} \rightarrow \frac{1}{2T} \sum_k X_c \left(\underbrace{\frac{f_s}{2\pi} \{ \omega - \pi k \}} \right)$$

$$k=0 \Rightarrow \frac{1}{T} X_c \left(\frac{f_s}{2\pi} \omega \right)$$

$$k=1 \Rightarrow \textcircled{0}$$

$$\textcircled{h} \quad \frac{1}{T} \sum_k X_c \left(\frac{f_s}{2\pi} \{ \omega - 2\pi k \} \right)$$

VLSI Data Conversion Circuits : Lecture 3

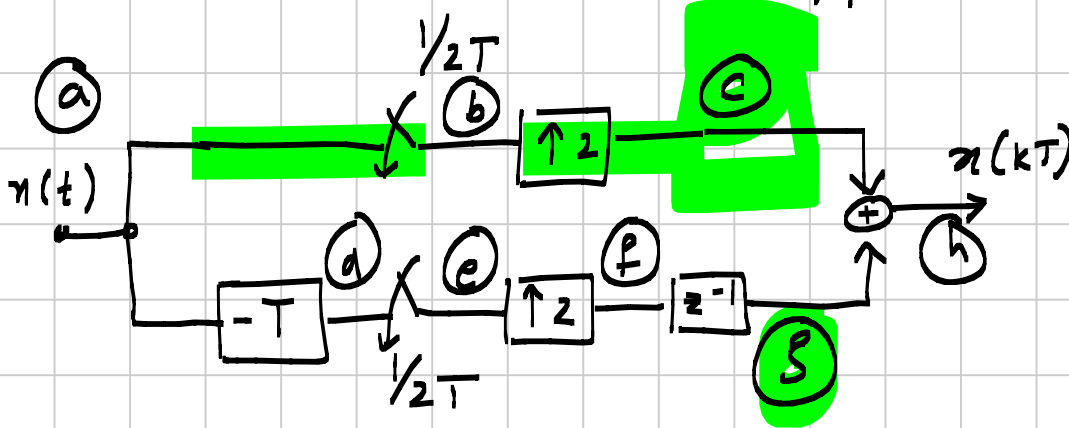
Note Title

07-12-2010



Full rate sampling

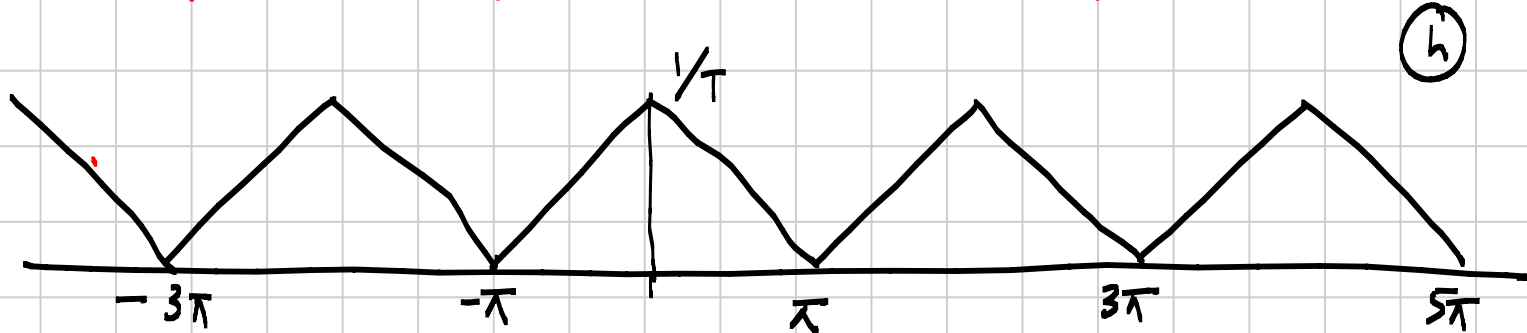
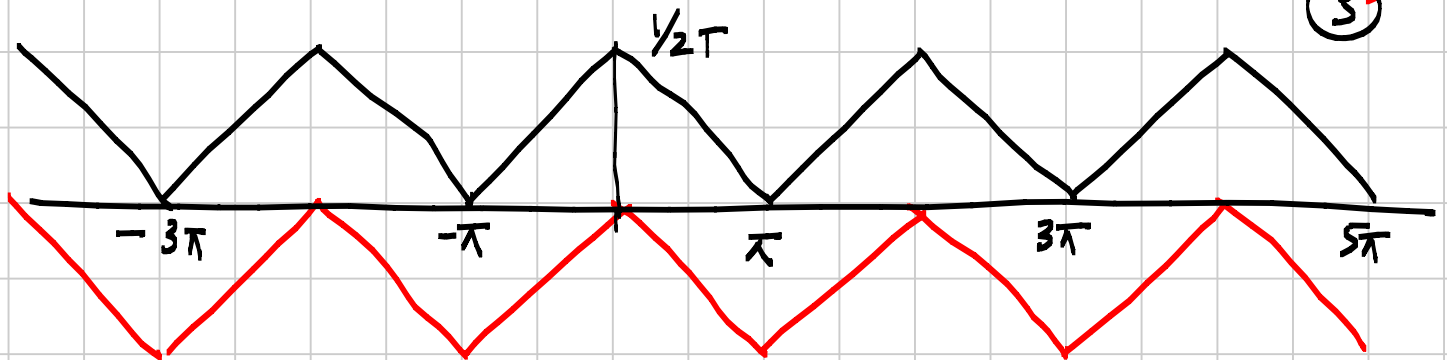
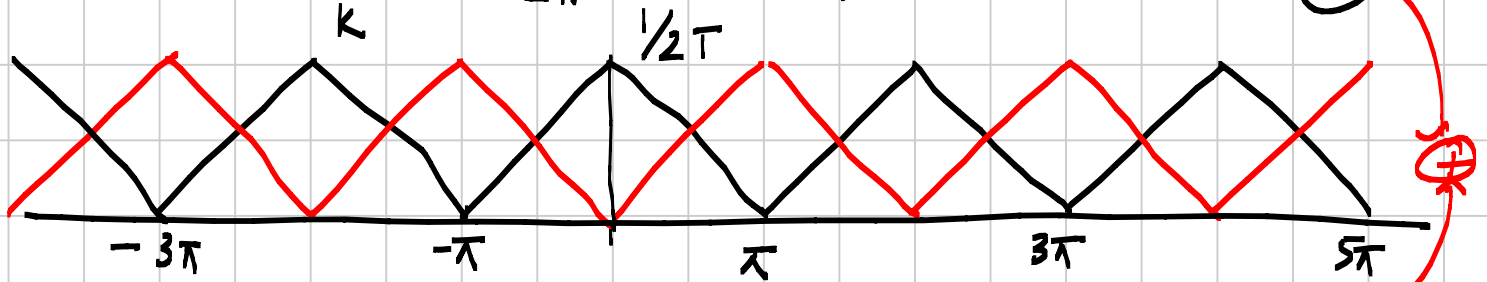
$$1/T \rightarrow f_s$$

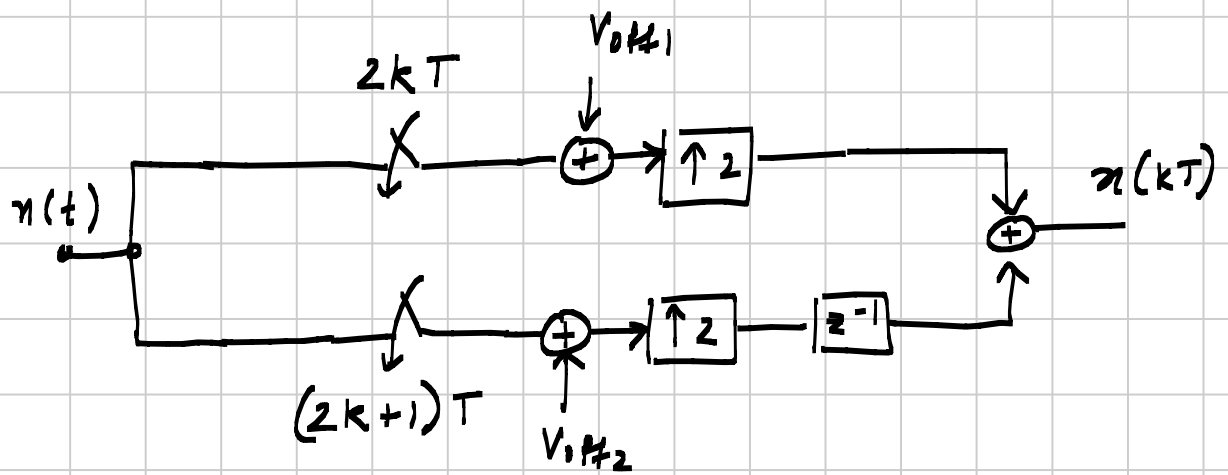


Time-interleaved sampling

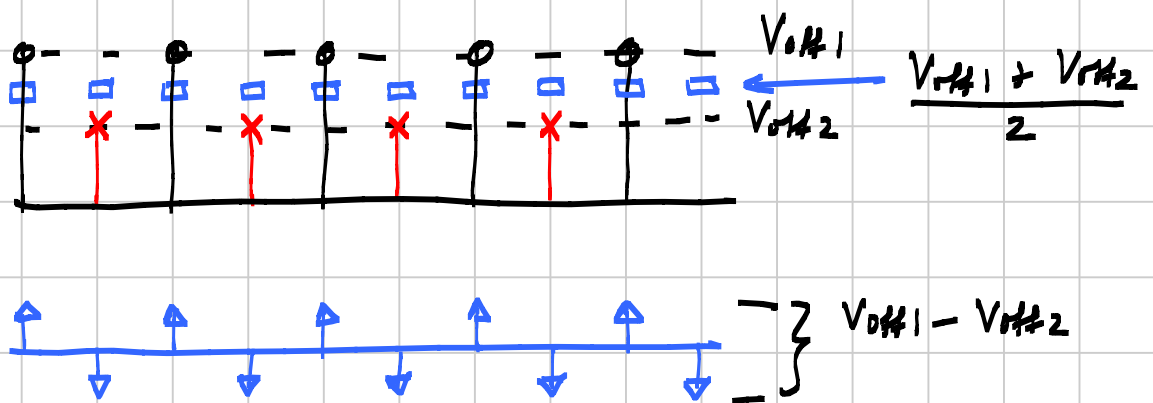
(c)
$$\frac{1}{2T} \sum_k X\left(\frac{f_s}{2\pi} \{\omega - \pi k\}\right)$$

(g)
$$\frac{1}{2T} \sum_k X\left(\frac{f_s}{2\pi} \{\omega - \pi k\}\right) e^{-jk\pi}$$



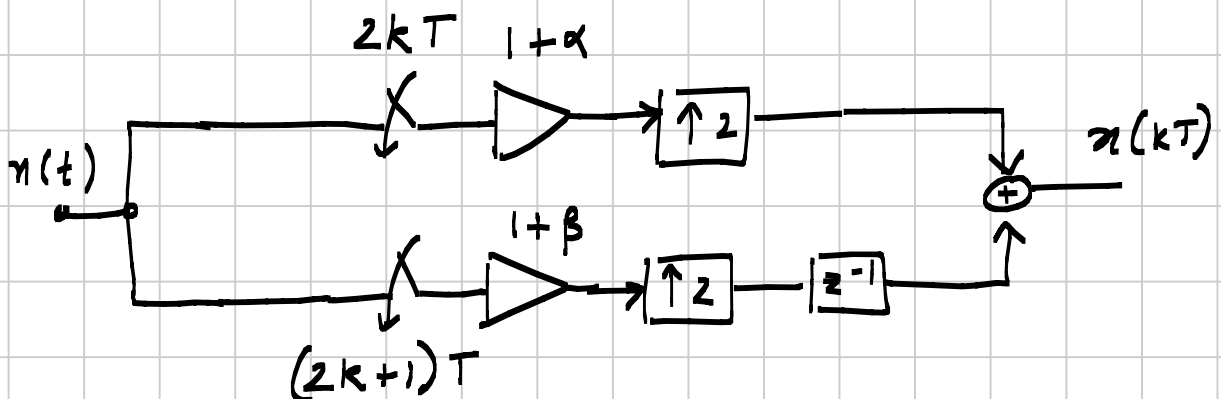


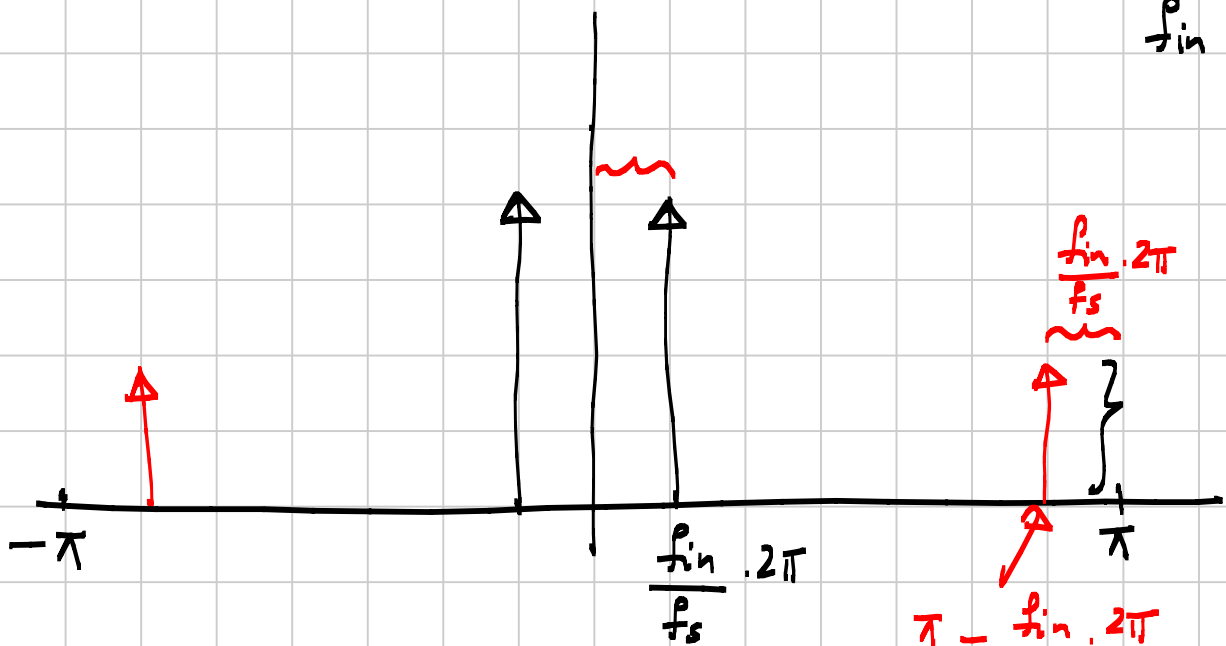
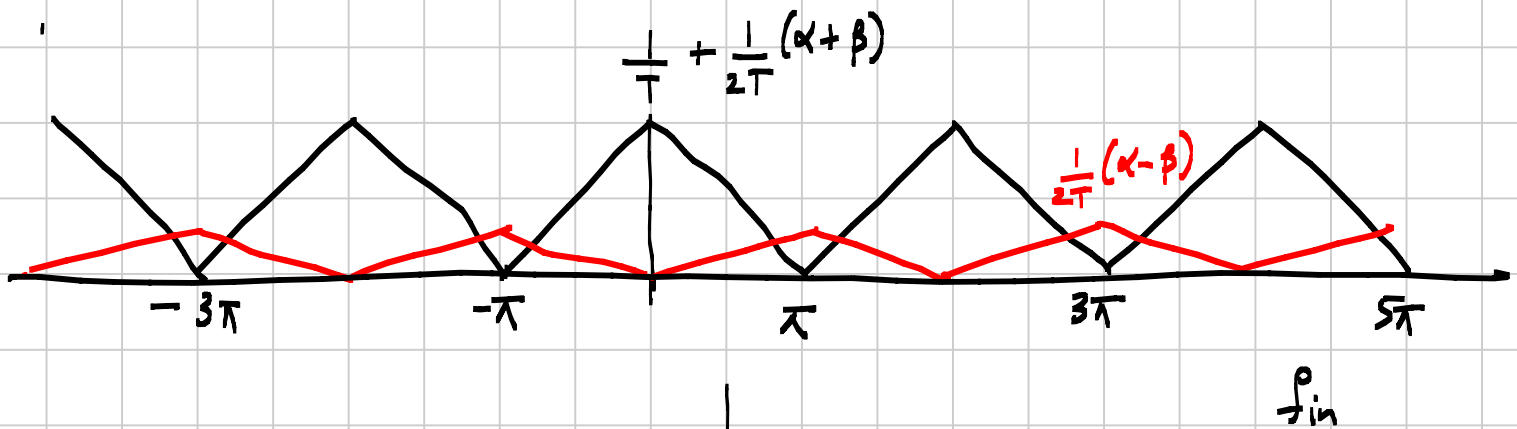
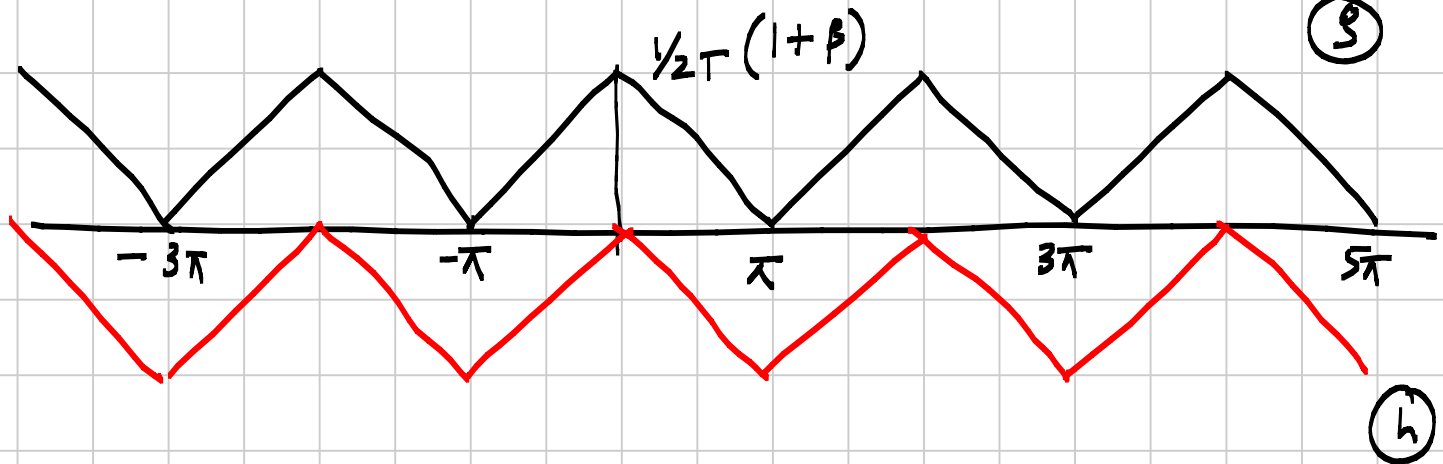
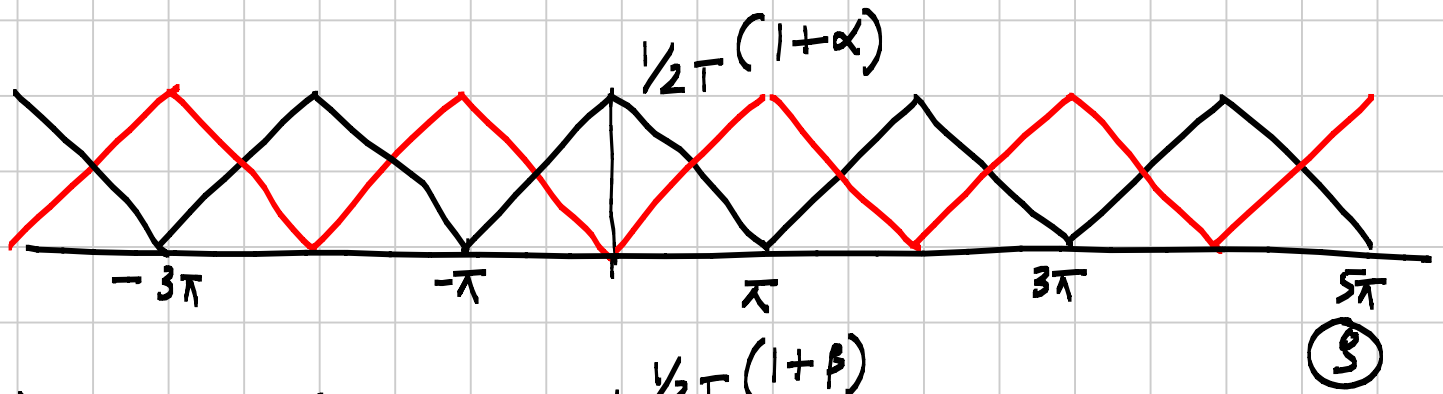
1) Non-idealities : Offset



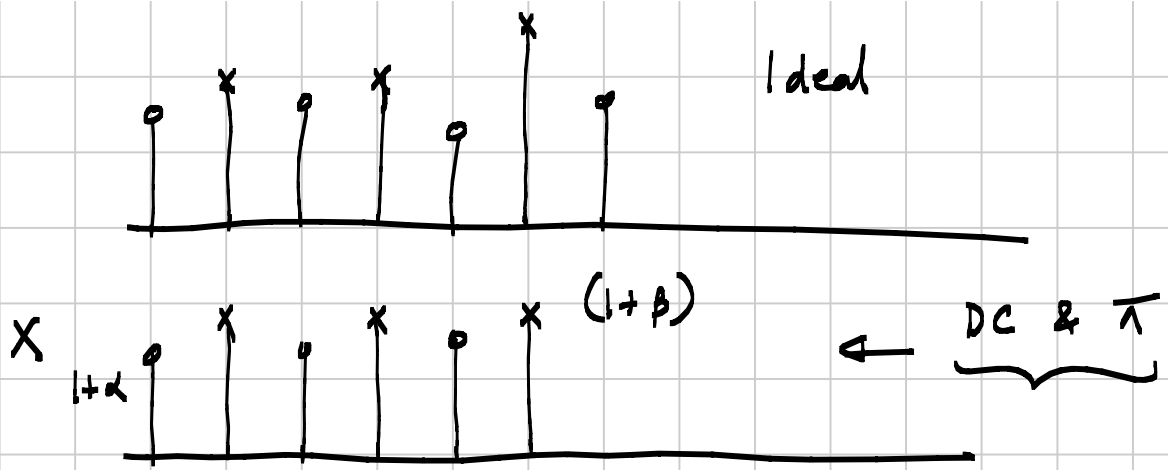
→ Causes offset & tone @ $\omega = \pi$ ($f_n = f_s/2$)

2) Non-ideality : Gain Error





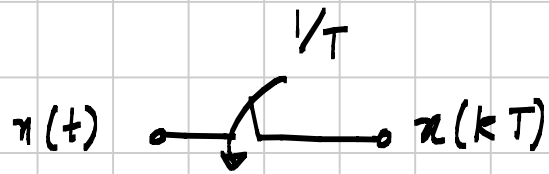
$In \text{ c.T} \rightarrow \frac{f_s}{2} - f_{in}$



VLSI Data Conversion Circuits : Lecture 4

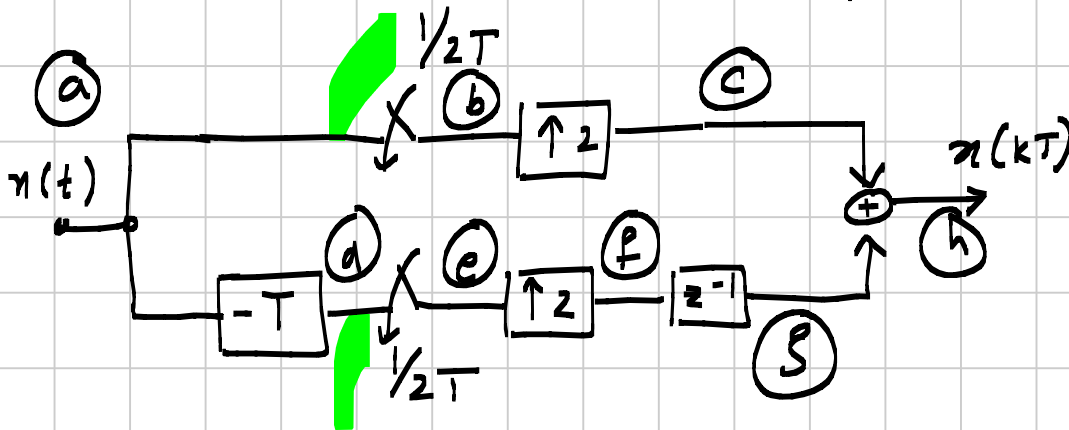
Note Title

07-12-2010



Full rate sampling

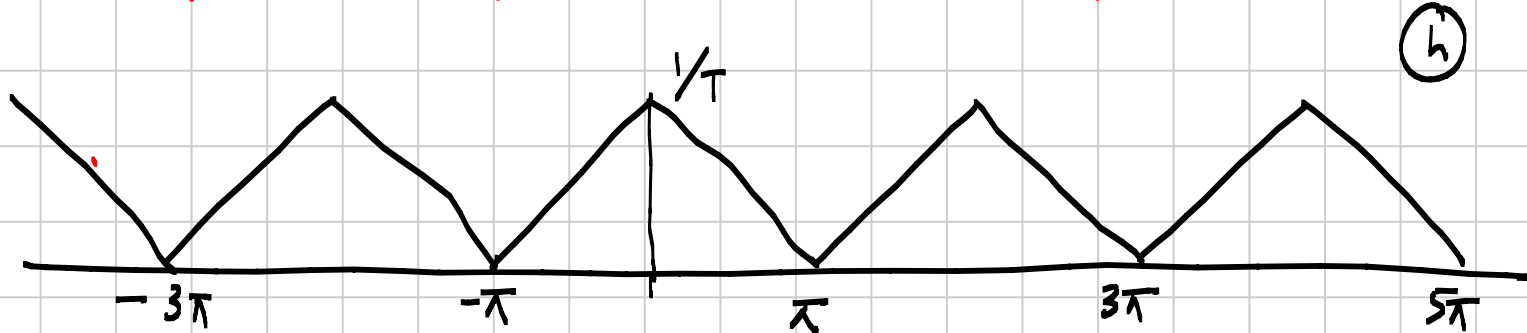
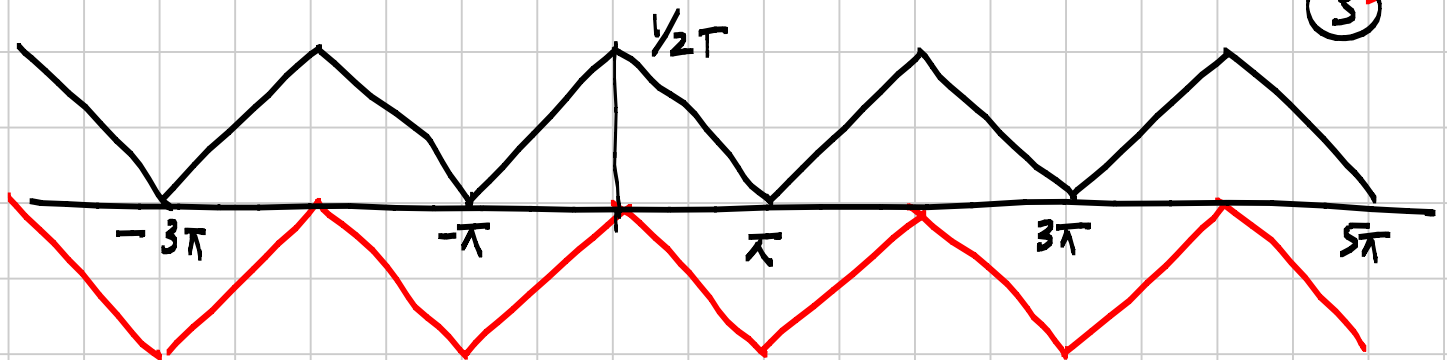
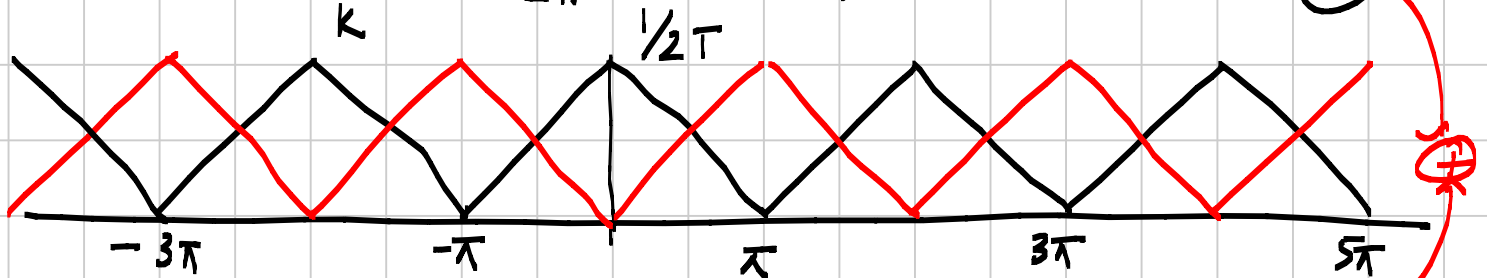
$$1/T \rightarrow f_s$$



Time-interleaved sampling

$$(c) \quad \frac{1}{2T} \sum_k X\left(\frac{f_s}{2\pi} \{\omega - \pi k\}\right)$$

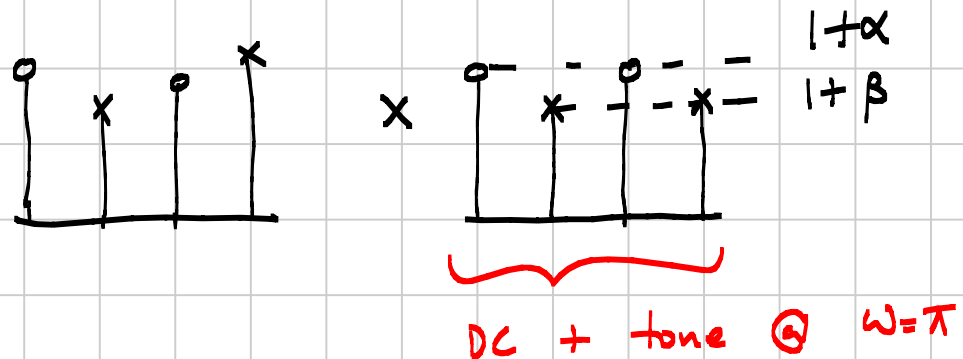
$$(g) \quad \frac{1}{2T} \sum_k X\left(\frac{f_s}{2\pi} \{\omega - \pi k\}\right) e^{-jk\pi}$$



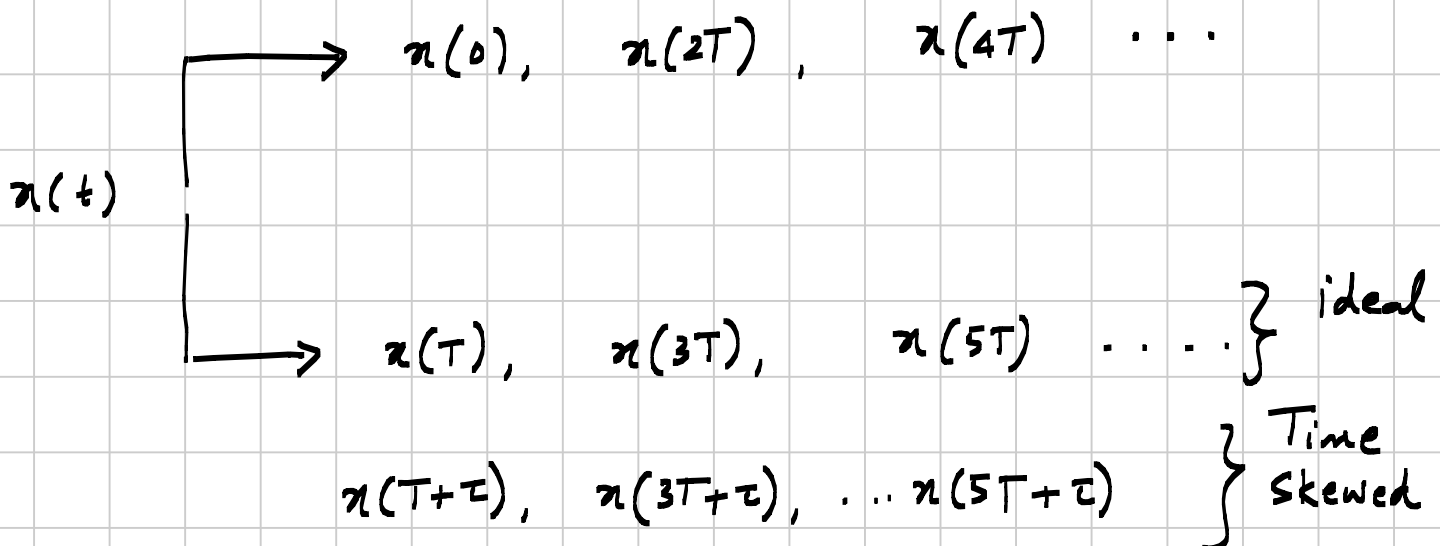
Non idealities

* Offset $\rightarrow$ tone @ $f_s/2$ (or $\omega = \pi$) and a DC offset

* Gain mismatch $\rightarrow$



Ideally



Actual

$x(0) \quad x(T+\tau) \quad x(2T) \quad x(3T+\tau) \quad x(4T) \quad \dots$

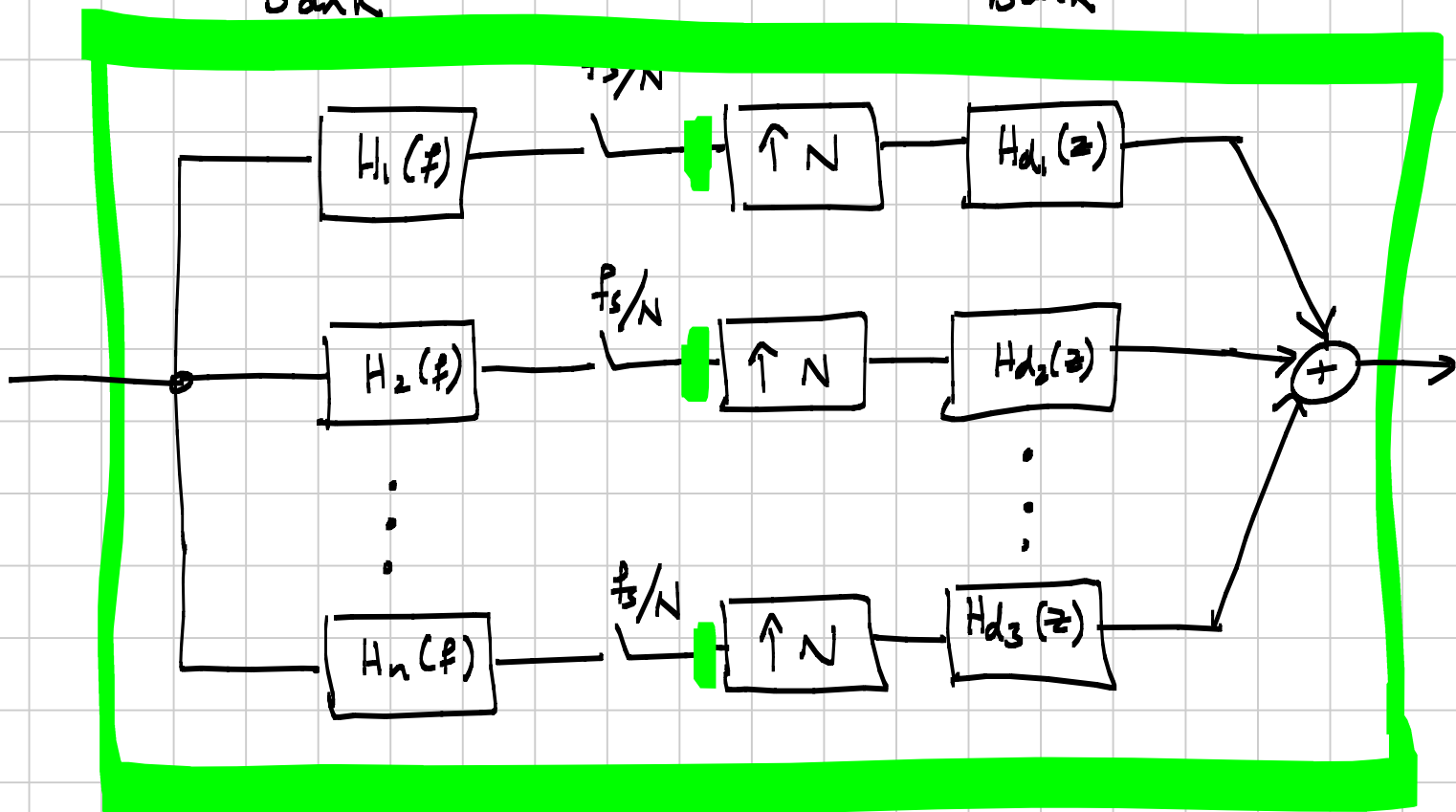
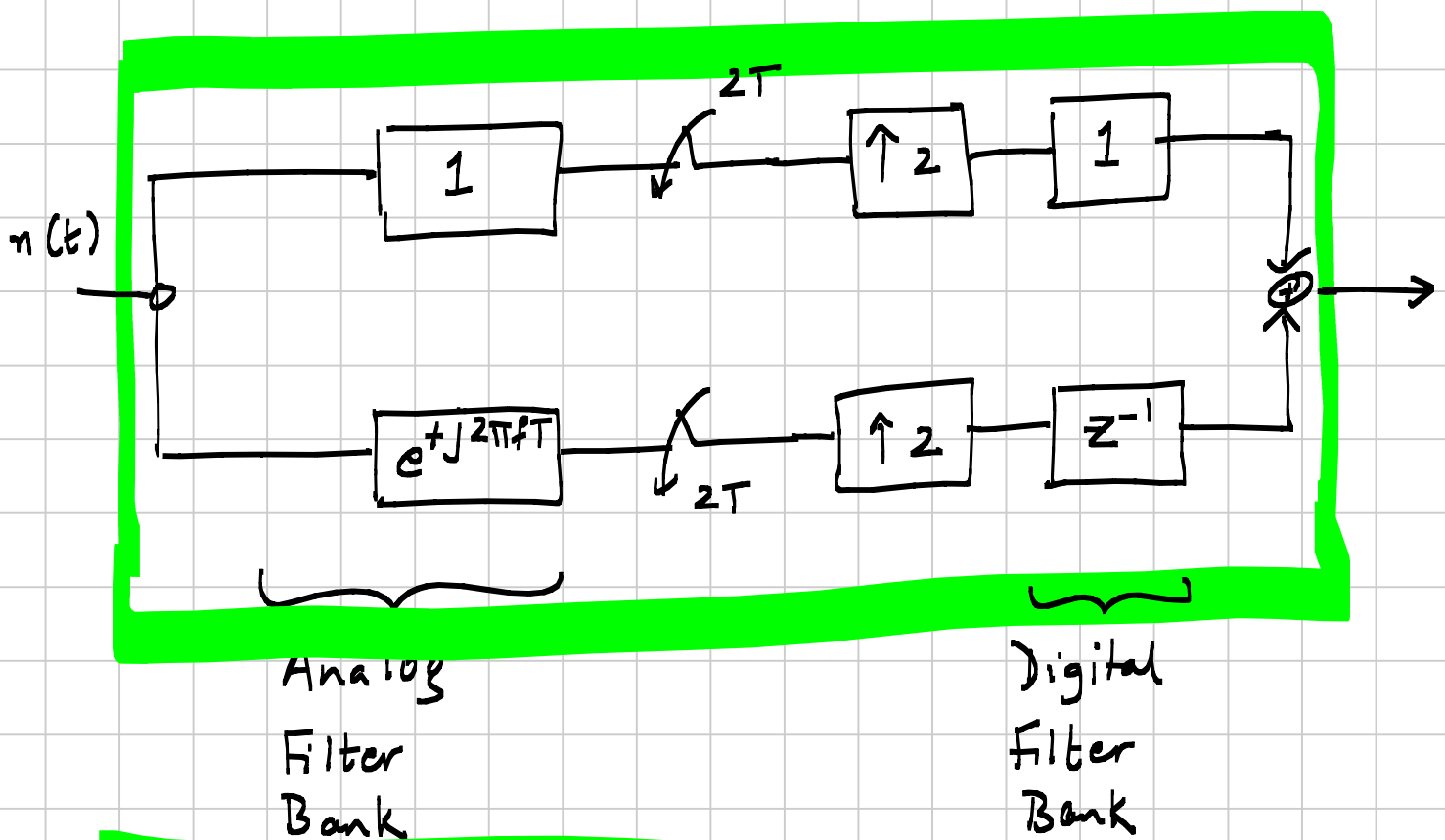
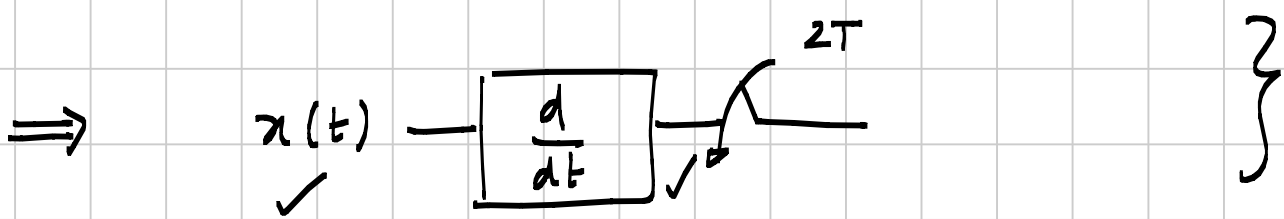
Ideal

$x(0) \quad x(T) \quad x(2T) \quad x(3T) \quad x(4T) \quad \dots$

Error

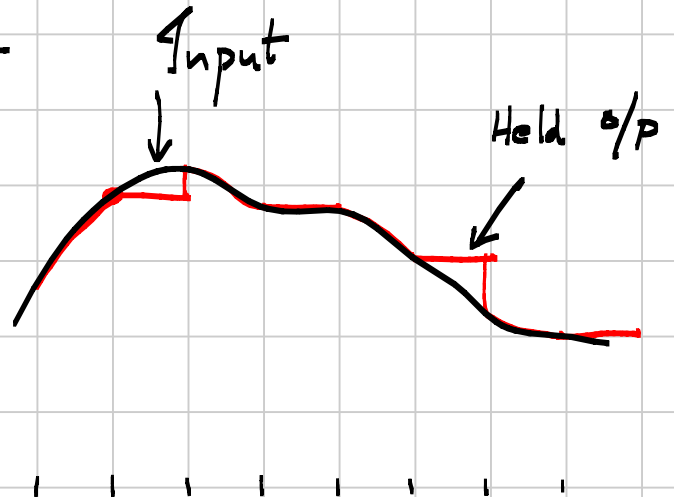
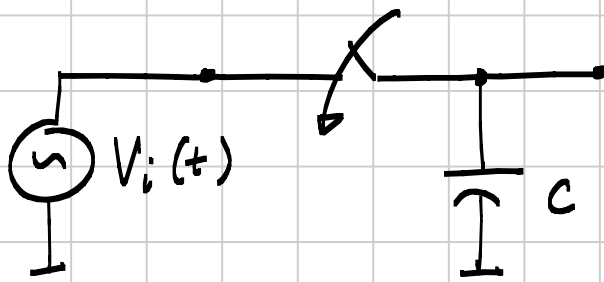
$0 \quad \tau x'(T) \quad 0 \quad \tau x'(3T) \quad 0 \quad \dots$

$$x(T+\tau) \approx x(T) + \tau \left. \frac{dx(t)}{dt} \right|_{t=T}$$



Multi channel Sampling

Sampling Circuits

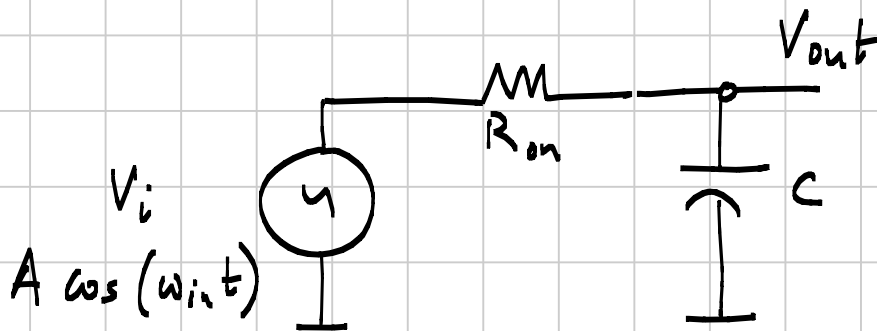


Track & Hold
1/2 1/2



Nonidealities :-

(a) On-resistance



$$\frac{A \cos(\omega_{in} t - \phi)}{\sqrt{1 + \omega_{in}^2 R_{on}^2 C^2}}$$

$$\phi = \tan^{-1}(\omega_{in} R_{on} C)$$

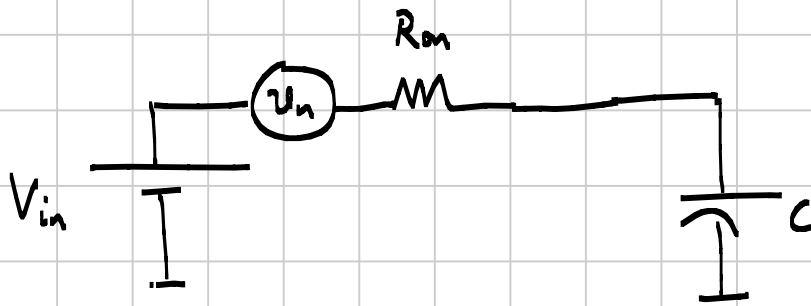
$$\omega_{in} R_{on} C \ll 1$$

$$R_{on} C \ll \frac{1}{\omega_{in}}$$

$$\rightarrow R C \rightarrow \tau$$

$$\rightarrow \frac{R}{2} 2C \rightarrow \tau$$

$$\rightarrow 10 R \frac{C}{10} \rightarrow \tau$$

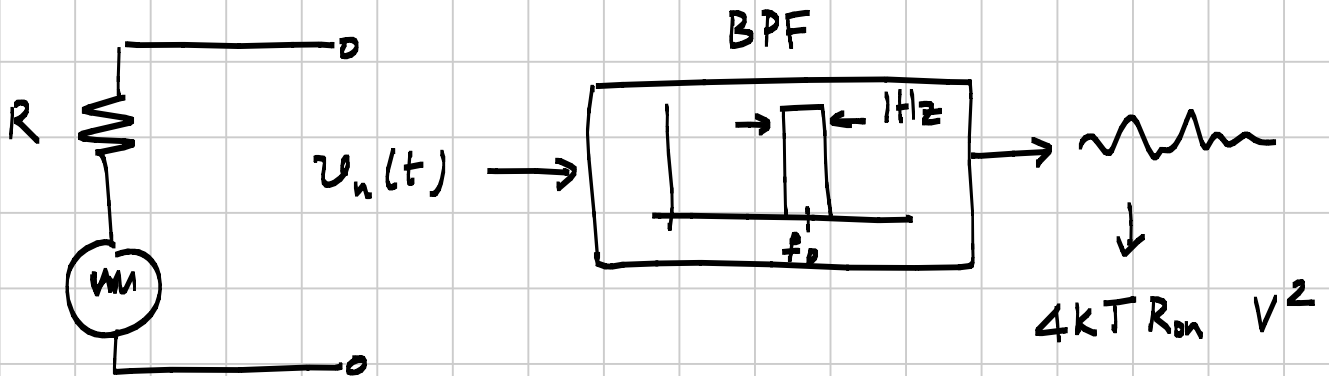


$v_n \rightarrow$ Zero mean

$$S_v(f) \rightarrow 4kT R_{on} \quad V^2/Hz$$

k Boltzmann's const

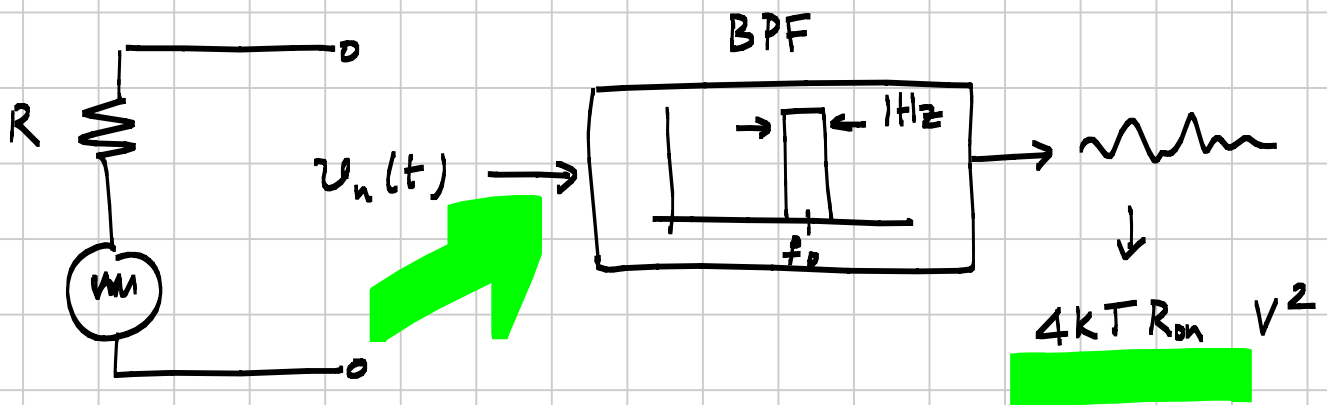
$T \rightarrow$ Absolute Temp (K)



VLSI Data Conversion Circuits: Lecture 5

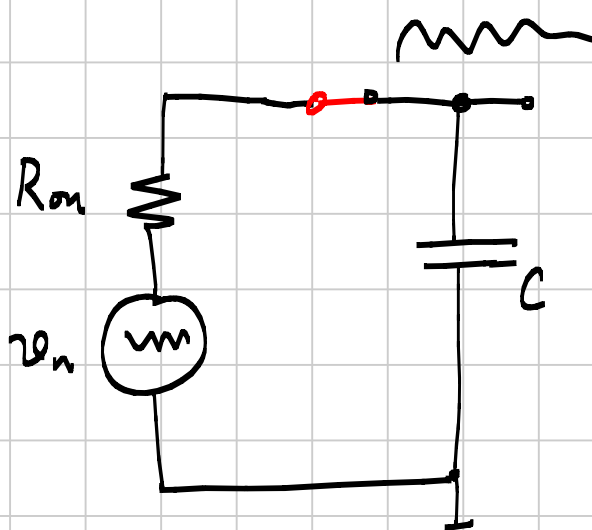
Note Title

09-12-2010



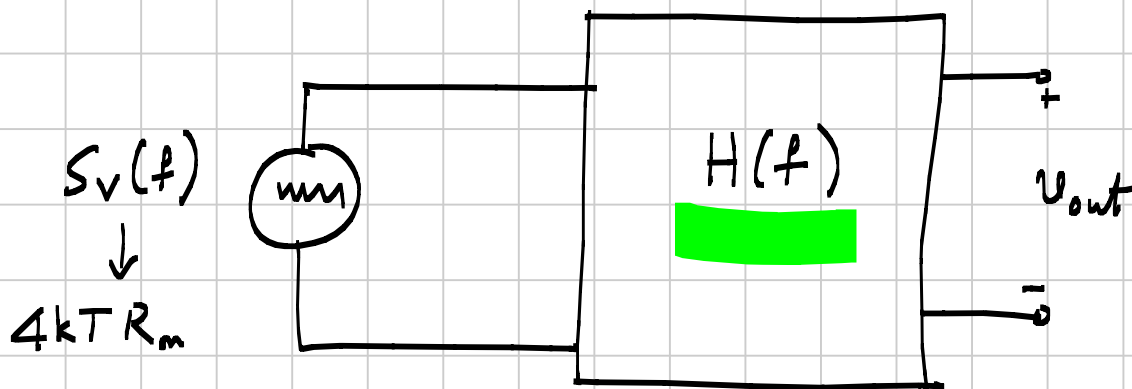
$$S_v(f) = 4kTR_{on} \frac{V^2}{\text{Hz}}$$

"White" Noise



Track & Hold
Input = 0

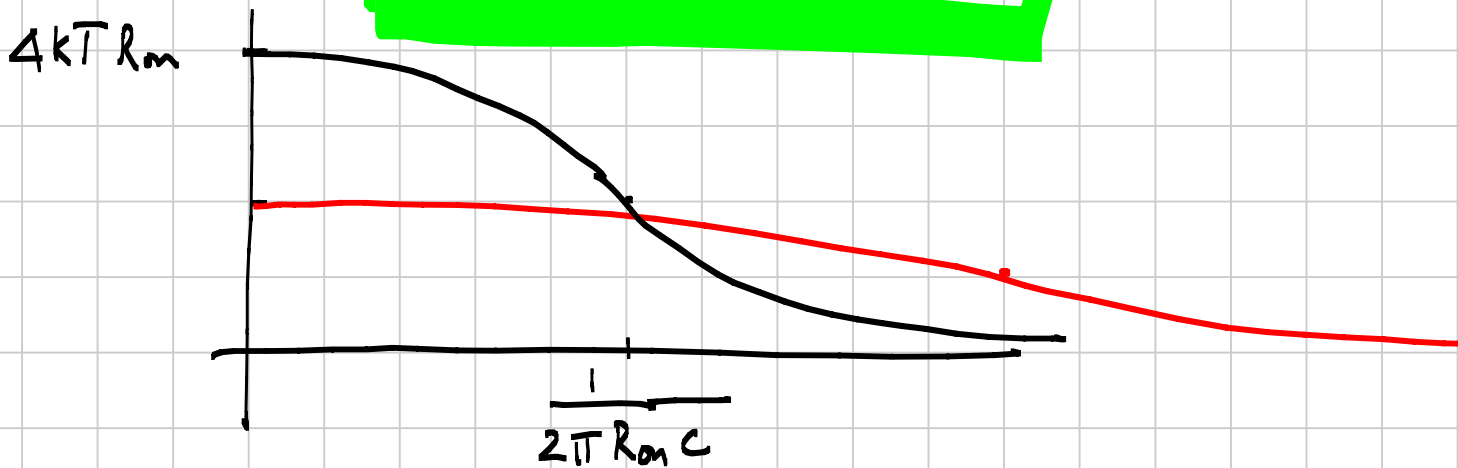
Held voltage has a noise component (mean = 0)



$$S_{v_{out}}(f) = S_v(f) |H(f)|^2$$

$$S_{vout}(f) = 4kT R_{on} \frac{1}{1 + 4\pi^2 f^2 R_{on}^2 C^2}$$

$$\frac{V^2}{Hz}$$



$$\overline{v_{out}^2} = \int_0^{\infty} S_{vout}(f) df$$

$$= 4kT R_{on} \int_0^{\infty} \frac{1}{1 + 4\pi^2 f^2 R_{on}^2 C^2} df$$

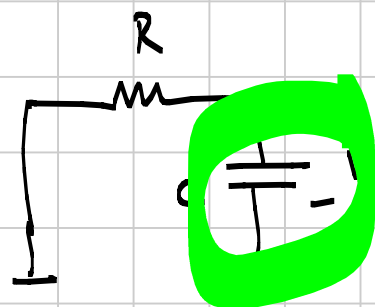
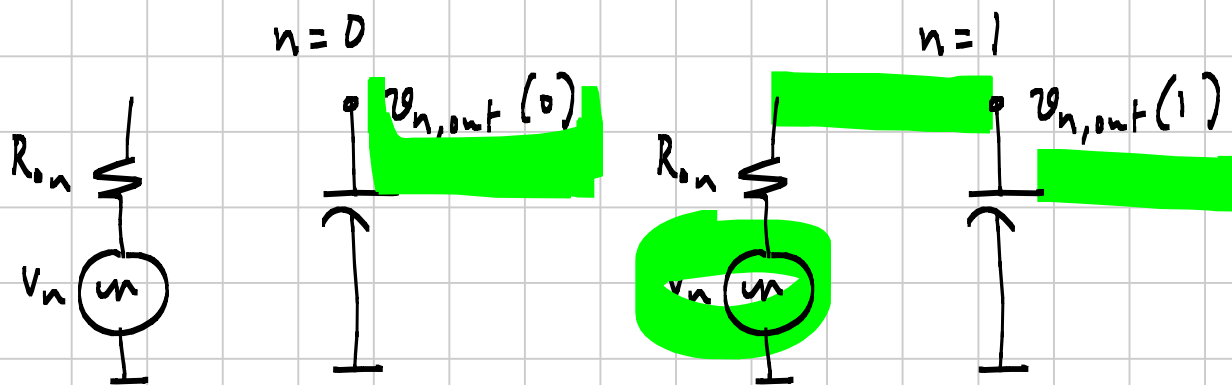
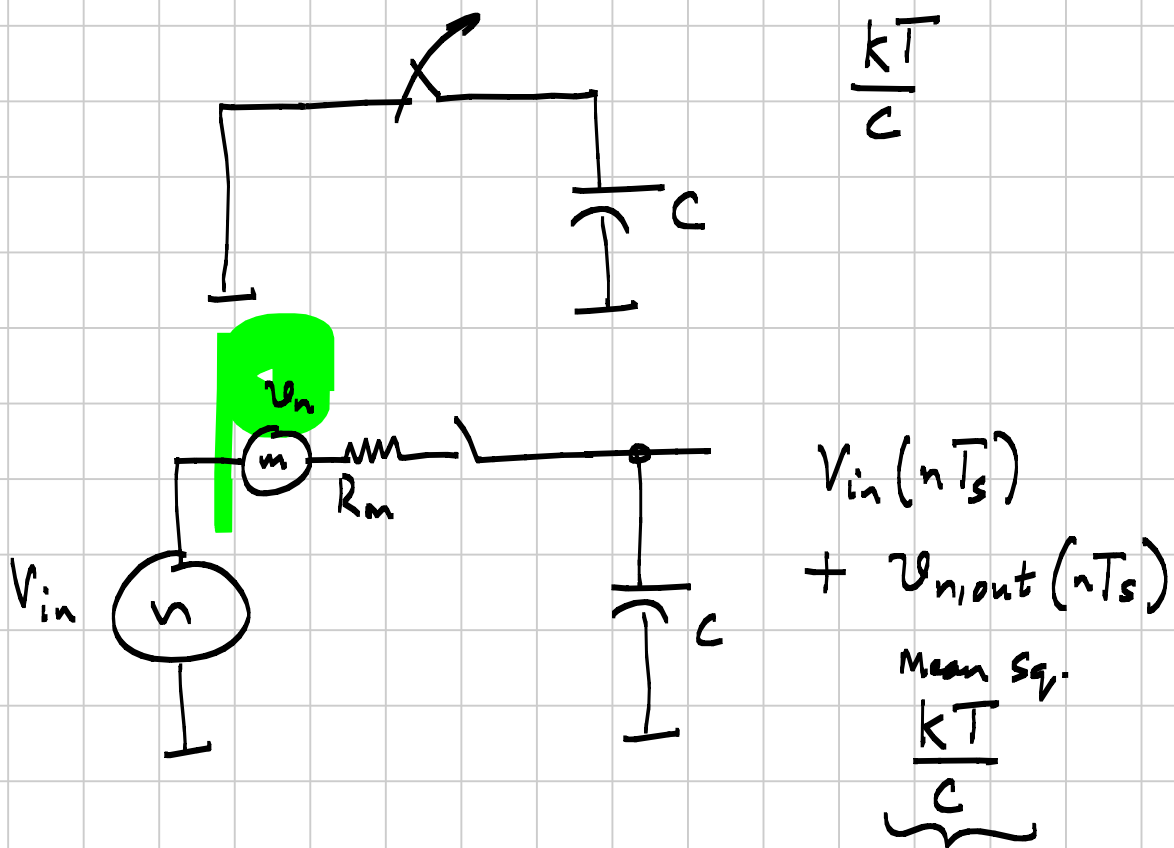
Choose $2\pi f R_{on} C = u$

$$\overline{v_{out}^2} = 4kT R_{on} \int_0^{\infty} \frac{du}{2\pi R_{on} C (1 + u^2)}$$

$$= \frac{4kT}{2\pi C} \int_0^{\infty} \frac{du}{1 + u^2} = \frac{4kT}{2\pi C} \left[\tan^{-1} u \right]_0^{\infty}$$

$\frac{\pi}{2}$

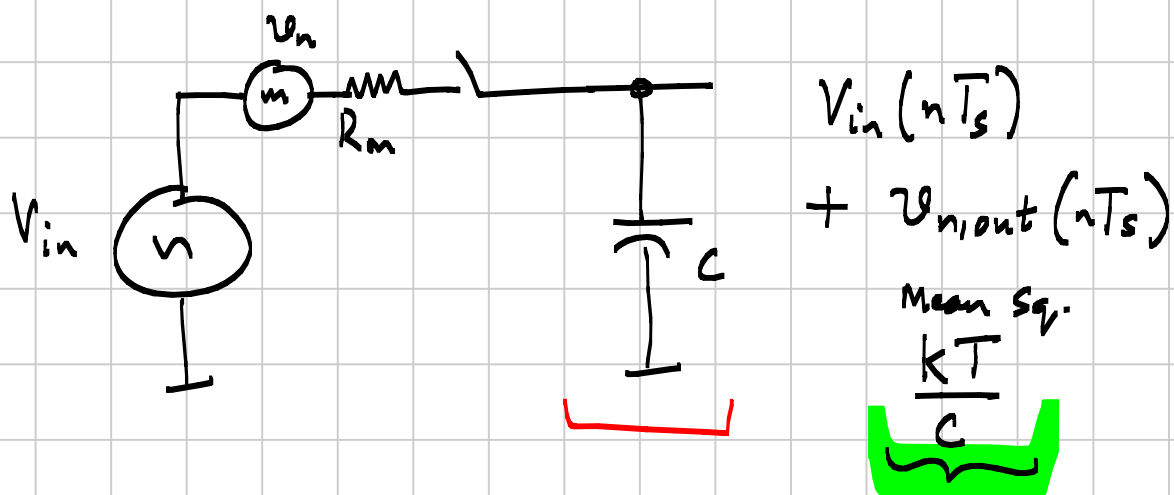
$$\overline{v_{out}^2} = \frac{kT}{C}$$



VLSI Data Conversion Circuits : Lecture 6

Note Title

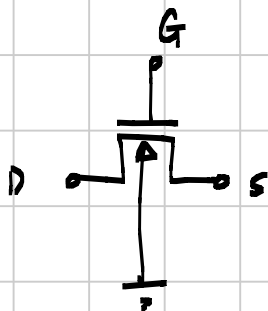
09-12-2010



$\sqrt{\frac{KT}{C}}$ = RMS thermal noise < Step size

Peak signal Amplitude = A

$SNR = \frac{A^2 C}{2 KT}$



n-well CMOS processes

→ Triode (Closed Switch)

→ Off (open switch)

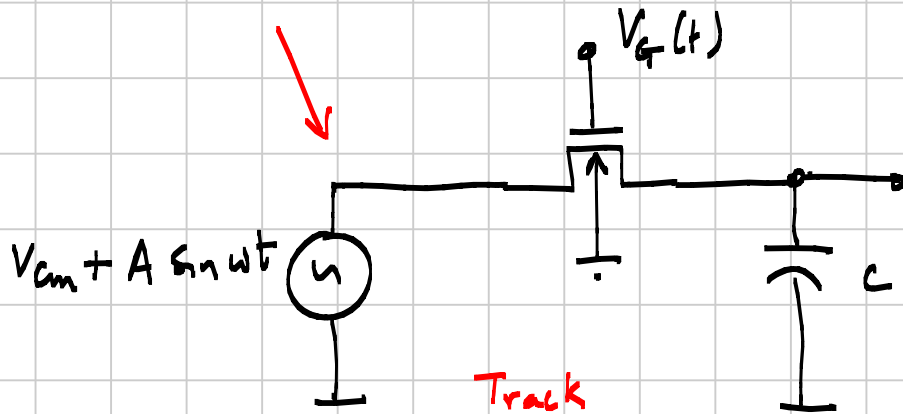
Triode : $V_{GS} > V_T$, $V_{DS} \leq V_{GS} - V_T$

$V_T = V_{T0} + \gamma (\sqrt{V_{SB} + 2\phi_0} - \sqrt{2\phi_0})$

$$I_D = \mu_n C_{ox} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right)$$

$$\alpha \rightarrow 1.1 \sim 1.2$$

$$R_{SW} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}$$

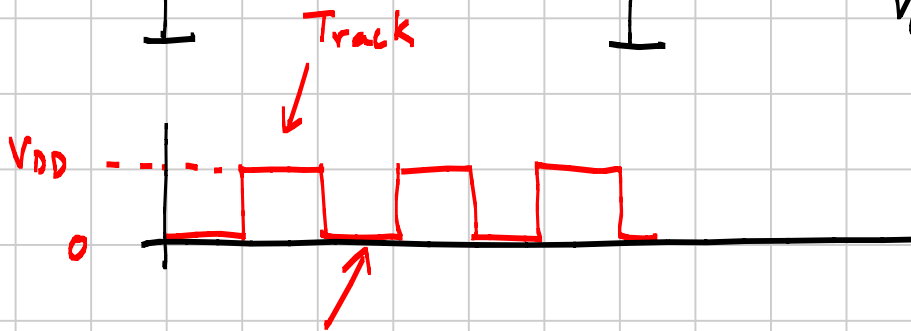


$$0 \text{ \& } V_{DD}$$

$$V_{cm} \rightarrow \frac{V_{DD}}{2}$$

$$V_G \rightarrow V_{DD} \quad \left\{ \begin{array}{l} \text{Track} \\ \text{Hold} \end{array} \right.$$

$$V_G \rightarrow 0$$

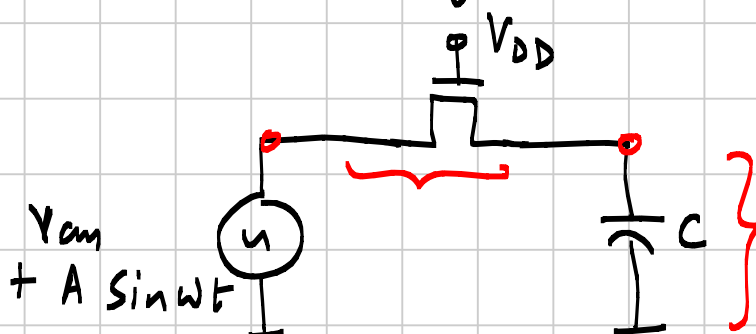


$$V_G = V_{DD} \quad \left\{ \begin{array}{l} \text{Track} \\ \text{Hold} \end{array} \right.$$

$$V_S = V_{cm} + A \sin wt$$

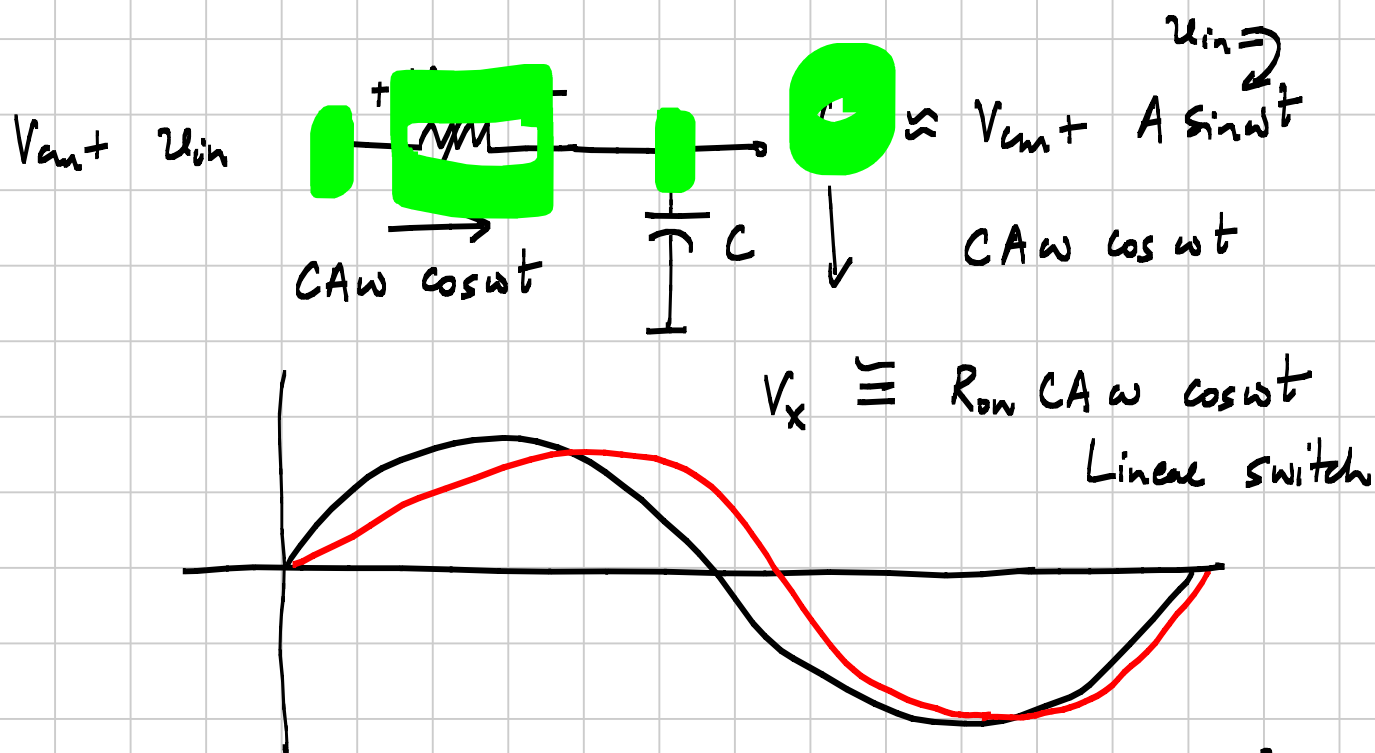
$$V_{GS} = V_{DD} - \{ V_{cm} + A \sin wt \}$$

$$= \frac{V_{DD}}{2} - A \sin wt$$



$$R_{on} = \frac{1}{\mu_n \epsilon_{ox} \frac{W}{L} (V_{GS} - V_T)} \leftarrow$$

Resistance of the switch depends on input $\rightarrow$ Nonlinearity $\rightarrow$ Distortion.



$$R(V_{in}) = R_{on} + r_1 V_{in} + r_2 V_{in}^2$$

Voltage drop across the switch

$$\begin{aligned} &\approx C \frac{dV_{in}}{dt} \left\{ R_{on} + r_1 V_{in} + r_2 V_{in}^2 \right\} \\ V_{in} &= A \sin \omega t \\ &\approx CA\omega \cos(\omega t) \left\{ R_{on} + r_1 A \sin \omega t + r_2 A^2 \sin^2 \omega t \right\} \\ &\approx CA\omega R_{on} \cos(\omega t) \end{aligned}$$

$$+ \frac{CA^2 r_1 \omega_{in}}{2} \sin(2\omega_{in} t)$$

$$+ \frac{CA^3 r_2 \omega_{in}}{2} \cos(\omega_{in} t) \{1 - \cos(2\omega_{in} t)\}$$

$$\underbrace{\hspace{15em}}$$

$$\frac{CA^3 r_2 \omega_{in}}{2} L(\text{redacted}) - \frac{CA^3 r_2 \omega_{in}}{4} \{ \cos(3\omega_{in} t) + \cos(\omega_{in} t) \}$$

$$\approx CA \omega_{in} R_{on} \cos(\omega_{in} t)$$

$$+ \frac{CA^2 r_1 \omega_{in}}{2} \sin(2\omega_{in} t)$$

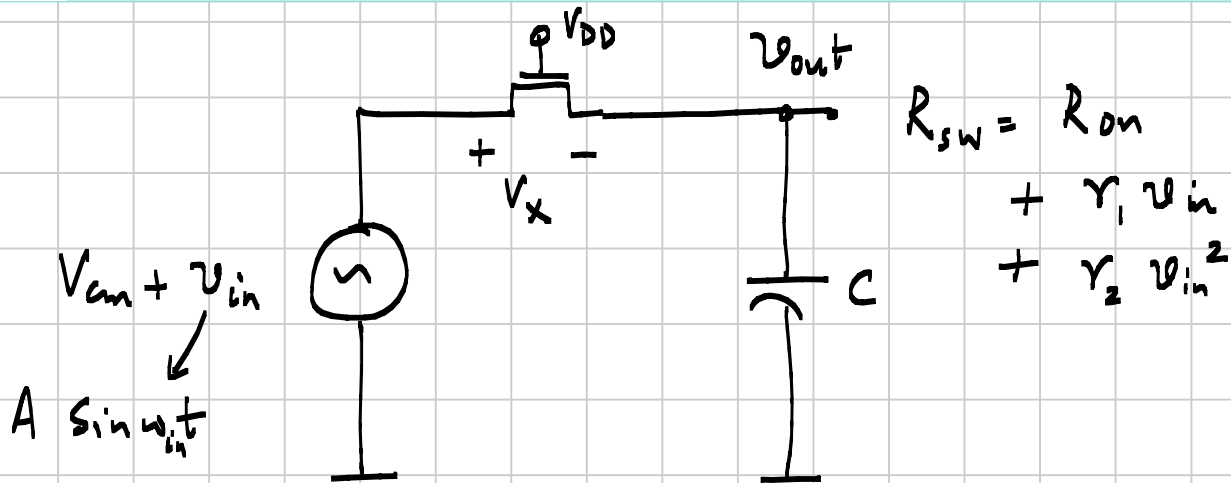
$$- \frac{CA^3 r_2 \omega_{in}}{4} \cos(3\omega_{in} t)$$

} Drop across the switch

VLSI Data Conversion Circuits : Lecture 7

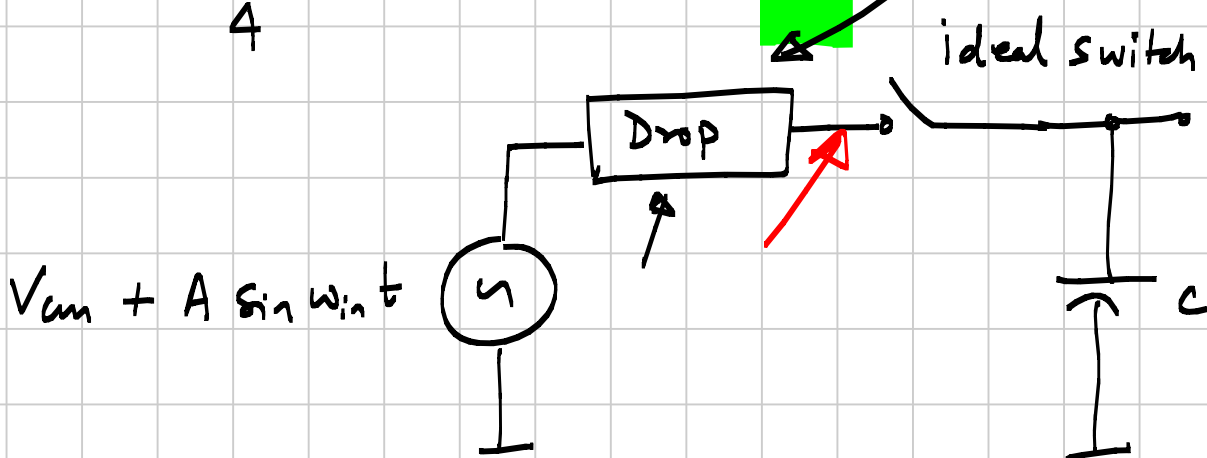
Note Title

09-12-2010



$$\begin{aligned}
 V_x(t) \approx & CA \omega_{in} R_{on} \cos(\omega_{in} t) \\
 & + \frac{CA^2}{2} r_1 \omega_{in} \sin(2\omega_{in} t) \\
 & - \frac{CA^3}{4} r_2 \omega_{in} \cos(3\omega_{in} t)
 \end{aligned}$$

Drop across the switch



$$HD_2 = \frac{CA^2 r_1}{2} \frac{\omega_{in}}{A} = \frac{C}{2} r_1$$

$$HD_3 = \frac{CA^3 r_2}{4} \frac{\omega_{in}}{A} = \frac{C}{4} r_2$$

Eg: $f_{in} = 400 \text{ kHz}$ $f_s = 1 \text{ MHz}$
 $2 f_{in} = 800 \text{ kHz} \rightarrow 200 \text{ kHz}$

$$3 f_n = 1.2 \text{ MHz} \rightarrow 200 \text{ kHz}$$

$$\frac{A^2 C}{2 kT} = \text{SNR}$$

$$A \downarrow 2, \quad HD_2 \downarrow 2, \quad HD_3 \downarrow 4$$

$$\text{SNR} \downarrow 4$$

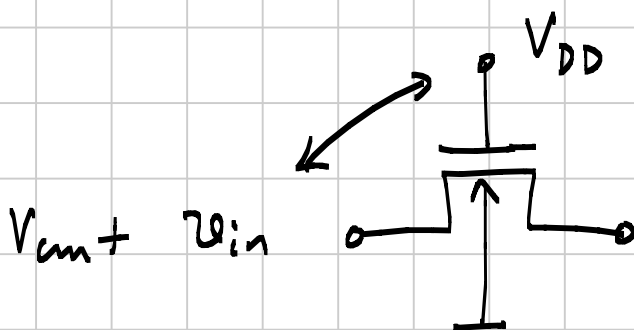
$$\Rightarrow C \uparrow 4 \Rightarrow \text{Cap. current} \uparrow 2$$

$$HD_2 = \frac{4 C \frac{A}{2} W_{in} r_1}{2} = 2 \frac{CA W_{in}}{2}$$

$$HD_3 = \frac{4 C \frac{A^2}{4} W_{in} r_2}{4} = \frac{CA^2 W_{in}}{4}$$

→ Need to reduce r_1 & r_2

⇒ Resistance must be independent of the input signal



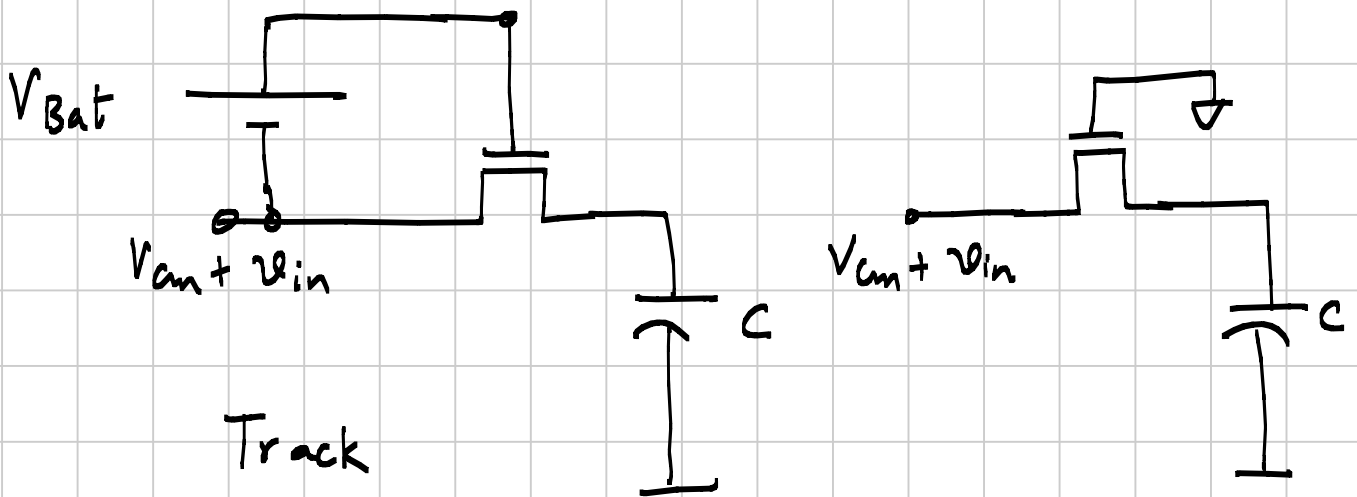
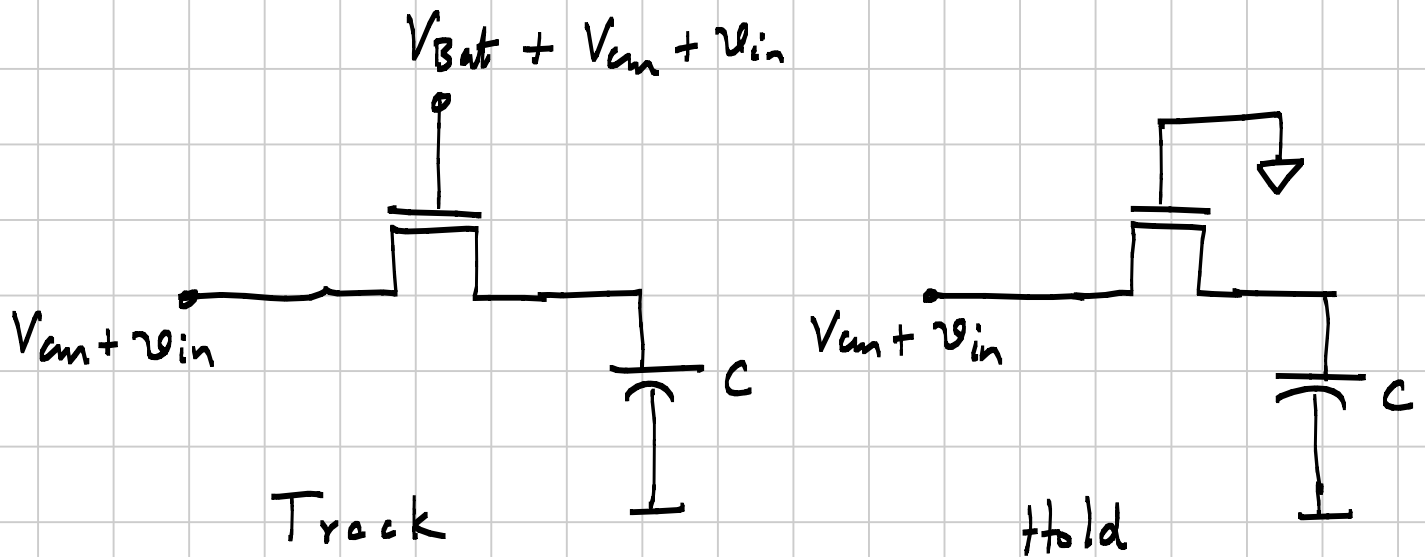
$$V_{GS} = V_{DD} - V_{cm} - V_{in}$$

$$R_{sw} \propto \frac{1}{(V_{GS} - V_T)}$$

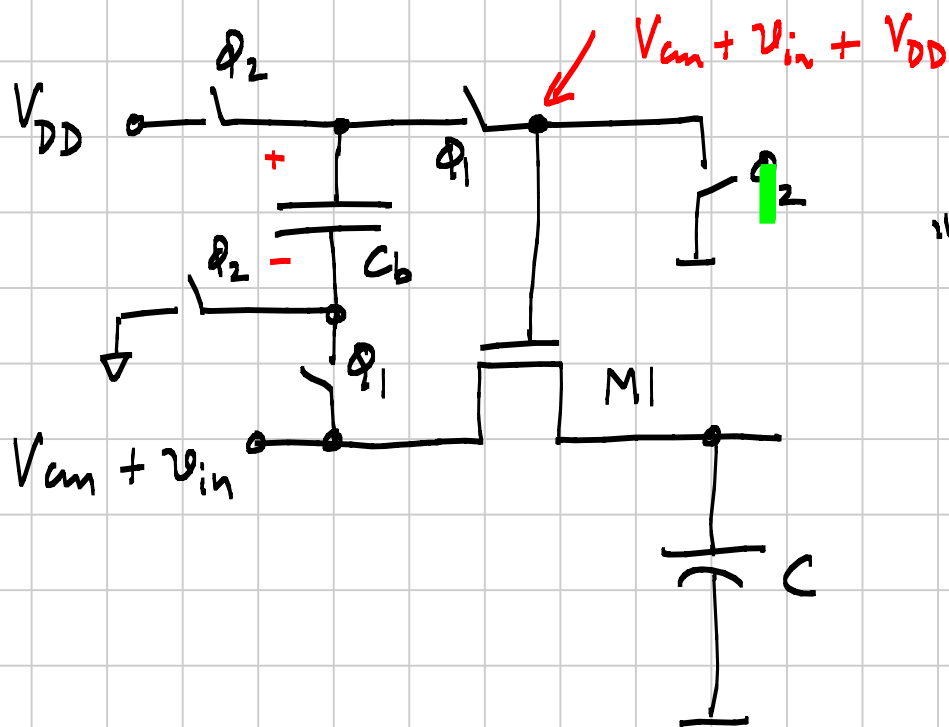
If V_{GS} was independent of input

→ R_{sw} would be " " "

→ Linear operation



- 1) V_{Bat} only in track phase (ϕ_1)
- 2) No current through V_{Bat}

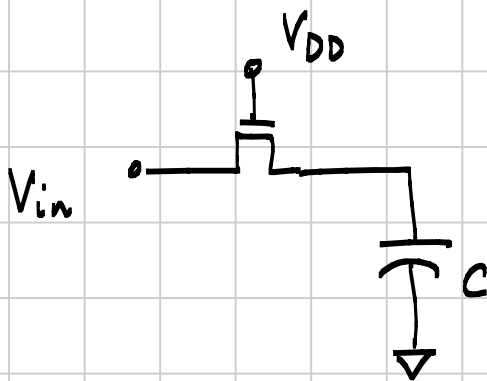


" Bootstrapped
Sampling"
switch

VLSI Data Conversion Circuits : Lecture 8

Note Title

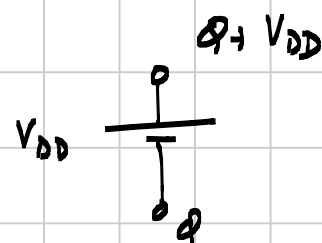
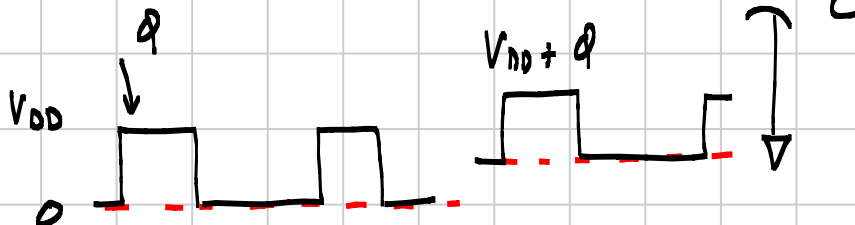
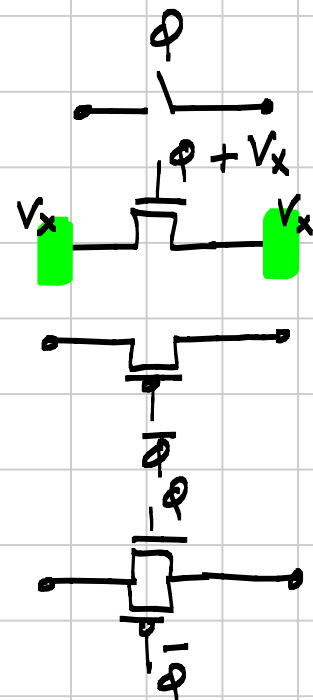
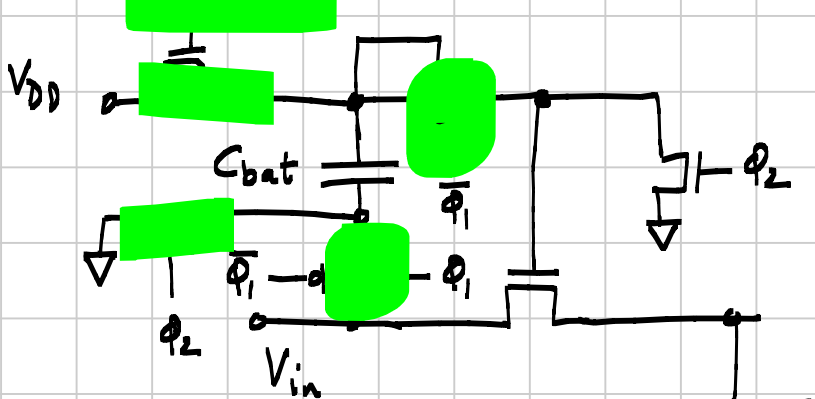
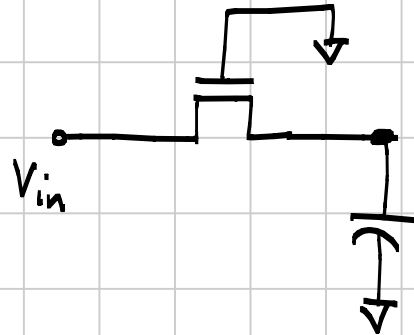
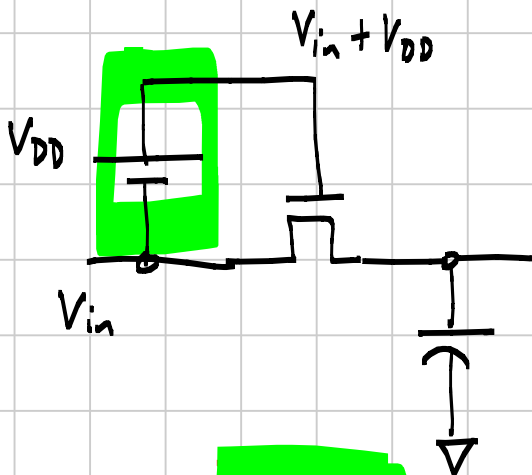
14-12-2010

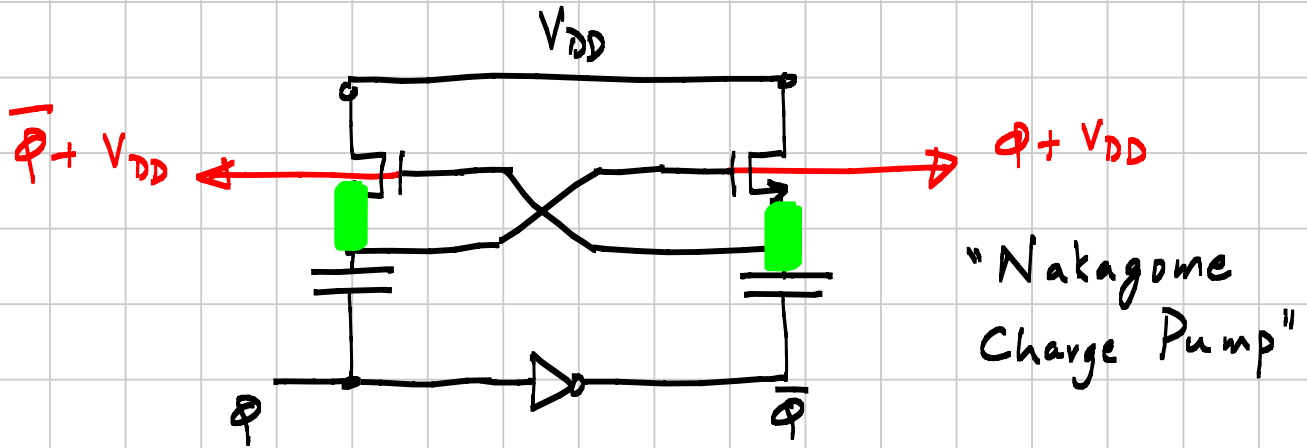
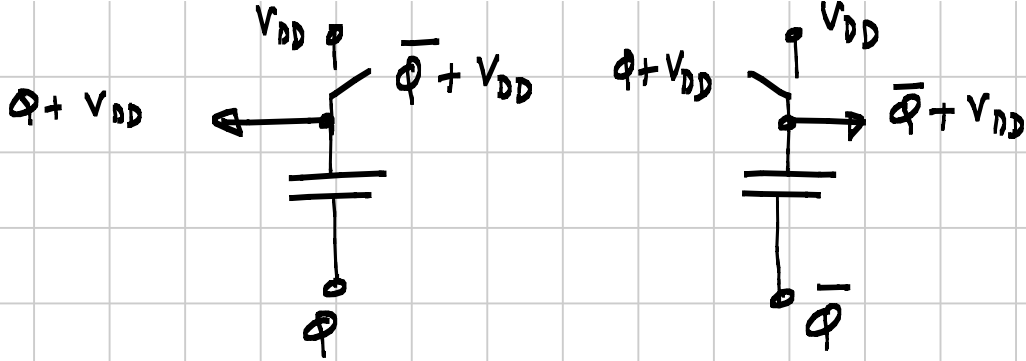


Sample :

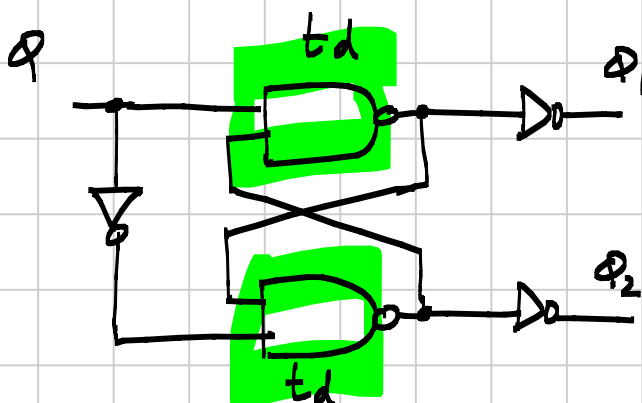
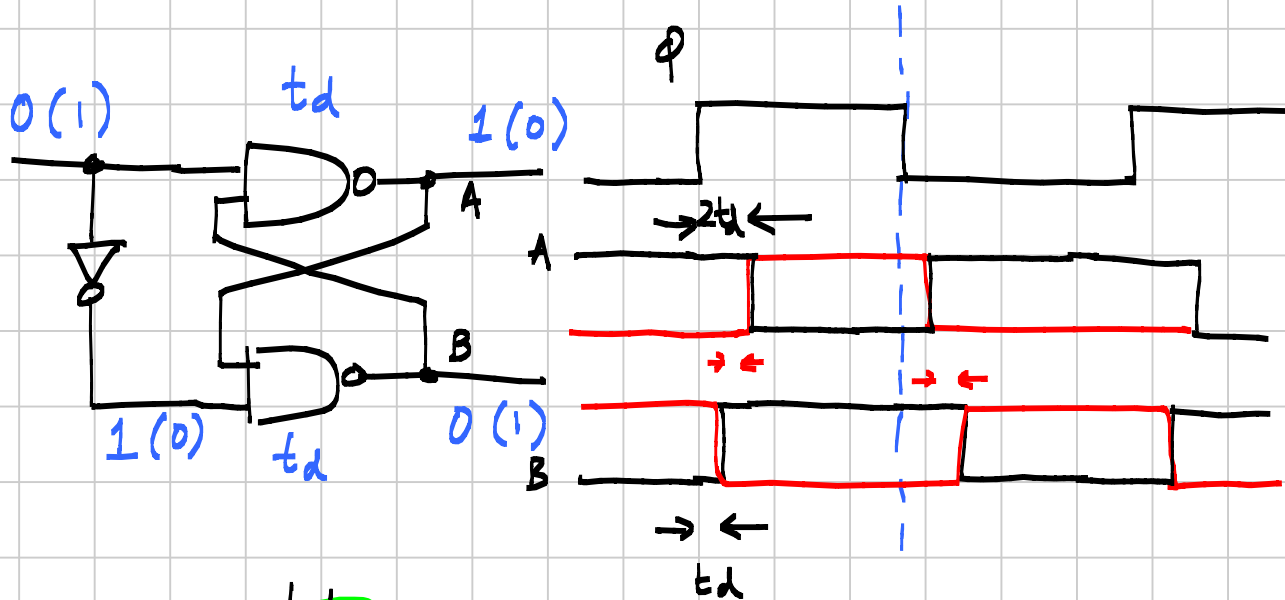
$$V_{GS} = V_{DD} - V_{in}$$

$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{DD} - V_{in} - V_T)}$$





Φ_1 & Φ_2 must not overlap



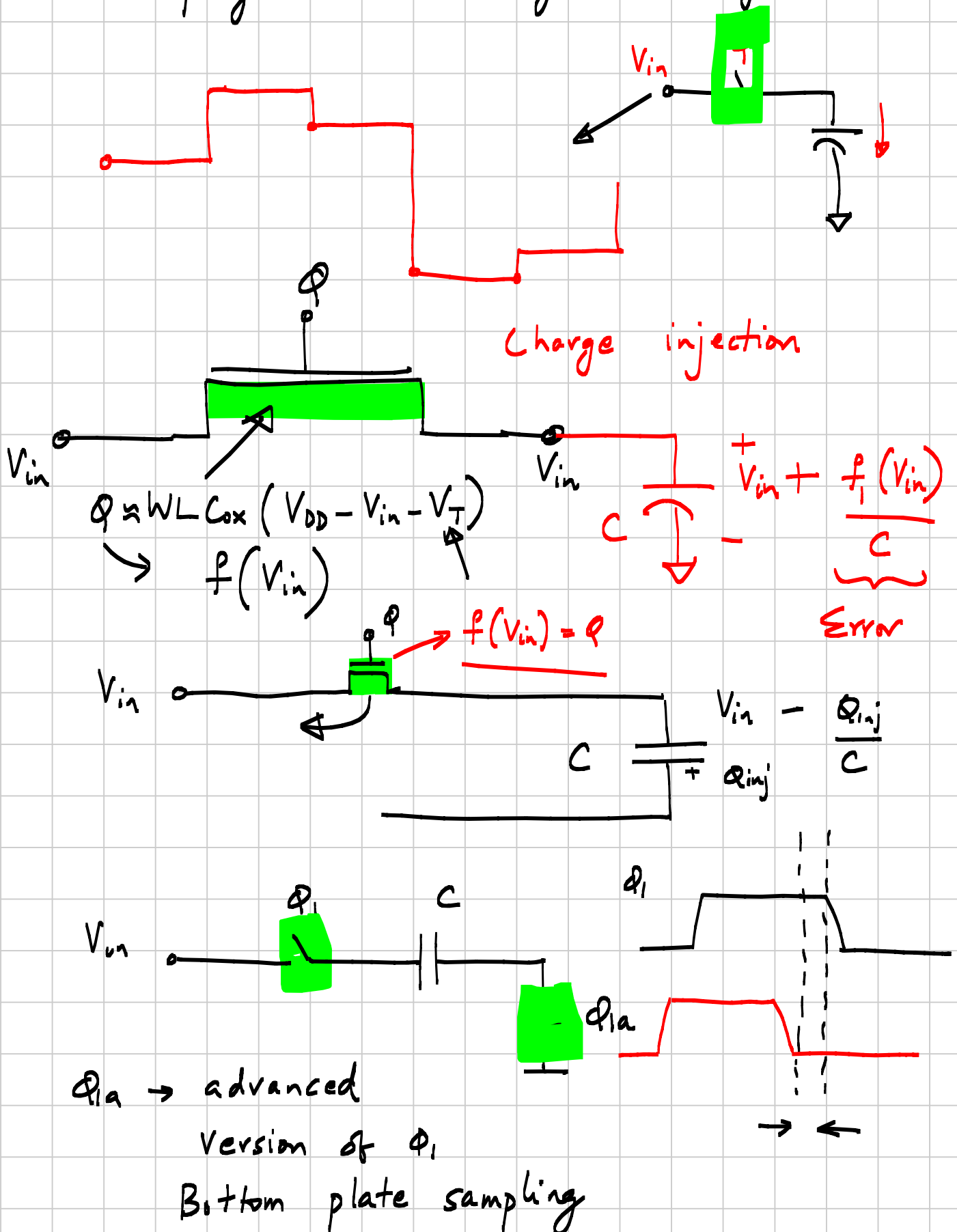
Non-overlapping
clock generator

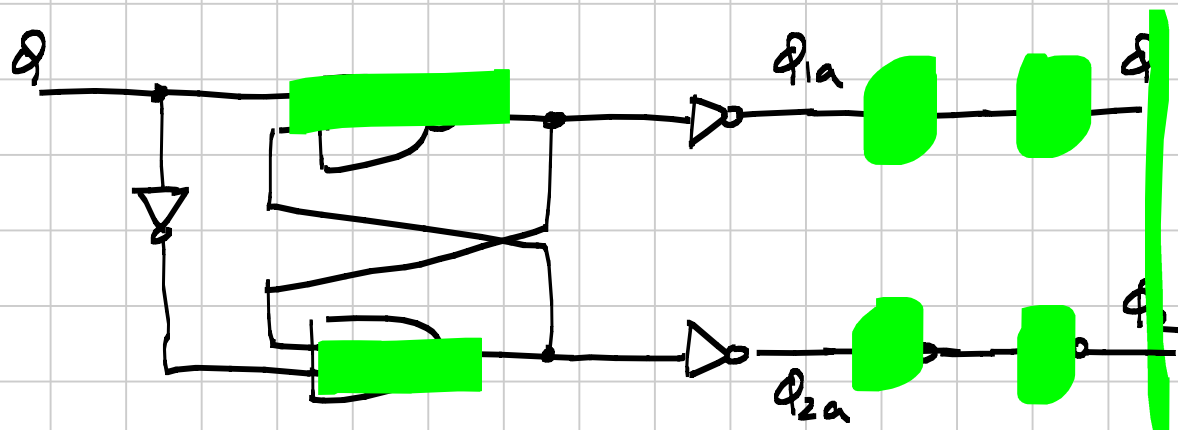
VLSI Data Conversion Circuits : Lecture 9

Note Title

14-12-2010

* Sampling circuit with good linearity





VLSI Data Conversion Circuits : Lecture 10

Note Title

14-12-2010

* Sample & Hold Circuits

$$A \cos(2\pi f_{in} t) \rightarrow \boxed{S/H} \rightarrow x[n]$$

$$x[n] = A \cos\left(2\pi f_{in} \frac{n}{f_s}\right) = x(n+N)$$

$$\Rightarrow A \cos\left(2\pi f_{in} \frac{n}{f_s}\right) = A \cos\left(2\pi f_{in} \frac{(n+N)}{f_s}\right)$$

$$\Rightarrow A \cos\left(\frac{2\pi f_{in} n}{f_s}\right) = A \cos\left(\frac{2\pi f_{in} n}{f_s} + \underbrace{2\pi \frac{f_{in} N}{f_s}}_{\text{integer}}\right)$$

$$2\pi \frac{f_{in}}{f_s} N = 2\pi m \leftarrow \text{integer}$$

$$\boxed{\frac{f_{in}}{f_s} = \frac{m}{N}}$$

$$f_{in} = \frac{m}{N} f_s$$

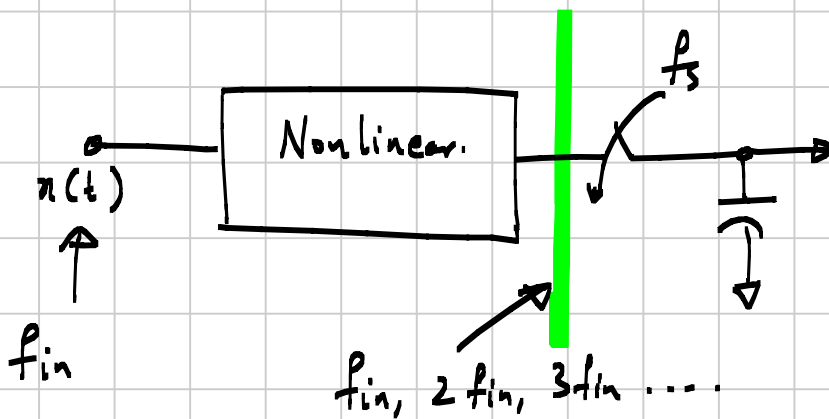
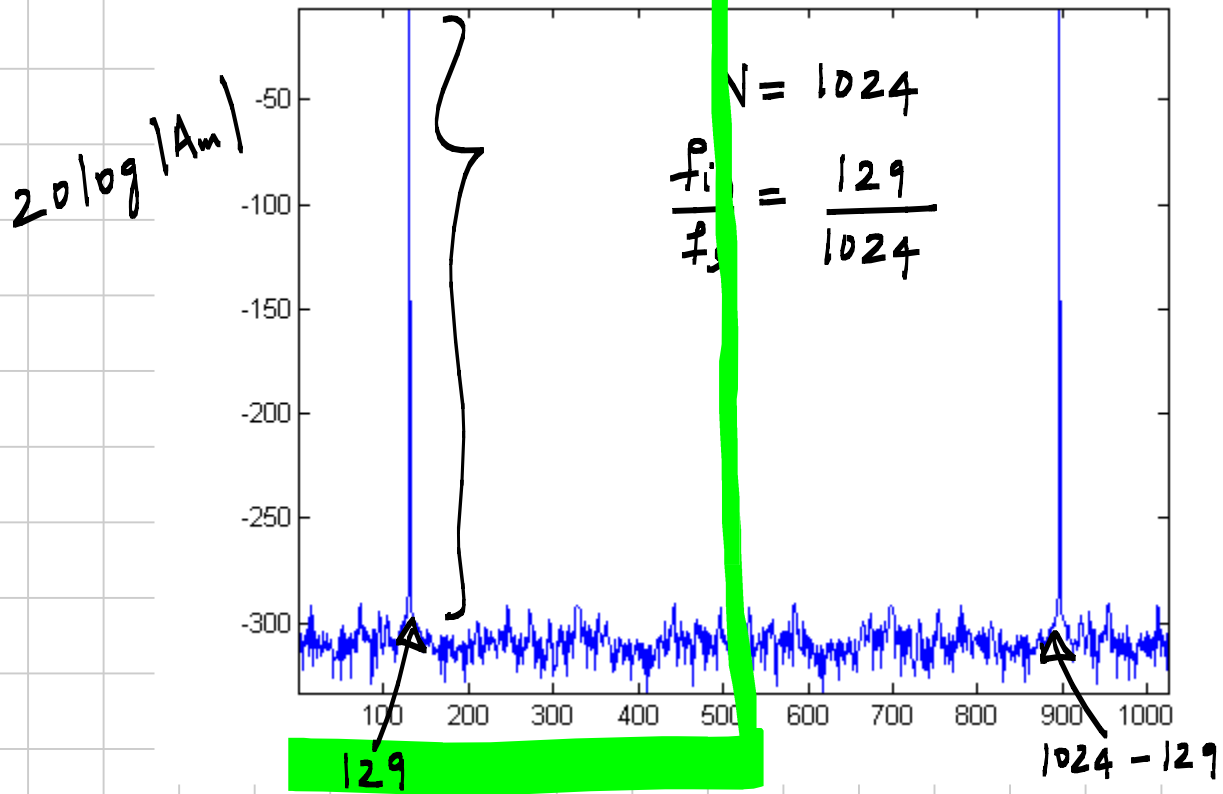
$$x(n) = \sum_{k=0}^{N-1} A_k \exp\left(j \frac{2\pi}{N} k n\right)$$

$N \rightarrow$ Record length

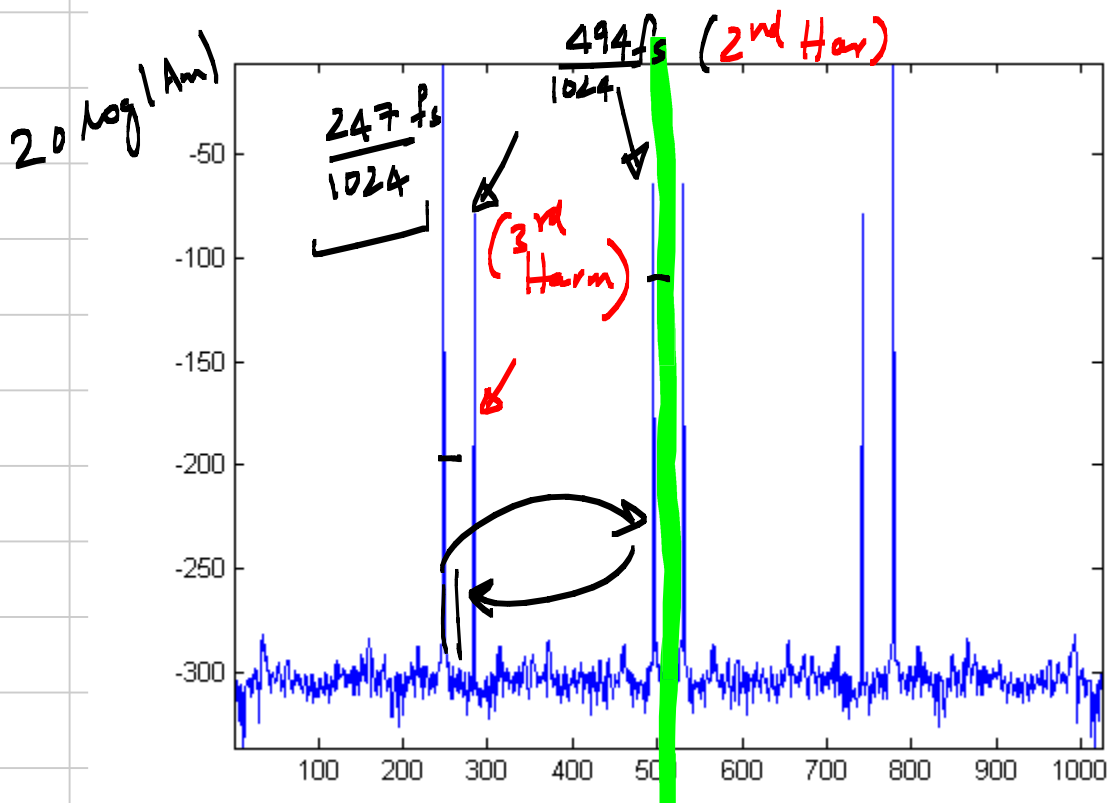
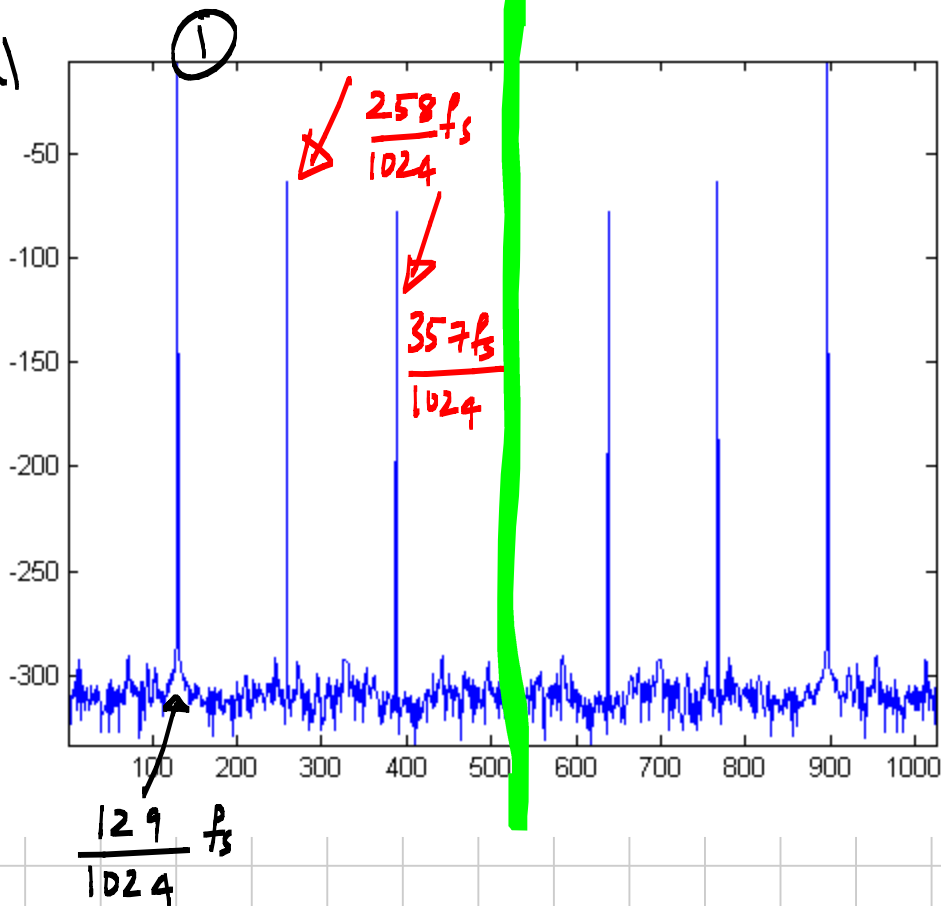
$\frac{2\pi}{N} k \rightarrow$ Frequency bins

$\frac{f_s}{N} \rightarrow$ "width of the bin"

$$A \cos\left(2\pi \frac{m}{N} f_s \cdot \frac{n}{f_s}\right) = A \cos\left(2\pi \frac{m}{N} n\right)$$



$20 \log |A_m|$
 $N = 1024$



$$\frac{f_{in}}{f_s} = \frac{m}{N}$$

Ex: $N = 1024$

$\odot \frac{f_s}{4}$

$\frac{f_{in}}{f_s} = \frac{256}{1024} \quad ??$

$$\begin{array}{c} 2^{\text{nd}} \\ 6^{\text{th}} \end{array} \rightarrow \frac{512}{1024} f_s$$

$$\begin{array}{c} 3^{\text{rd}} \\ 5^{\text{th}} \\ 7^{\text{th}} \end{array} \rightarrow \frac{256}{1024} f_s$$

VLSI Data Conversion Circuits : Lecture 11

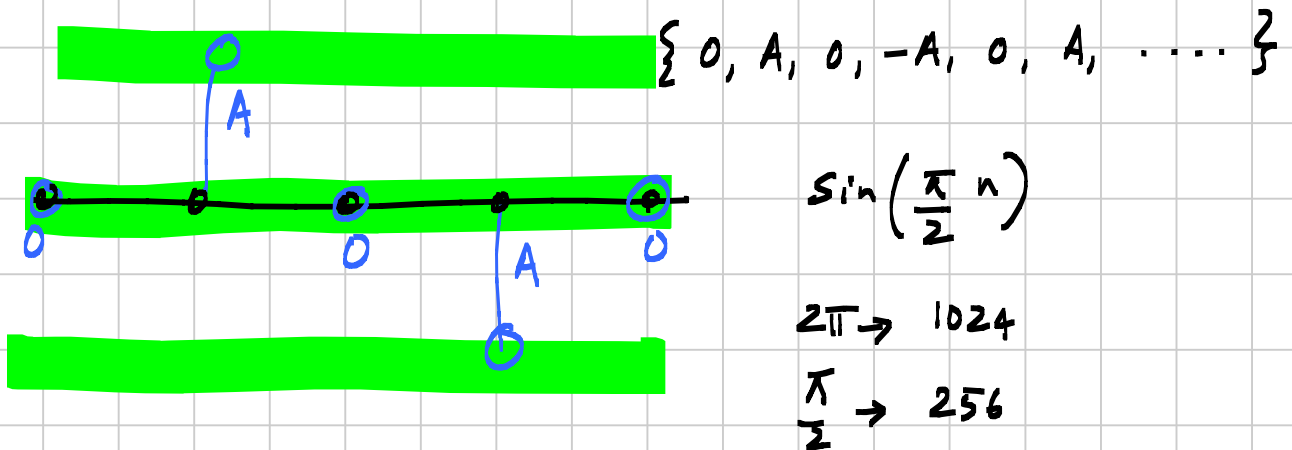
Note Title

14-12-2010

$$\frac{f_{in}}{f_s} = \frac{m}{N} \rightarrow \text{Record length}$$

$$N = 1024$$

$$m = 256$$



$\frac{m}{N}$ } Choose m & N to be relatively prime

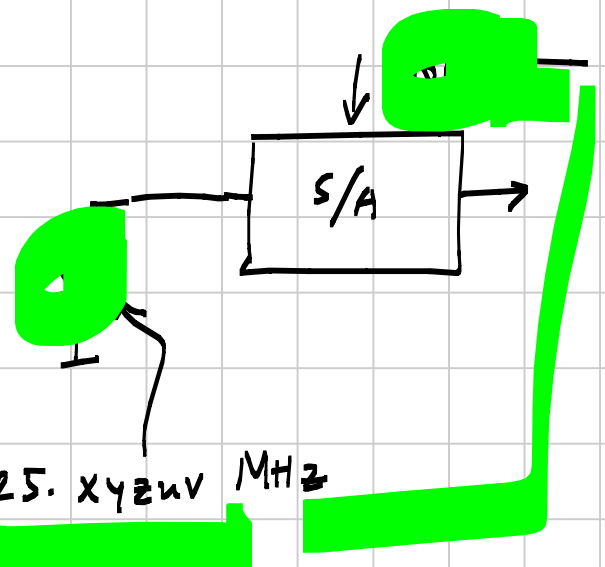
Ex: @ $\frac{f_s}{4} \Rightarrow \frac{247}{1024}$ }

@ $\frac{f_s}{2} \Rightarrow \frac{503}{1024}$

$f_{in} \leftarrow f_s$

$f_s = 100 \text{ MHz}$

$f_{in} = f_s \cdot \left(\frac{259}{1024}\right) = 25.442 \text{ MHz}$

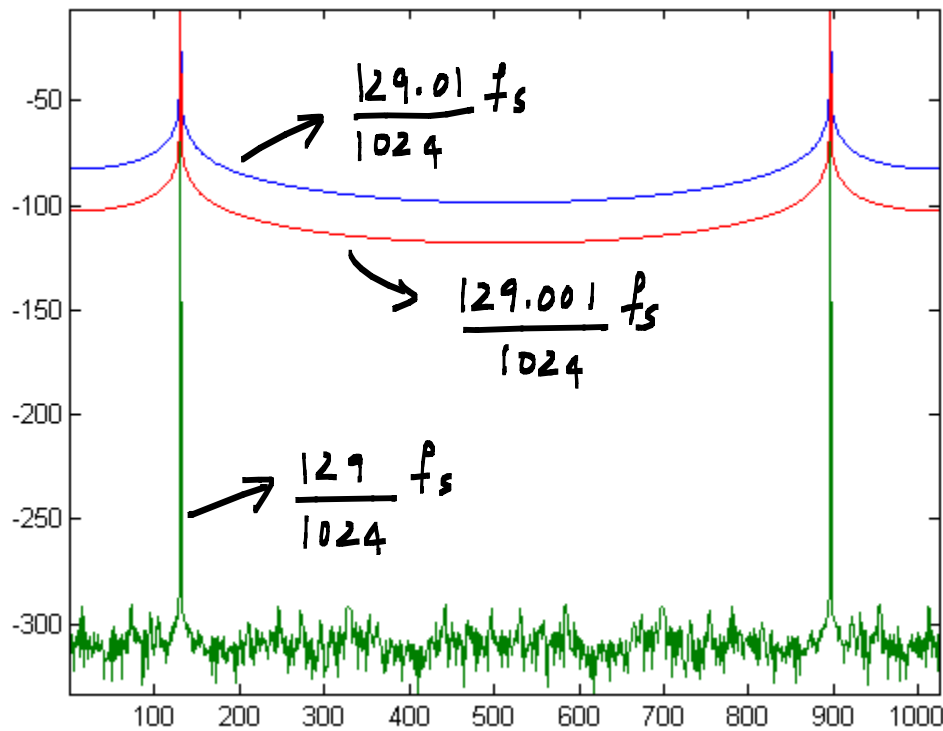


"Synchronous Sampling"

$$f_{in} = \frac{129}{1024} f_s$$

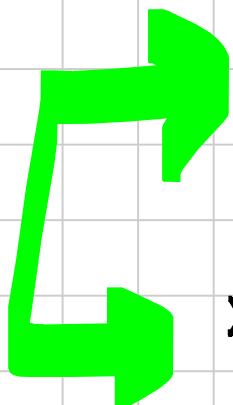
$$\frac{129.01}{1024} f_s \quad ??$$

Alien
Tower
Effect



$$\cos\left(2\pi \frac{129.01}{1024} f_s \cdot \frac{n}{f_s}\right) \rightarrow \text{Not periodic}$$

$x[n]$ = finite length sequence of length M

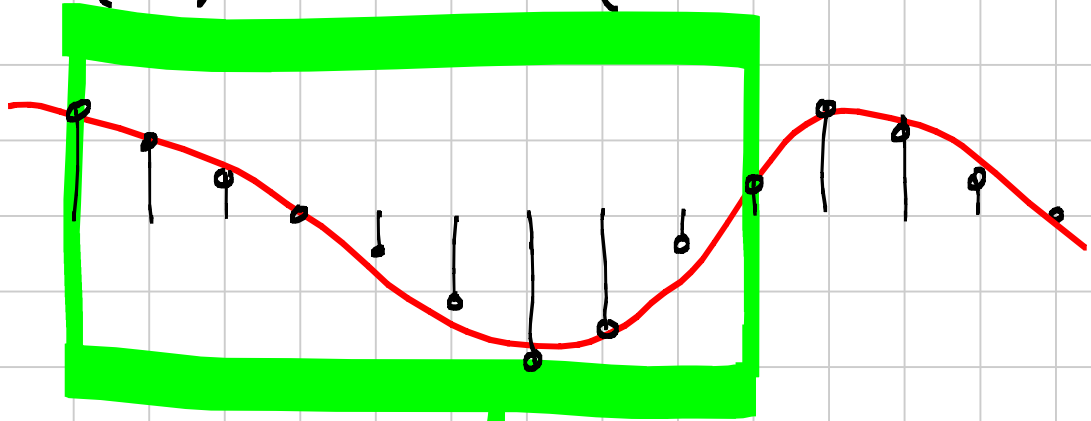


$$X(j\omega) = \sum_{n=0}^{M-1} x[n] e^{-j\omega n}$$

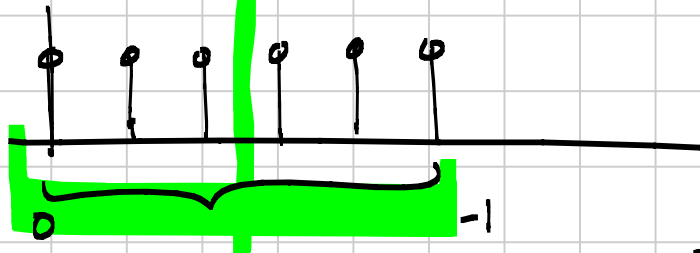
$$X(k) = \sum_{n=0}^{M-1} x[n] e^{-j \frac{2\pi k}{M} n}$$

DFS $\rightarrow$ sampled version of $X(j\omega)$

$$\cos(an) \rightarrow \pi (\delta(\omega - a) + \delta(\omega + a))$$



$\cos(an)$

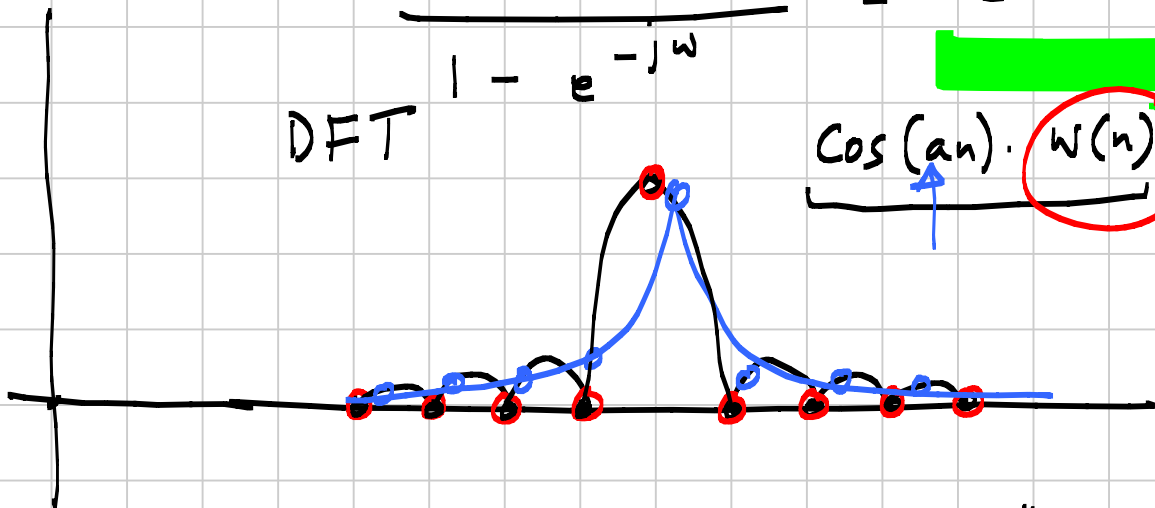


$$1 + e^{-j\omega} + \dots + e^{-j\omega(M-1)}$$

$$= \frac{1 - e^{-j\omega M}}{1 - e^{-j\omega}} = e^{-j\omega \frac{M-1}{2}} \frac{\sin\left(\frac{\omega M}{2}\right)}{\sin\left(\frac{\omega}{2}\right)}$$

DFT

$\cos(an) \cdot \omega(n)$



$$\frac{\omega M}{2} = \pi, 2\pi, 3\pi, \dots$$

$$\Rightarrow \frac{2\pi}{M}, \frac{4\pi}{M}, \dots$$

"Not residing on a bin"
Leakage in the FFT

VLSI Data Conversion Circuits : Lecture 12

Note Title

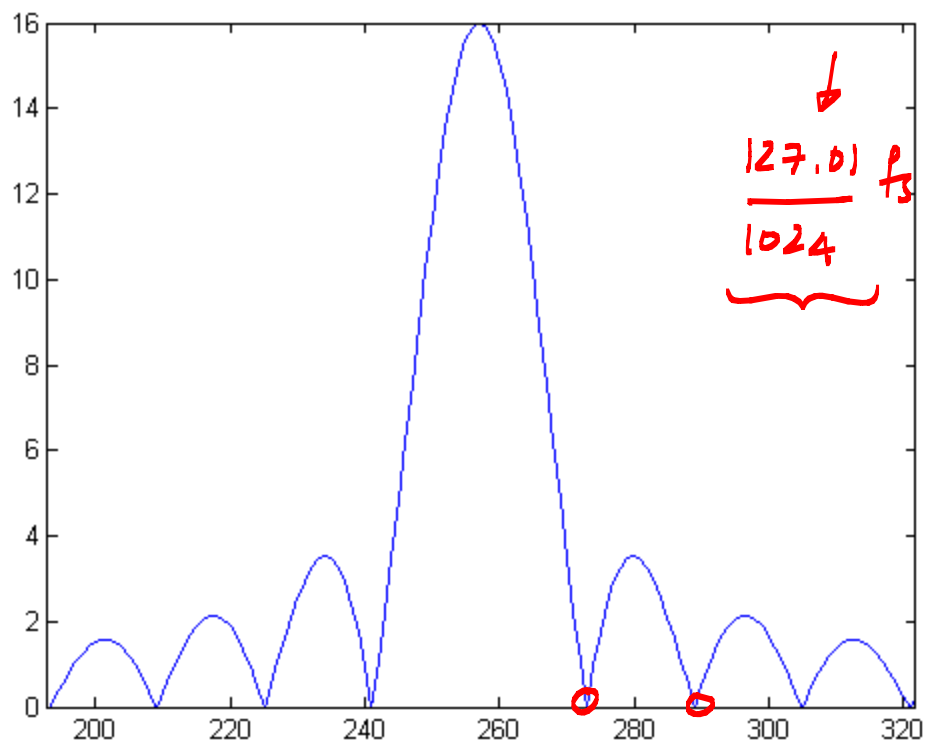
14-12-2010

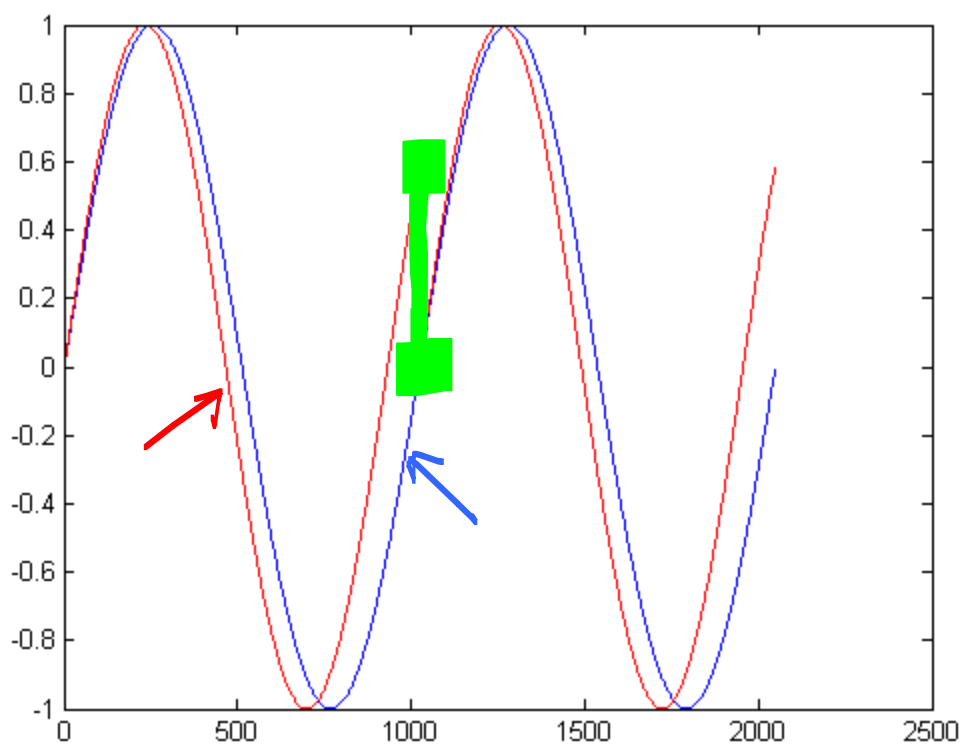
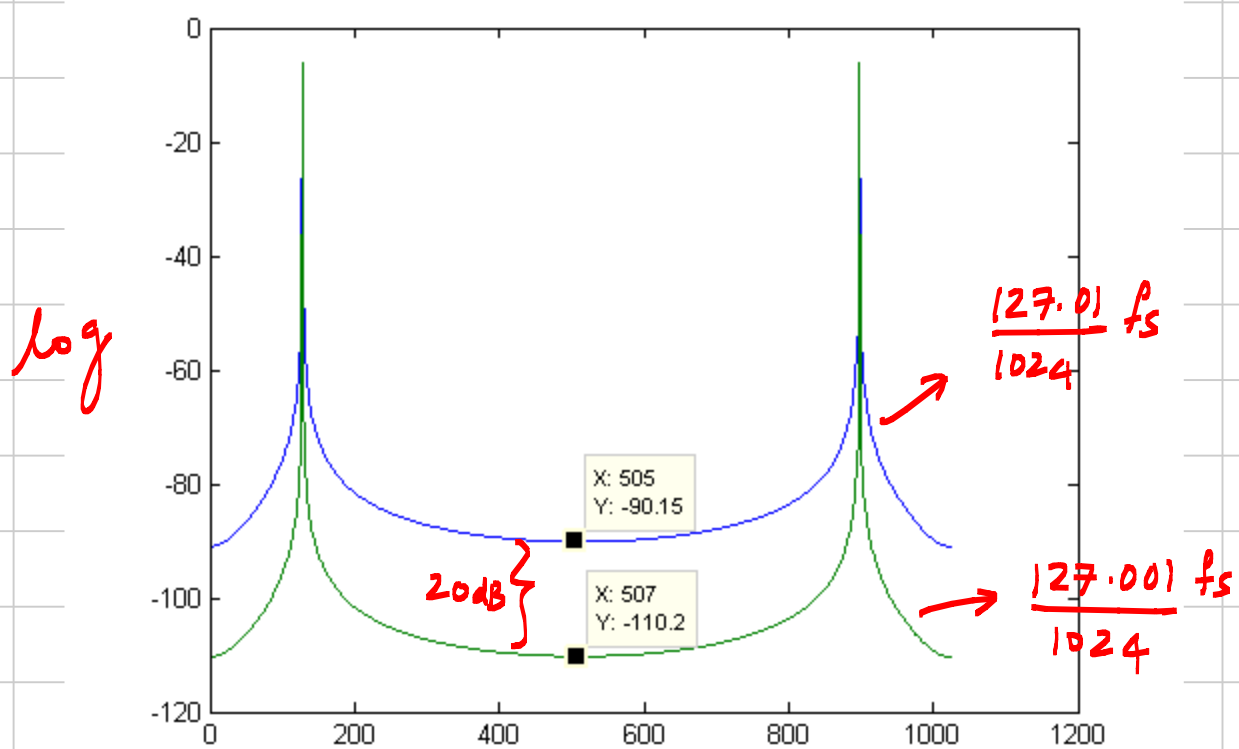
$$f_{in}, f_s \Rightarrow \frac{f_{in}}{f_s} = \frac{m}{N}$$

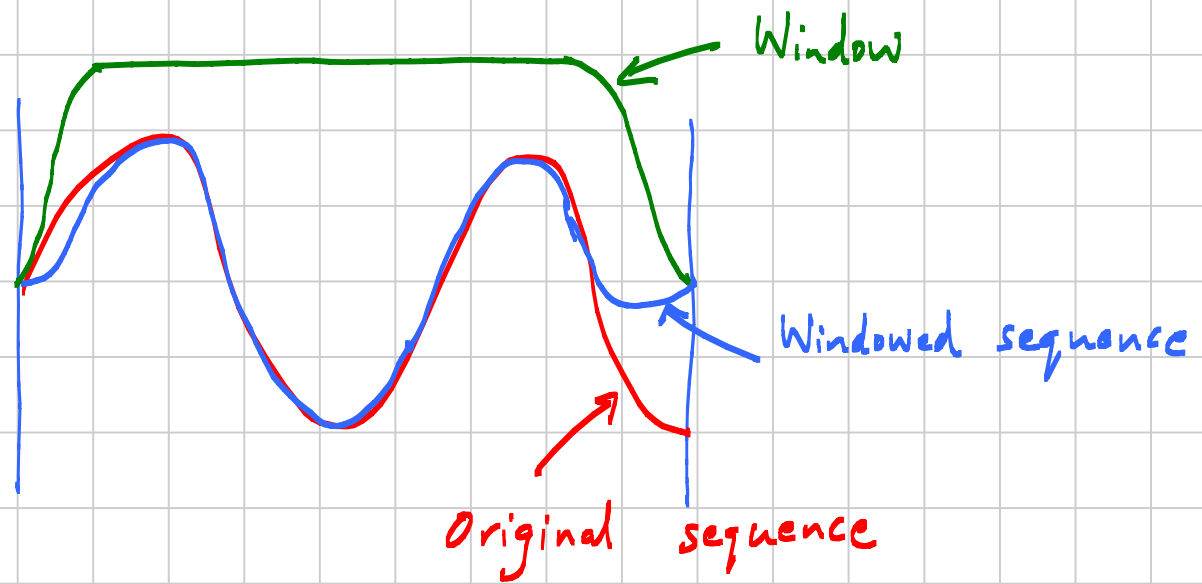
$N \rightarrow$ Record length (2^P)

$$x_{in}(n) = A \cos(an) \rightarrow$$

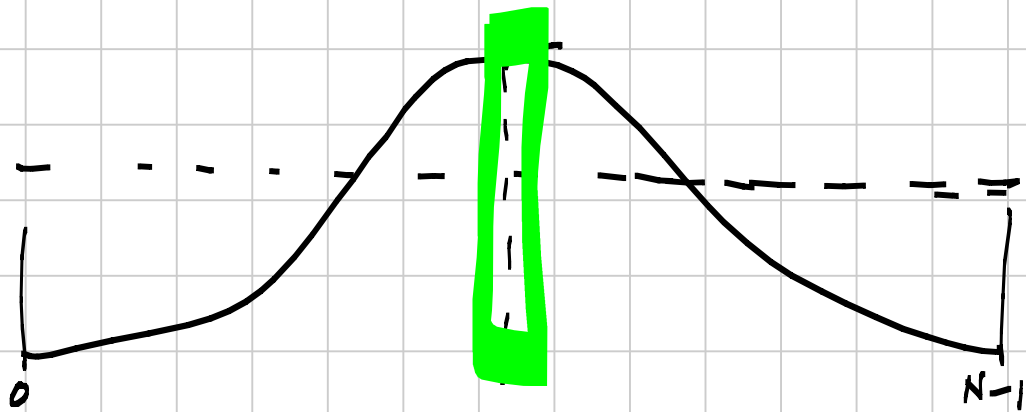
$$\underbrace{\pi [\delta(\omega - a) + \delta(\omega + a)]}_{\Delta, 2\Delta} * \underbrace{w(n)}_{\uparrow}$$







Hann
Window



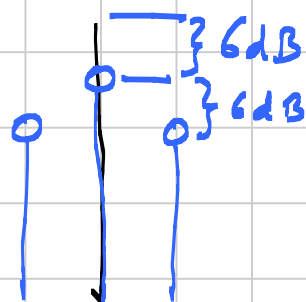
$$0.5 \left[1 - \cos\left(2\pi \frac{n}{N}\right) \right] \quad \left\{ \quad 0 \leq n \leq N-1 \right.$$

$$\cos(an) \cdot \left\{ 0.5 \left(1 - \cos\left(\frac{2\pi}{N}n\right) \right) \right\} \cdot \text{rect}(N)$$

$$\cos(an) - 0.5 \cos\left(\frac{2\pi}{N}n\right) \cdot \cos(an)$$

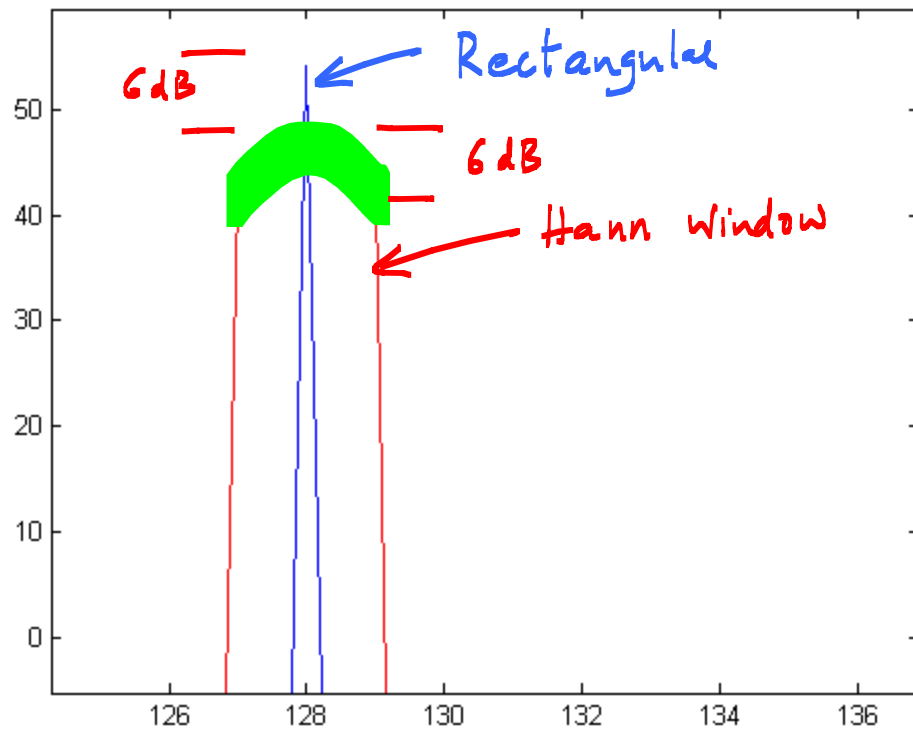
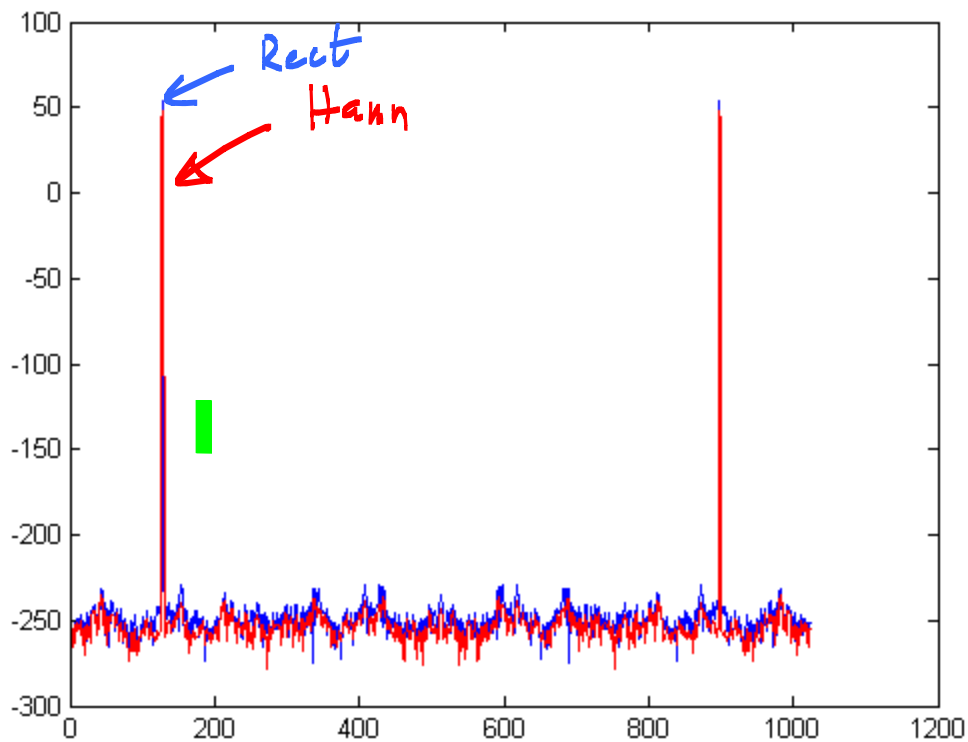
$$\begin{array}{ccc} a - \frac{2\pi}{N} & a & a + \frac{2\pi}{N} \\ \downarrow & \downarrow & \downarrow \\ \frac{1}{4} & 0.5 & \frac{1}{4} \end{array}$$

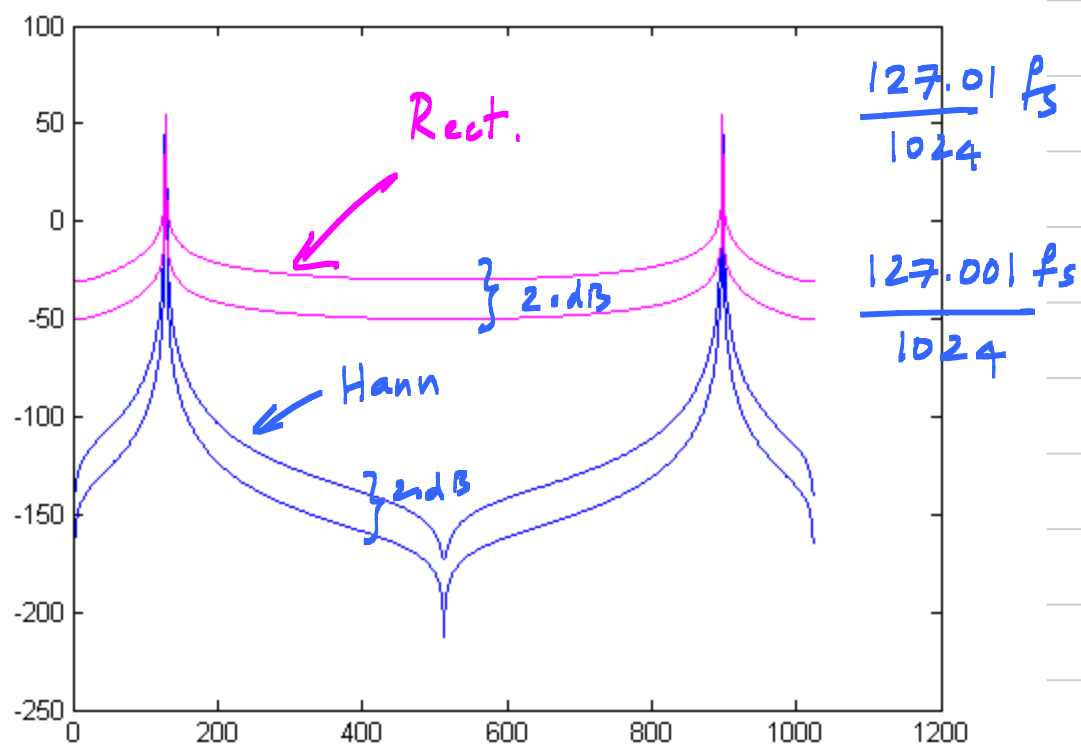
$$\begin{array}{l} \frac{1}{4} \cos\left(\left(a + \frac{2\pi}{N}\right)n\right) \\ \frac{1}{4} \cos\left(\left(a - \frac{2\pi}{N}\right)n\right) \end{array}$$



$$\frac{3}{8} \leq \frac{1}{4} + \frac{1}{16} + \frac{1}{16} \leftarrow \text{Power of the windowed seq.}$$

$$1 \leftarrow \text{Rect. windowed seq.}$$

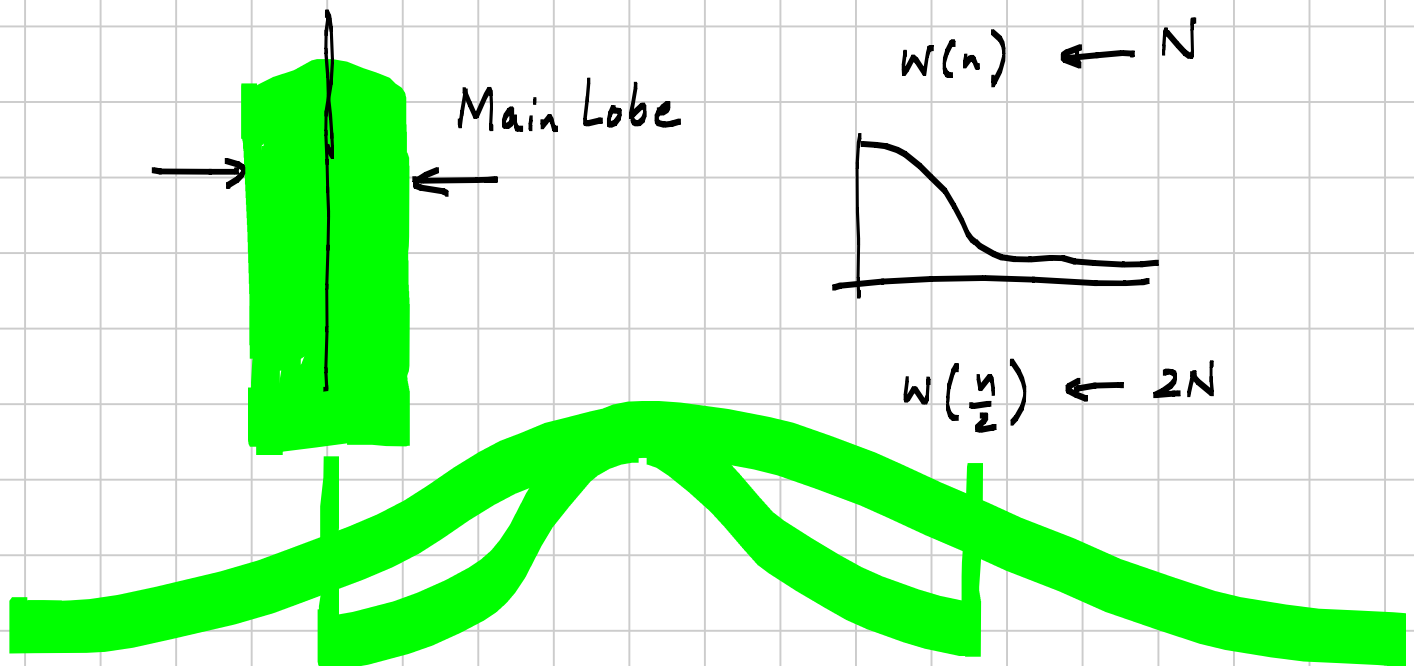




VLSI Data Conversion Circuits: Lecture 13

Note Title

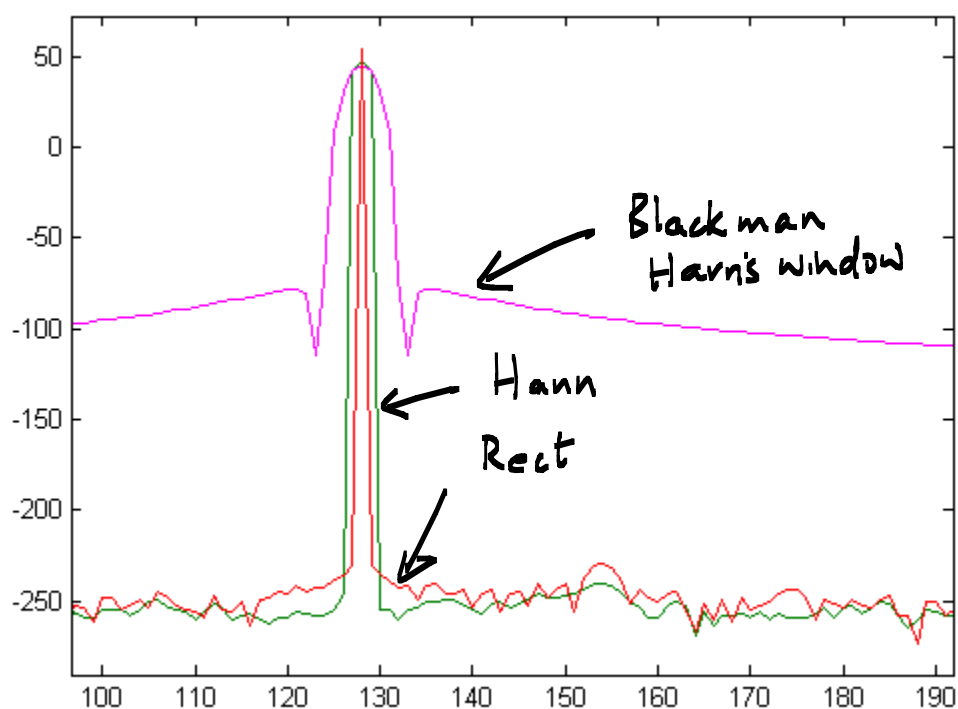
14-12-2010

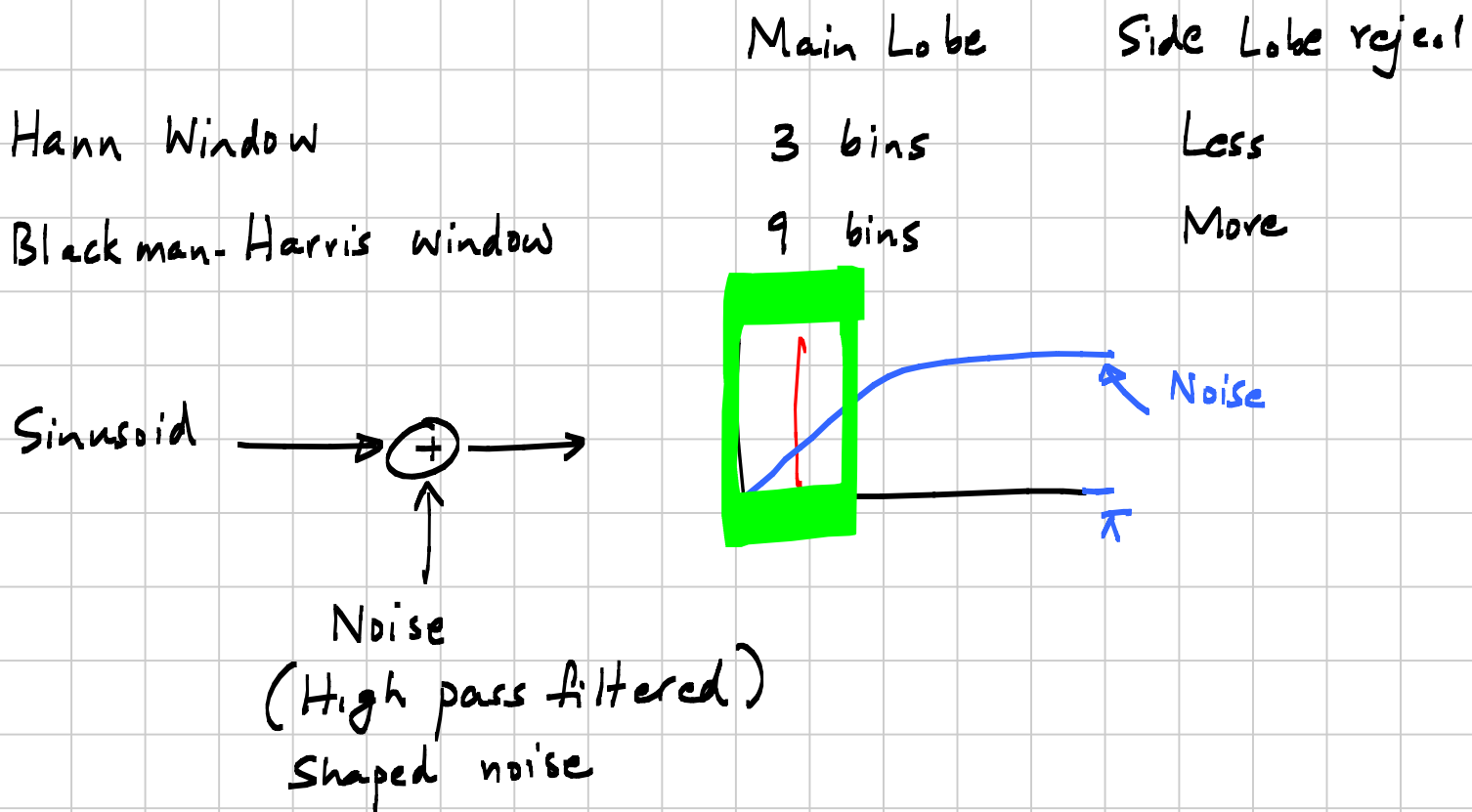
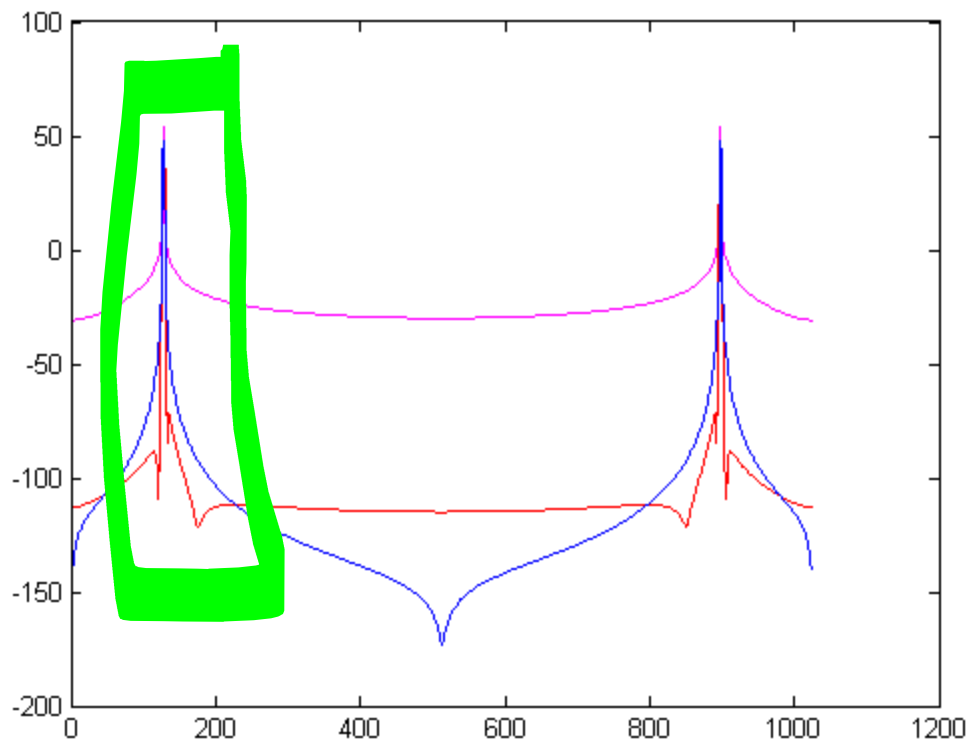


Main Lobe is wide

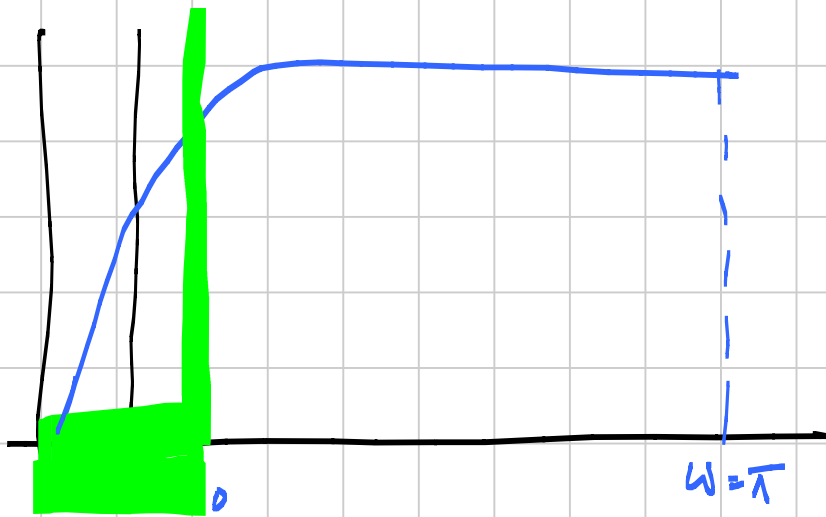
→ Side Lobes are lower

Blackman-Harris window





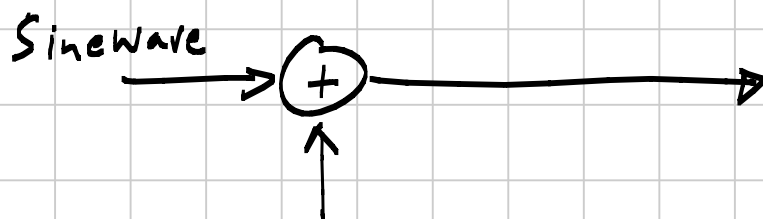
log



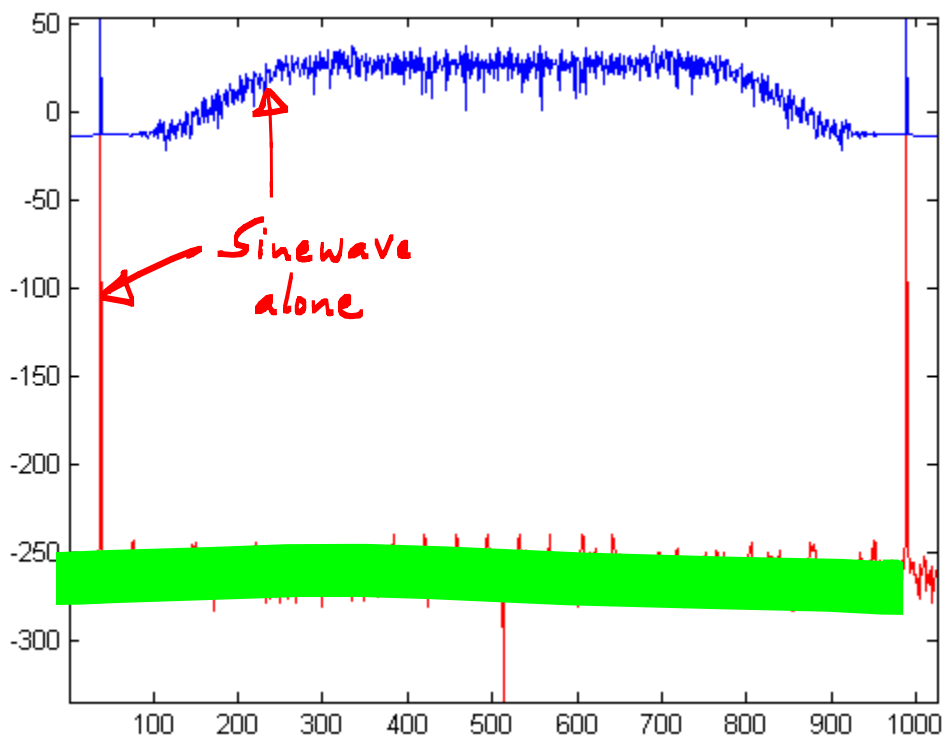
* Sinewave 15
on a bin

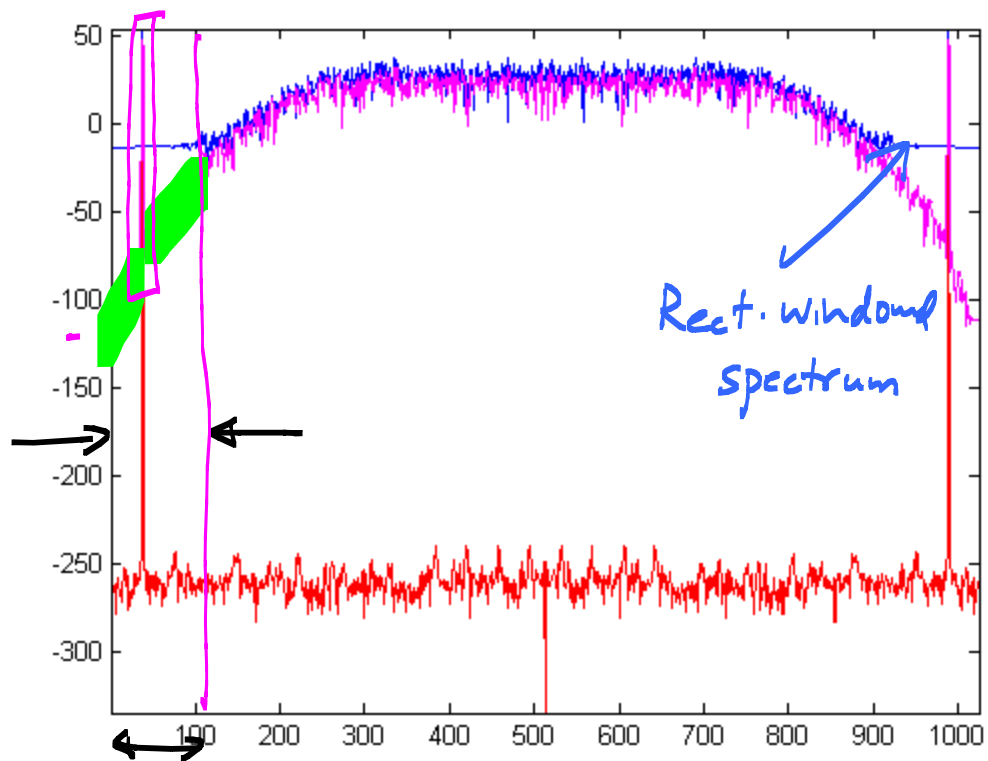
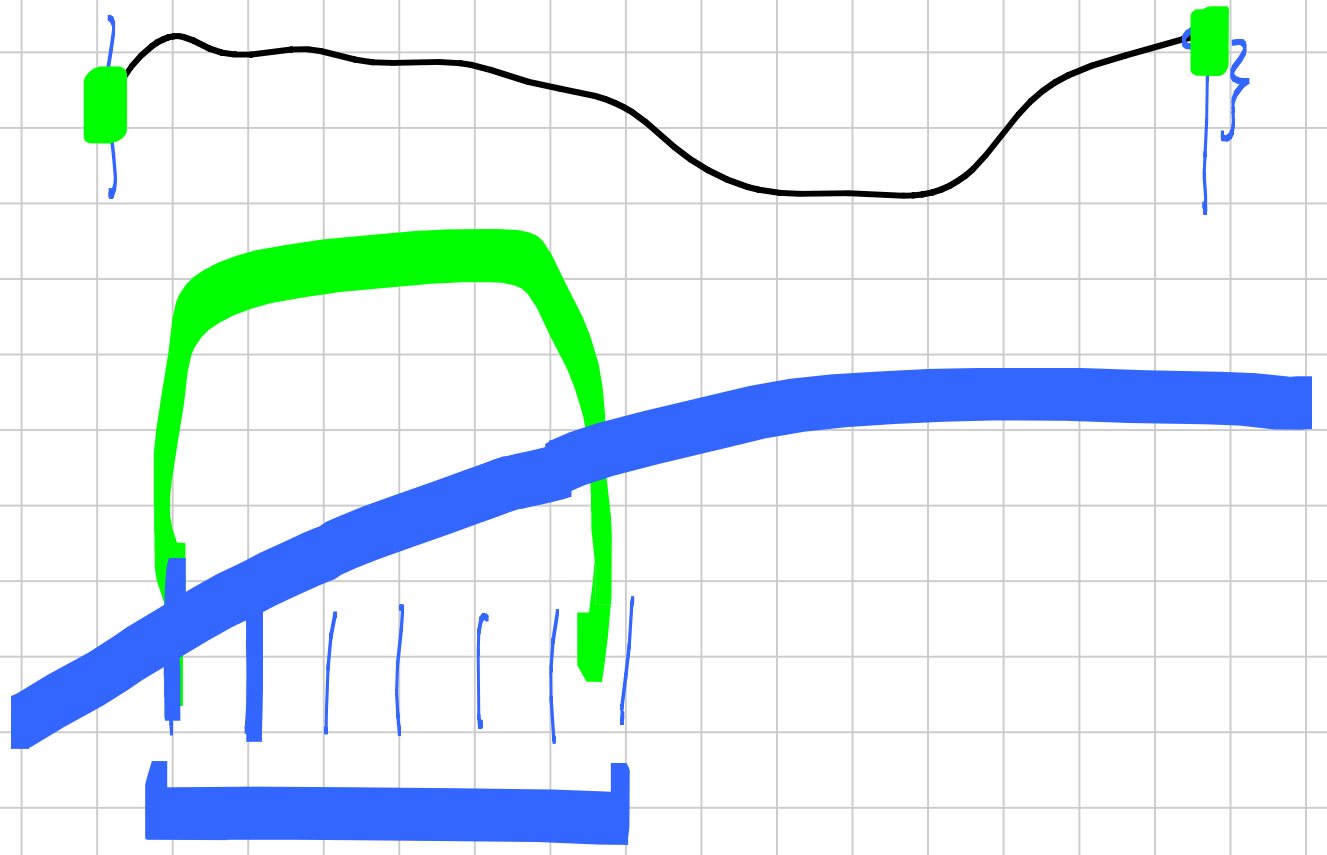
N

$$\frac{f_{in}}{f_s} = \frac{2}{3}$$



White Noise → Butter worth
5th order HPF



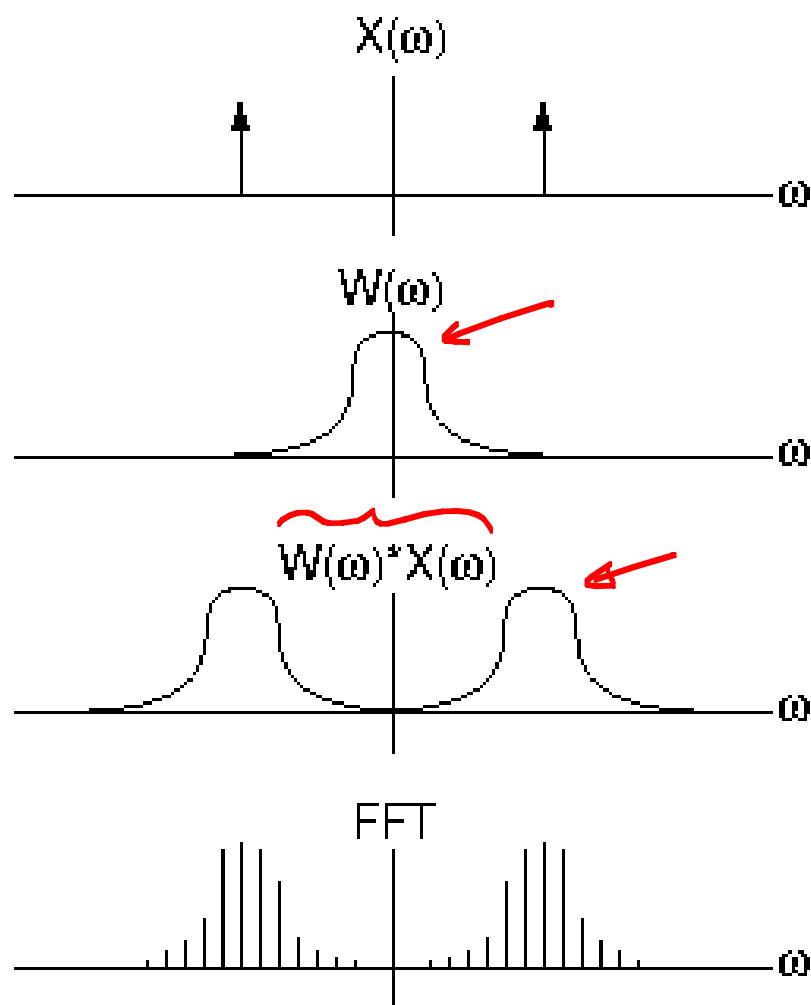


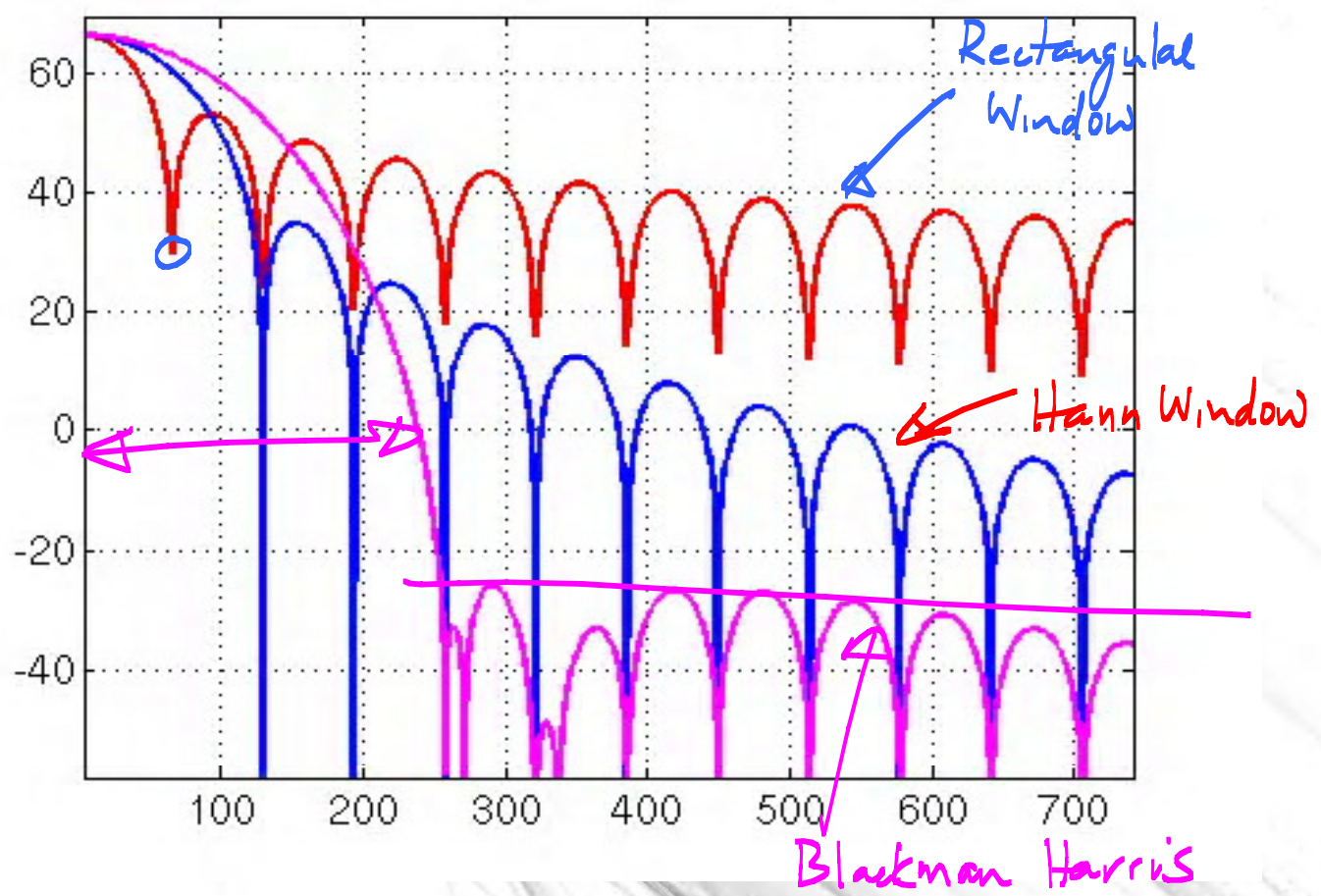
* Signal is on a bin $\rightarrow$ Hann window

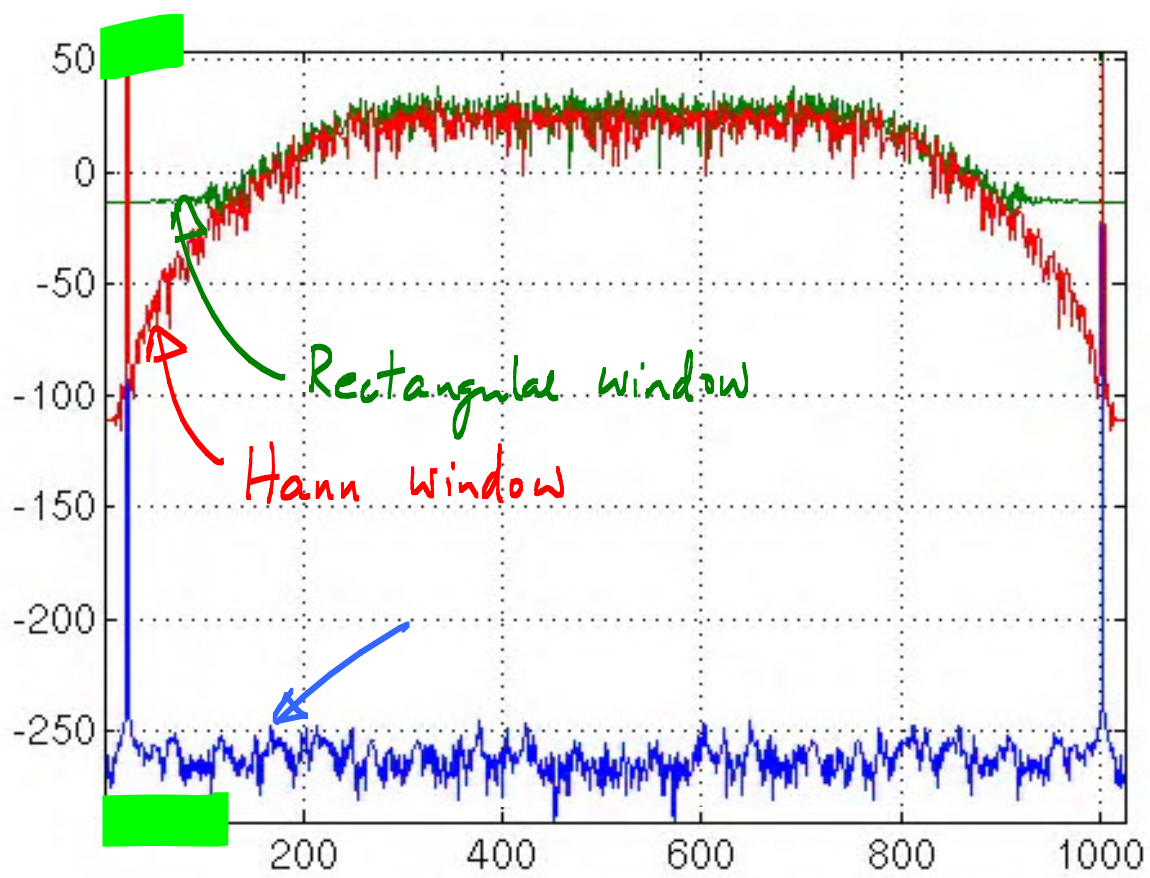
*

VLSI Data Conversion Circuits: Lecture 14

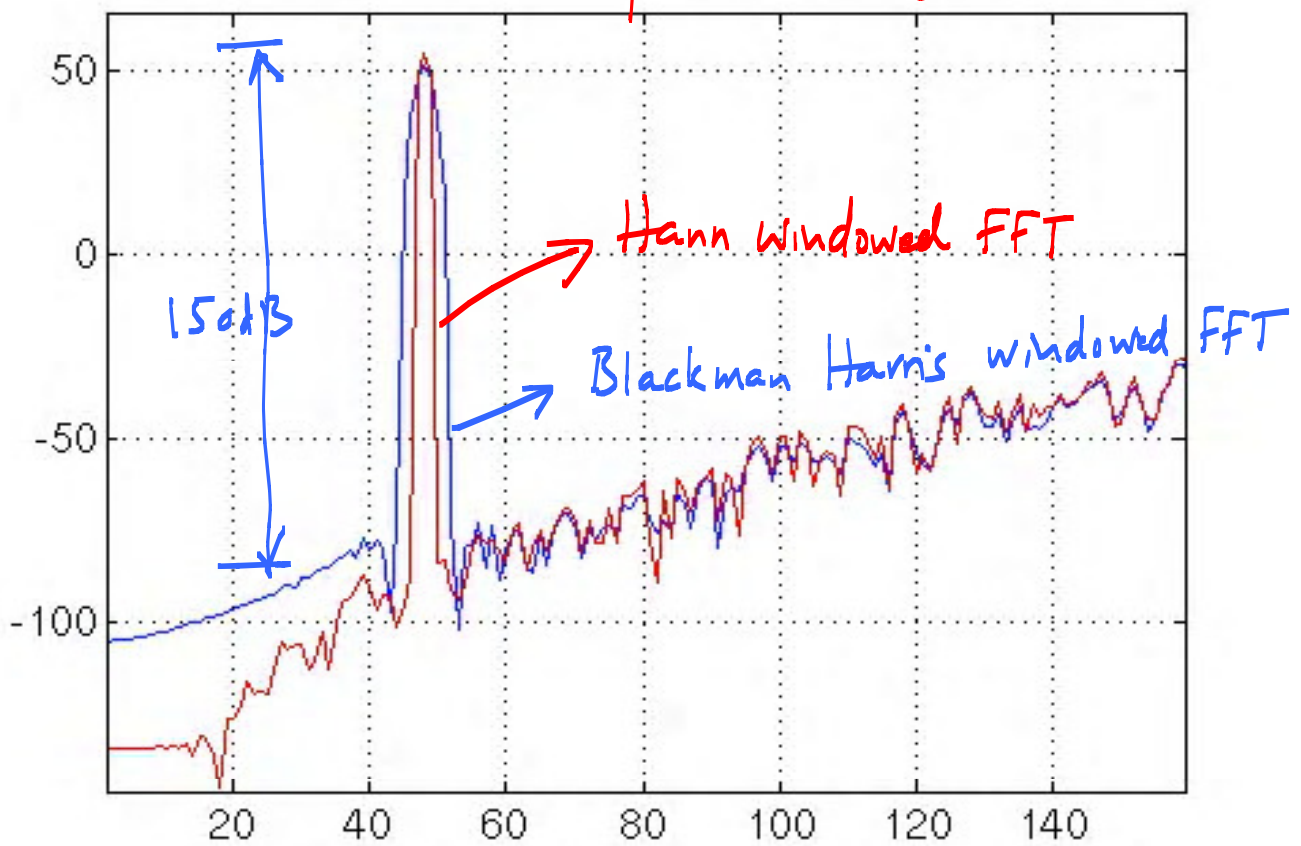
$\cos(an)$







Input is on an FFT bin



Simulation

Measurement

Hann Window

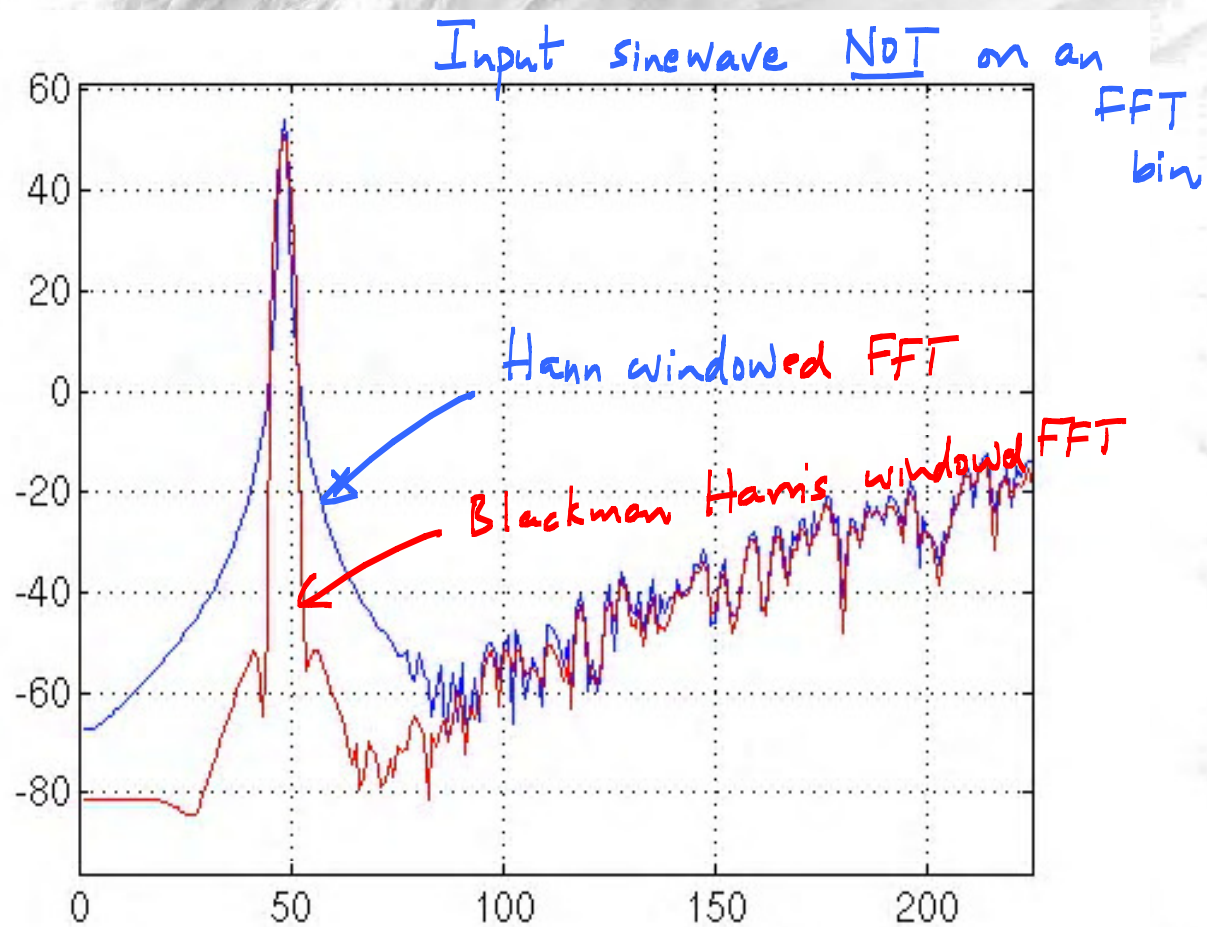


Blackman Harris Window



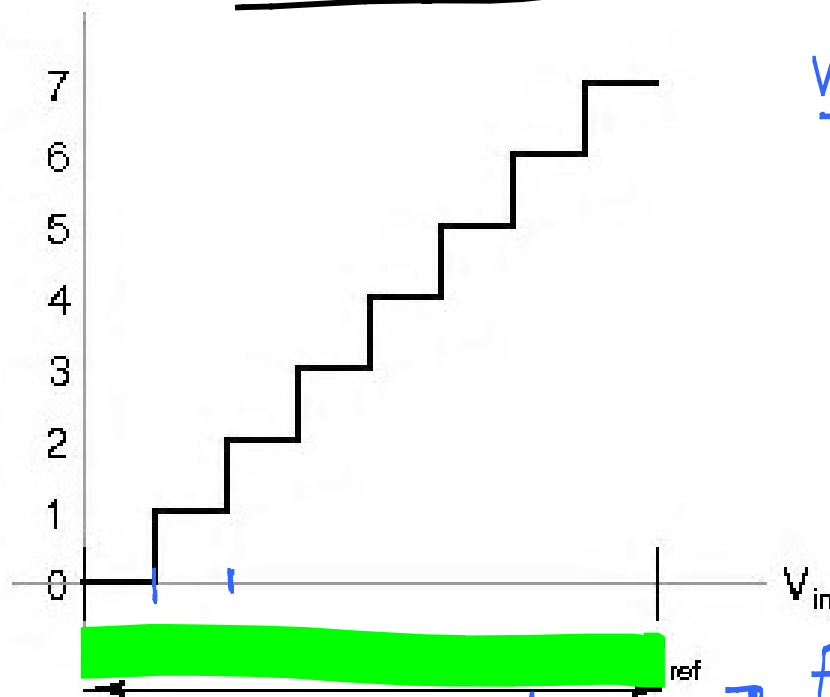
Signal is
on an FFT
bin

Quantization



Quantization

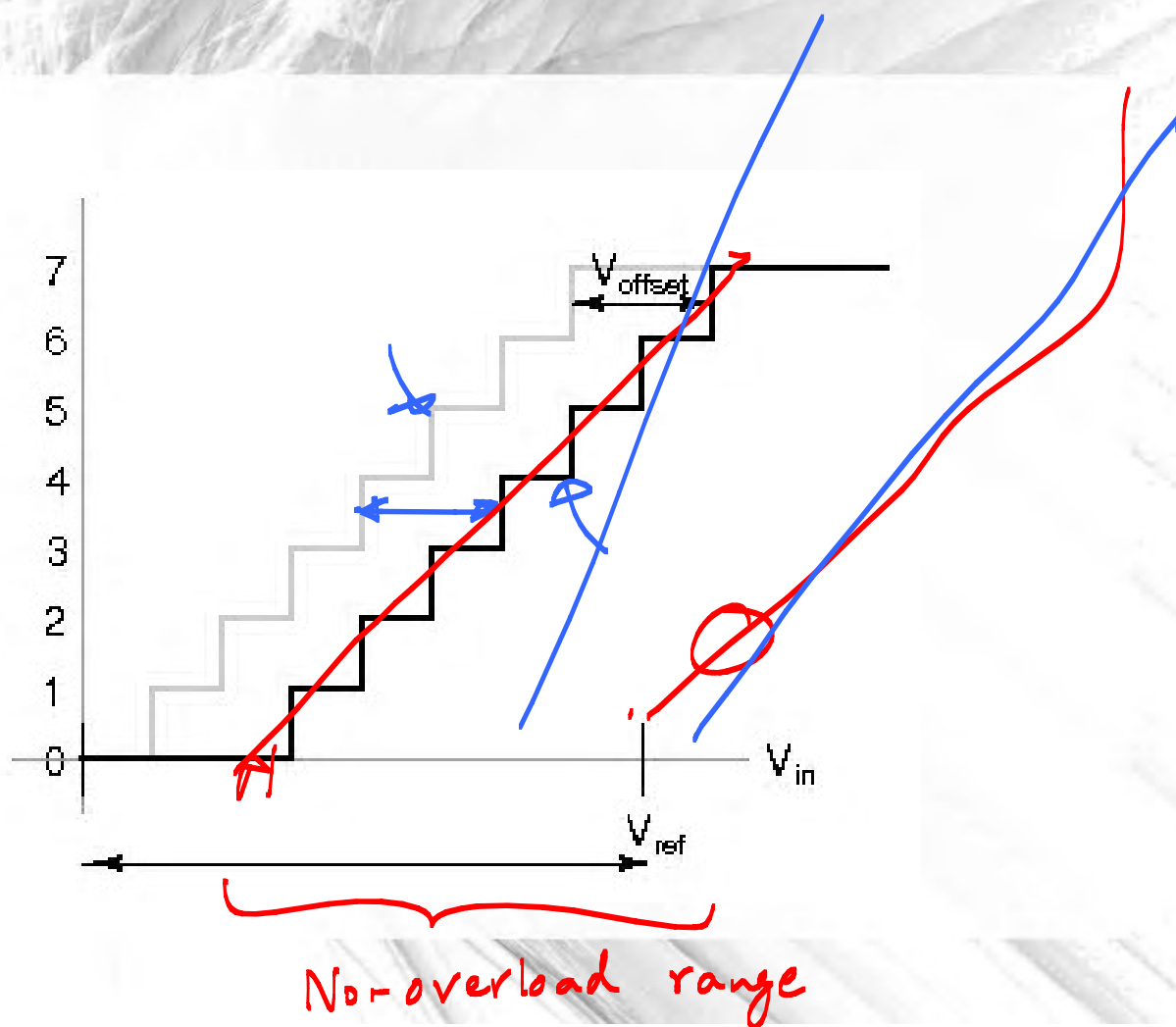
Code
3 bit
quantizer

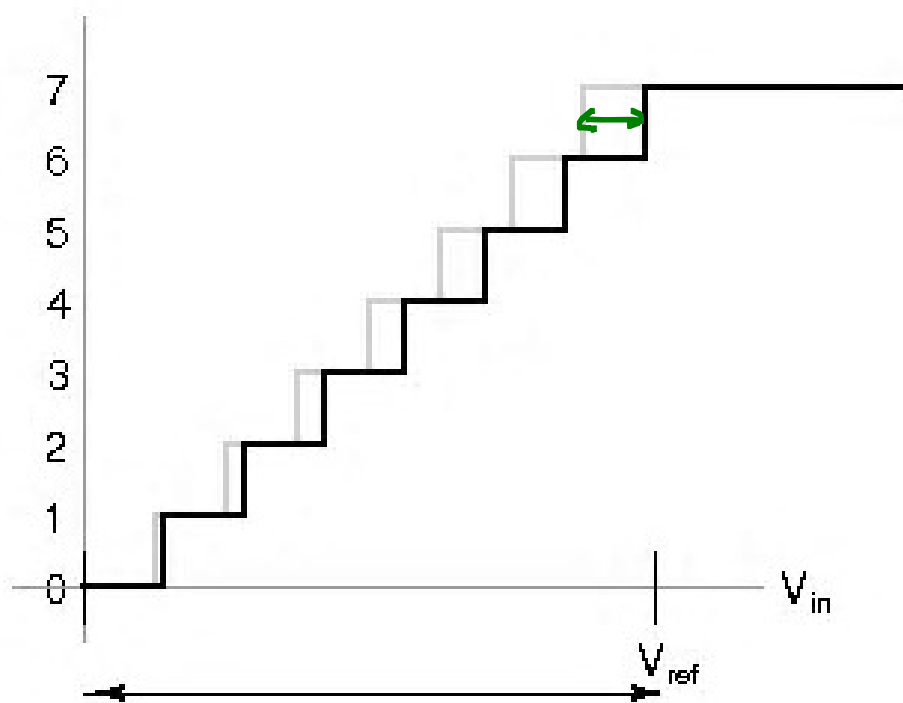


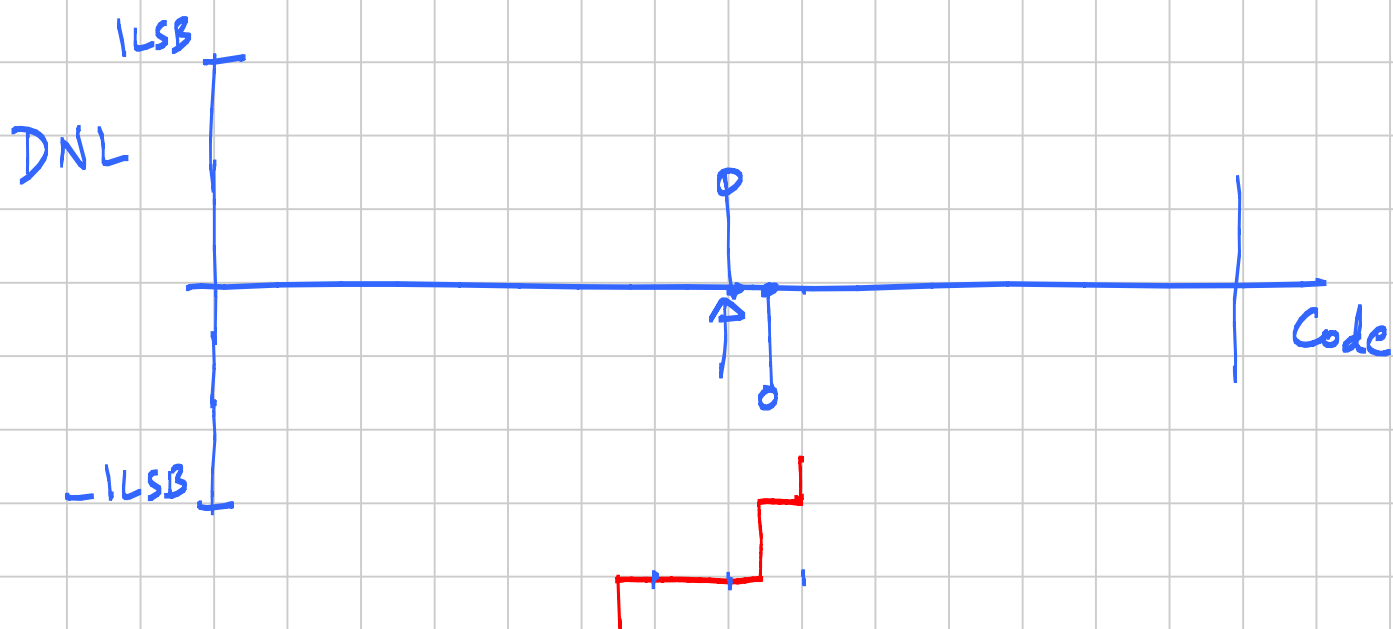
$\frac{V_{ref}}{8} \rightarrow$
Step
Size

Full scale
of the ADC

Code



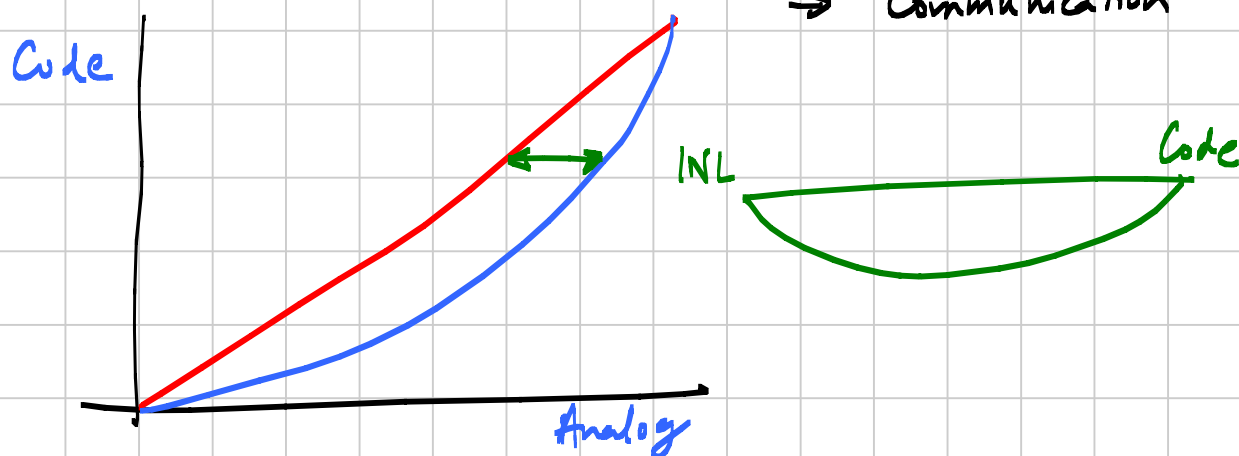




If $|DNL| < 1 \rightarrow$ Monotonic characteristic

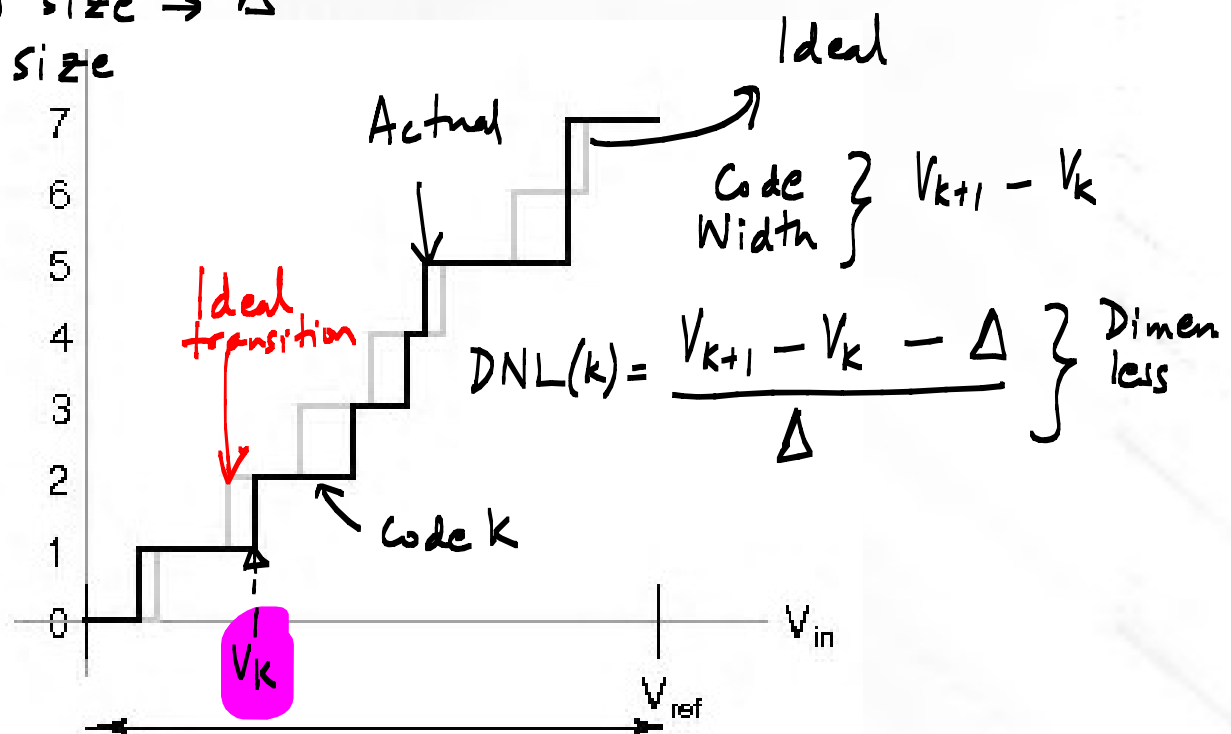
DNL important, INL is not $\rightarrow$ Displays

INL important, DNL is not AS important $\rightarrow$ Communication



VLSI Data Conversion Circuits: Lecture 15

Step size $\rightarrow \Delta$
LSB size



Integral Nonlinearity

Ideal transition to code "k" = $k\Delta$

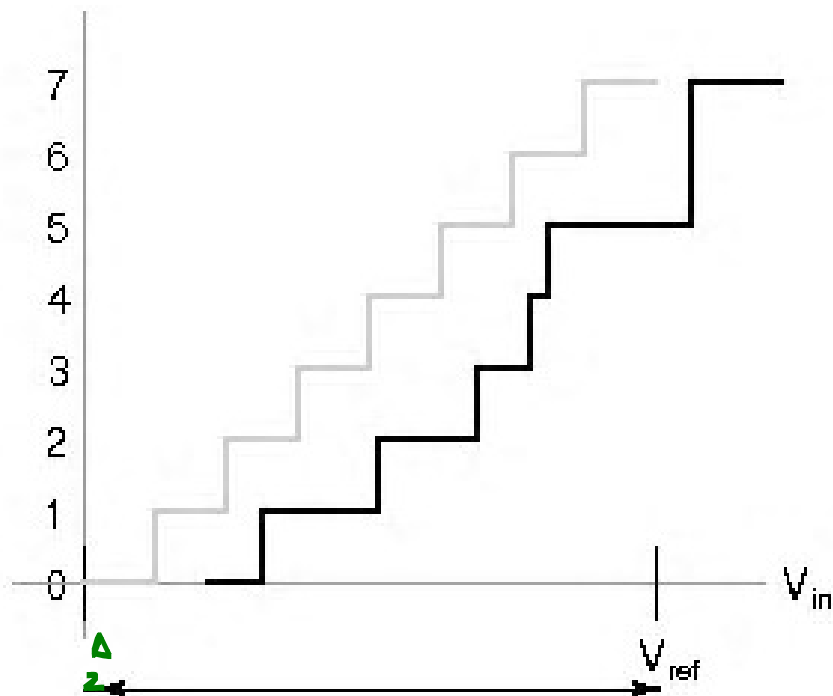
Actual transition = V_k

$$\frac{(\text{Actual transition}) - k\Delta}{\Delta} = \text{Integral nonlinearity } INL(k)$$

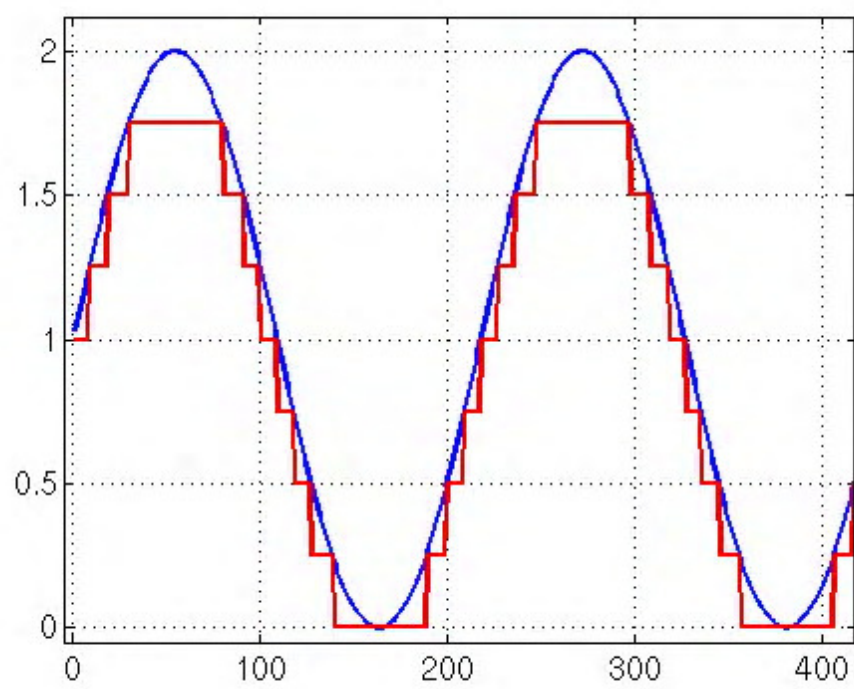
$$INL(k) = \frac{V_k - k\Delta}{\Delta}$$

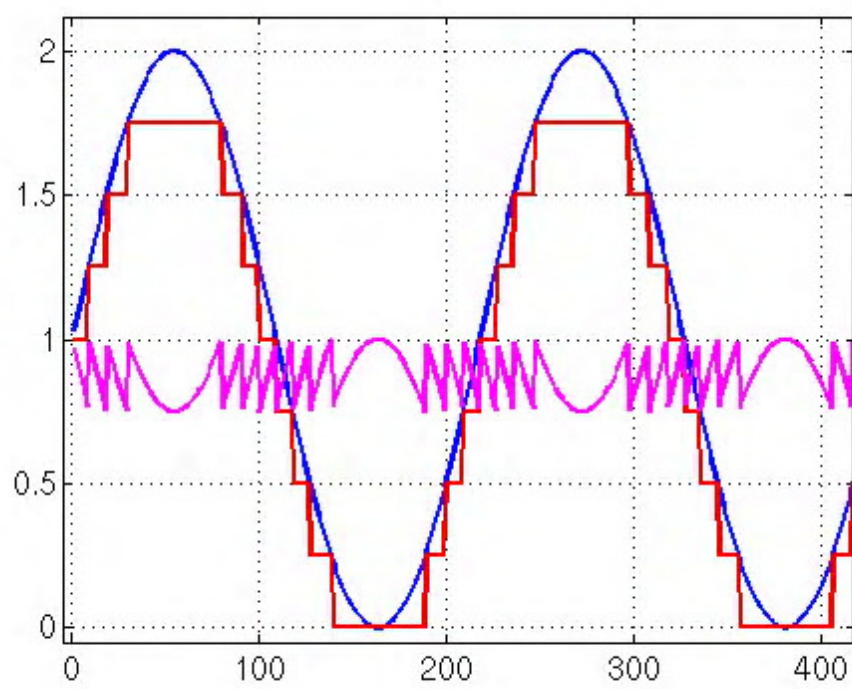
$$INL(k+1) = \frac{V_{k+1} - (k+1)\Delta}{\Delta}$$

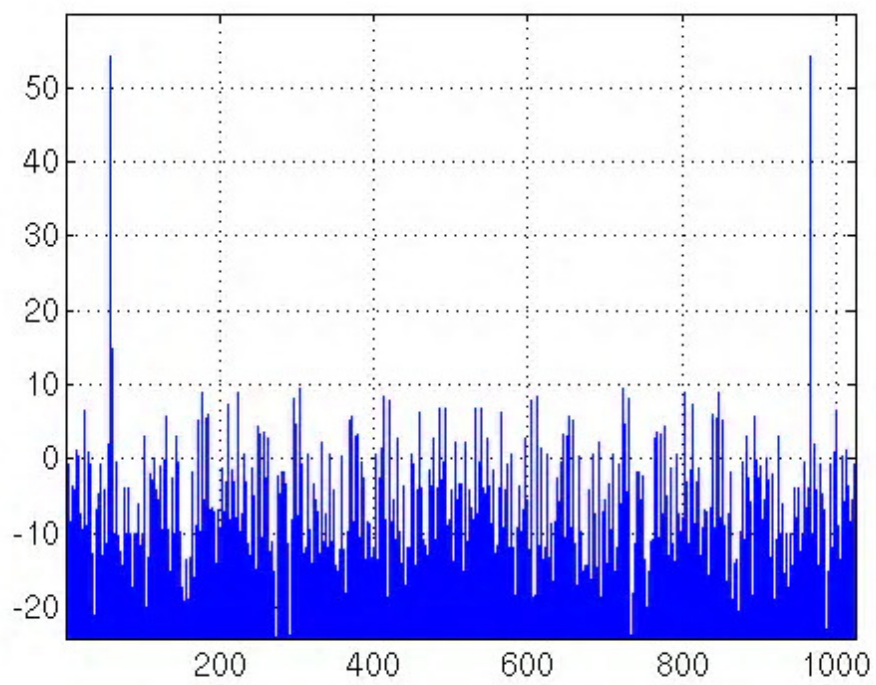
$$INL(k+1) - INL(k) = \frac{V_{k+1} - V_k - \Delta}{\Delta} = DNL(k)$$



* Remove Gain & Offset errors







Lecture 16

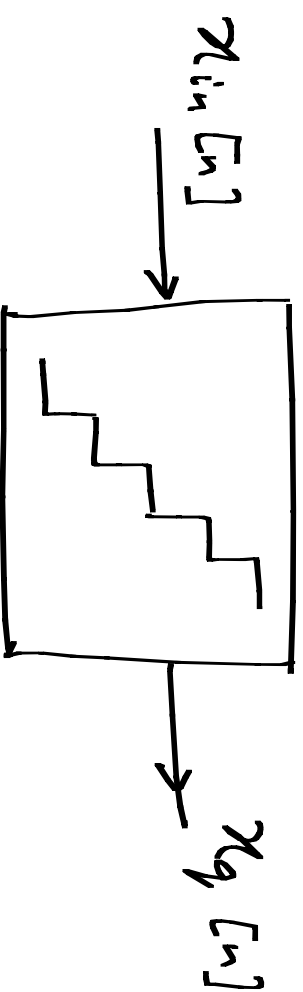
VLSI Data Conversion Circuits

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January 24, 2011

(i) Spectral properties of quantized signals



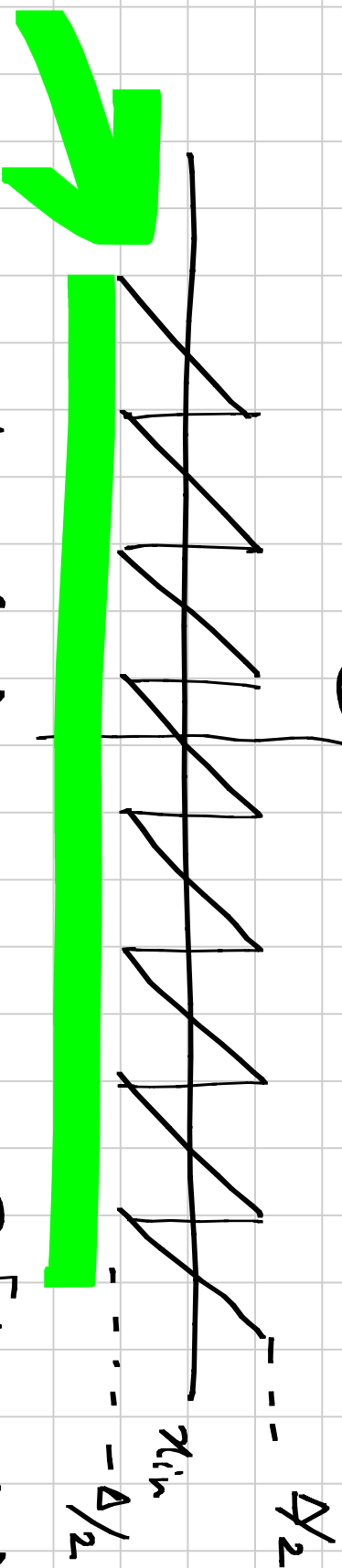
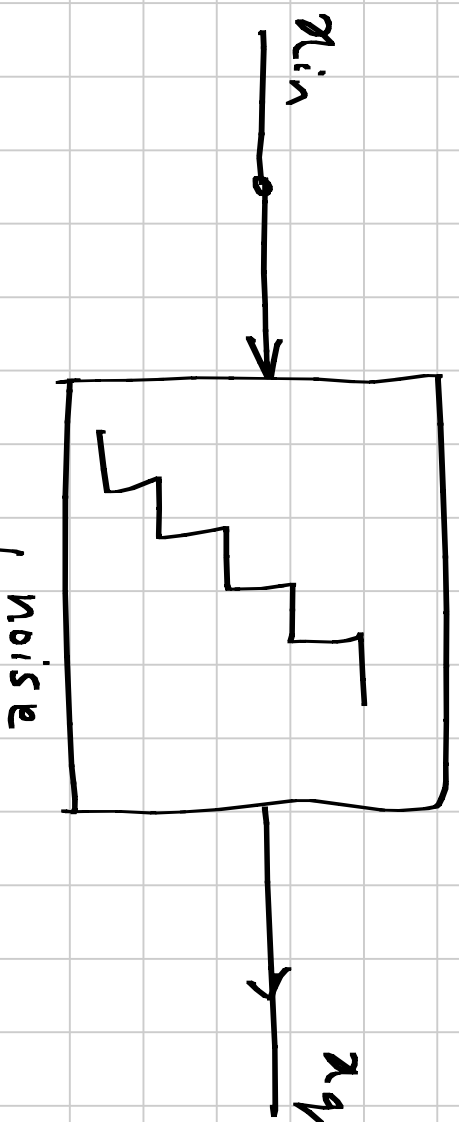
* If the quantizer is NOT overloaded,

Step : Δ

* Quantization error is deterministic

$x_q - x_{in}$ → Quantization error

Bounded $[-\frac{\Delta}{2}, \frac{\Delta}{2}]$



$$x_{in} \rightarrow A \cos(\omega t) \quad x_q = Q[A \cos(\omega t)]$$

$$x_q = x_{in} + \{\text{Error}\}$$

(i) Q. error as "noise"

(ii) Noise is independent of the input

(iii) Error is uniformly distributed between $[-\Delta/2, \Delta/2]$

$$SQNR = 6.02 N - 1.76$$

$$SQNR \text{ in dB} = 6.02 N + 1.76 \text{ dB}$$

Increase N by 1 bit

→ LSB size ↓ 2 → Q. noise power ↓ 4 = 6 dB

Sinusoid

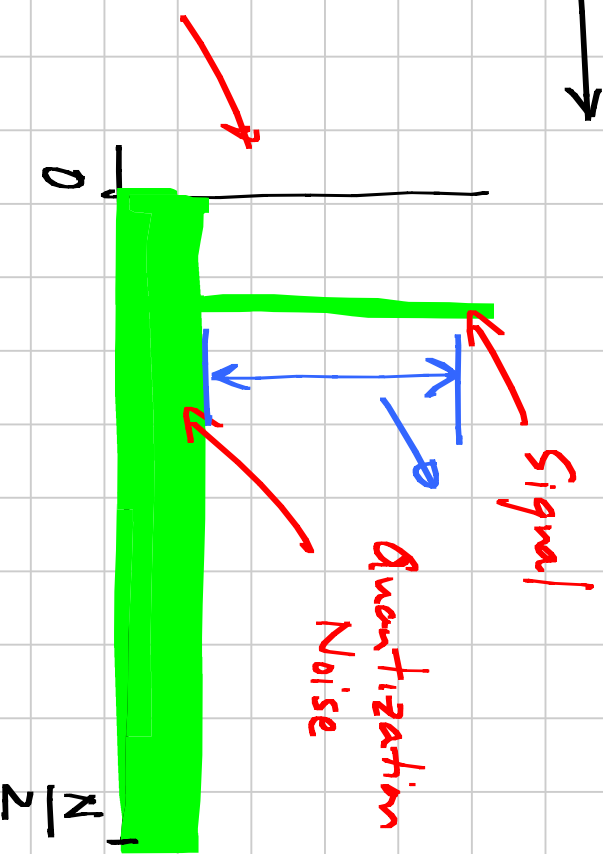


FFT

Effective Number of Bits

ENOB

$$\frac{SQNR_{\text{actual}} - 1.76}{6.02}$$



(iv) Noise is independent from sample to sample
→ white noise assumption.

Error is uniform in $[-\frac{\Delta}{2}, \frac{\Delta}{2}] \rightarrow \frac{\Delta^2}{12}$ { Variance of the noise

Quantization

N-bit quantizer $\rightarrow 2^N \Delta$

Max. sine wave amplitude $\rightarrow 2^{N-1} \Delta$

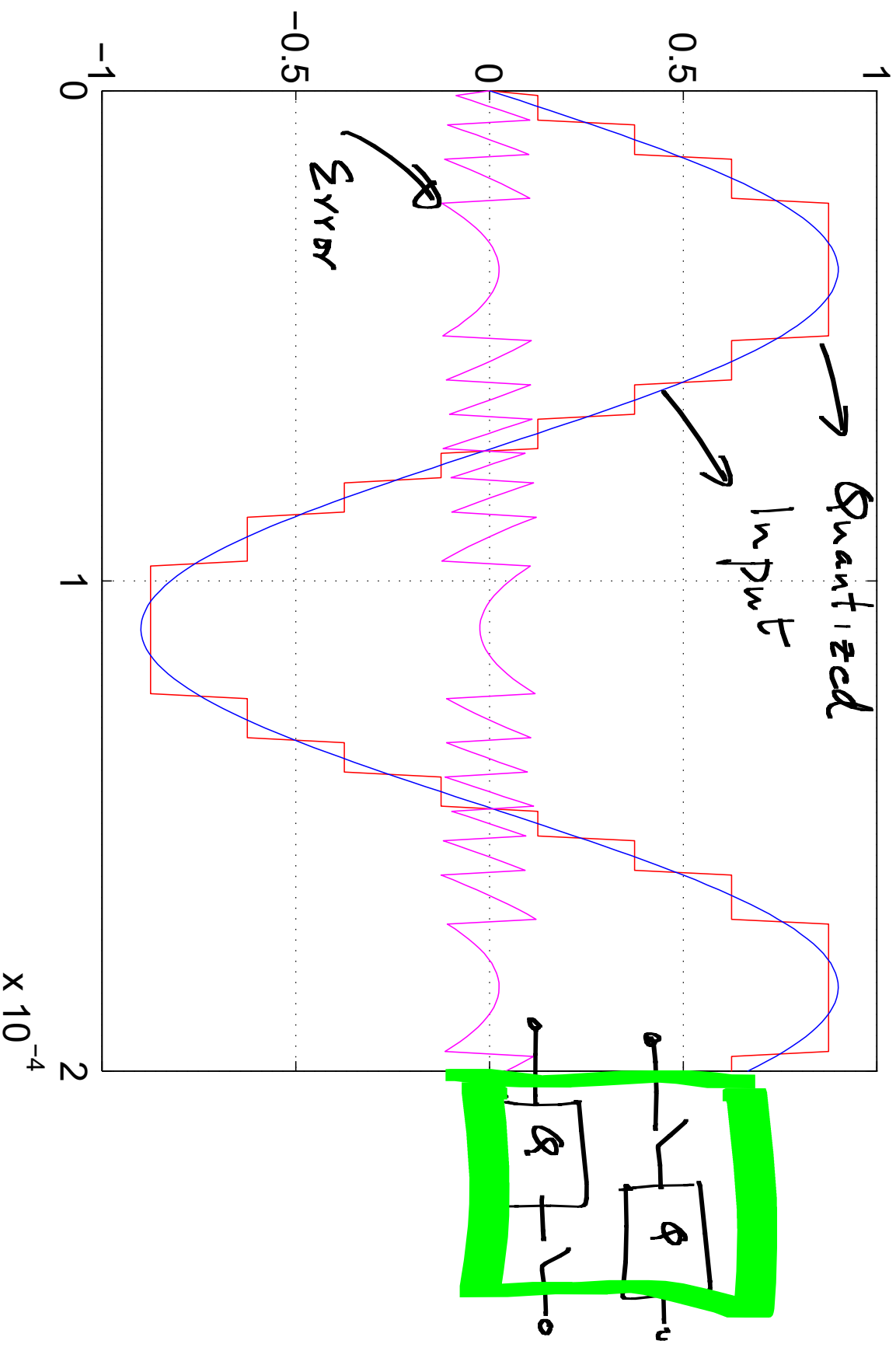
$$\text{Signal power} = \frac{(2^{N-1})^2 \Delta^2}{2}$$

$$\text{Noise power} = \frac{\Delta^2}{12}$$

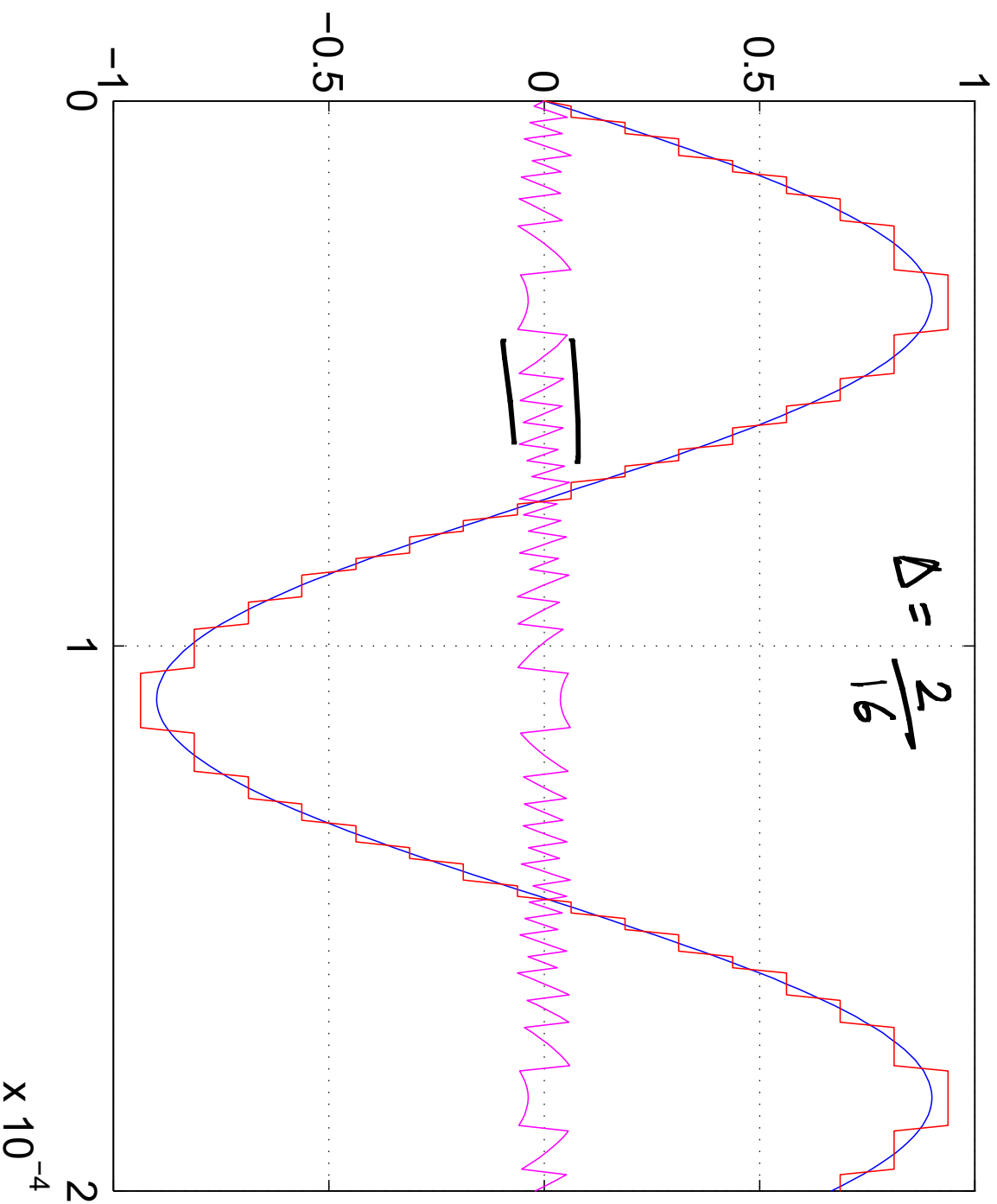
$$\text{SQNR} = \frac{(2^{N-1})^2 \cdot 12}{2} = 6 \cdot 2^{2N-2}$$

Sinusoid : Amplitude = 0.9, step size = 0.25

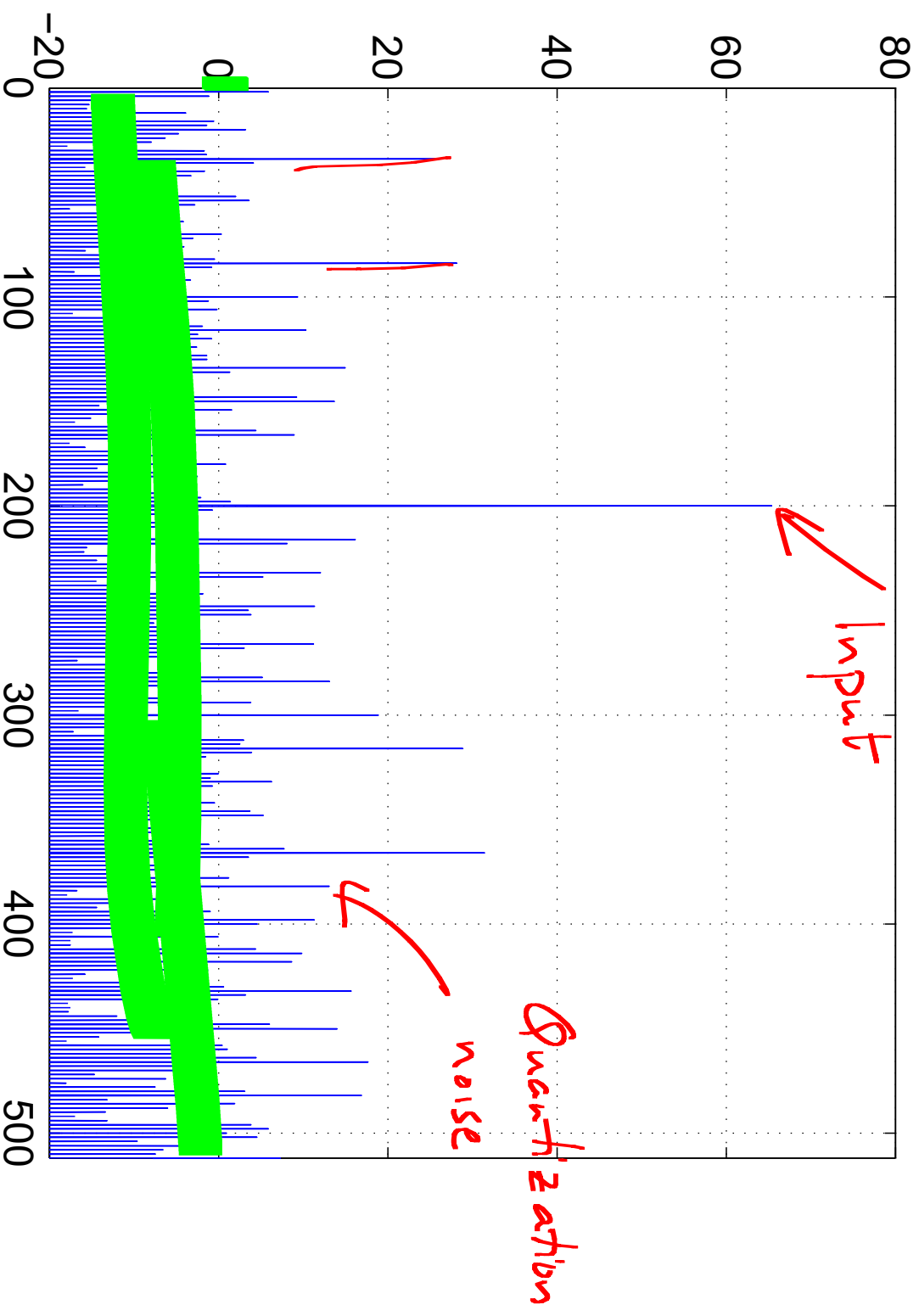
$$\Delta = \frac{2}{8}$$



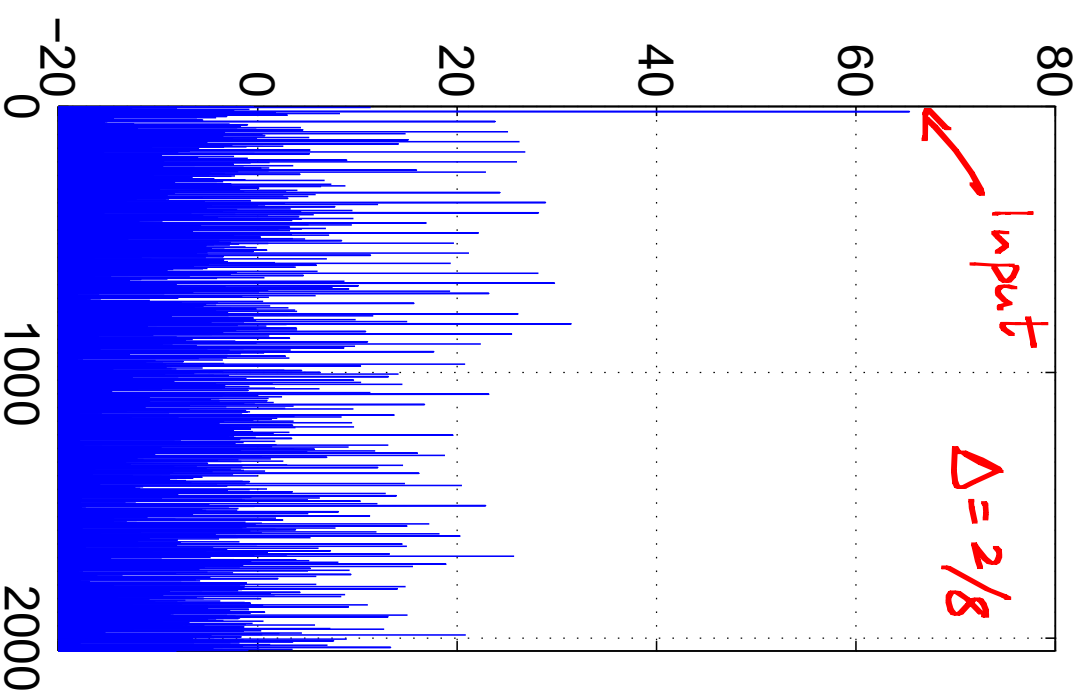
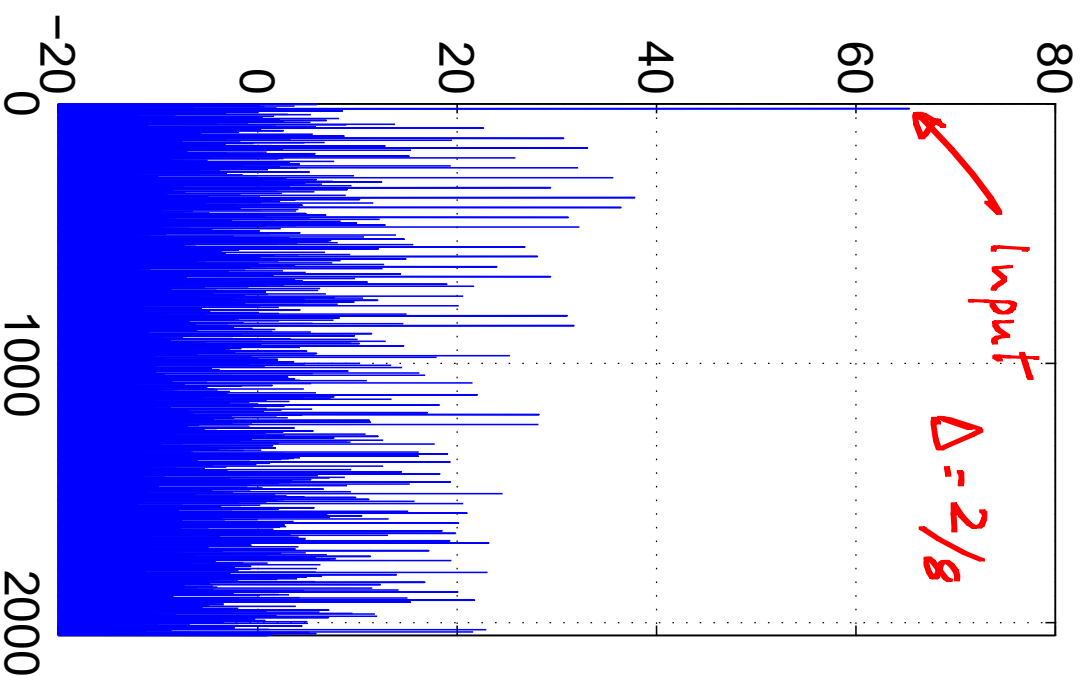
Sinusoid : Amplitude = 0.9, step size = 0.125



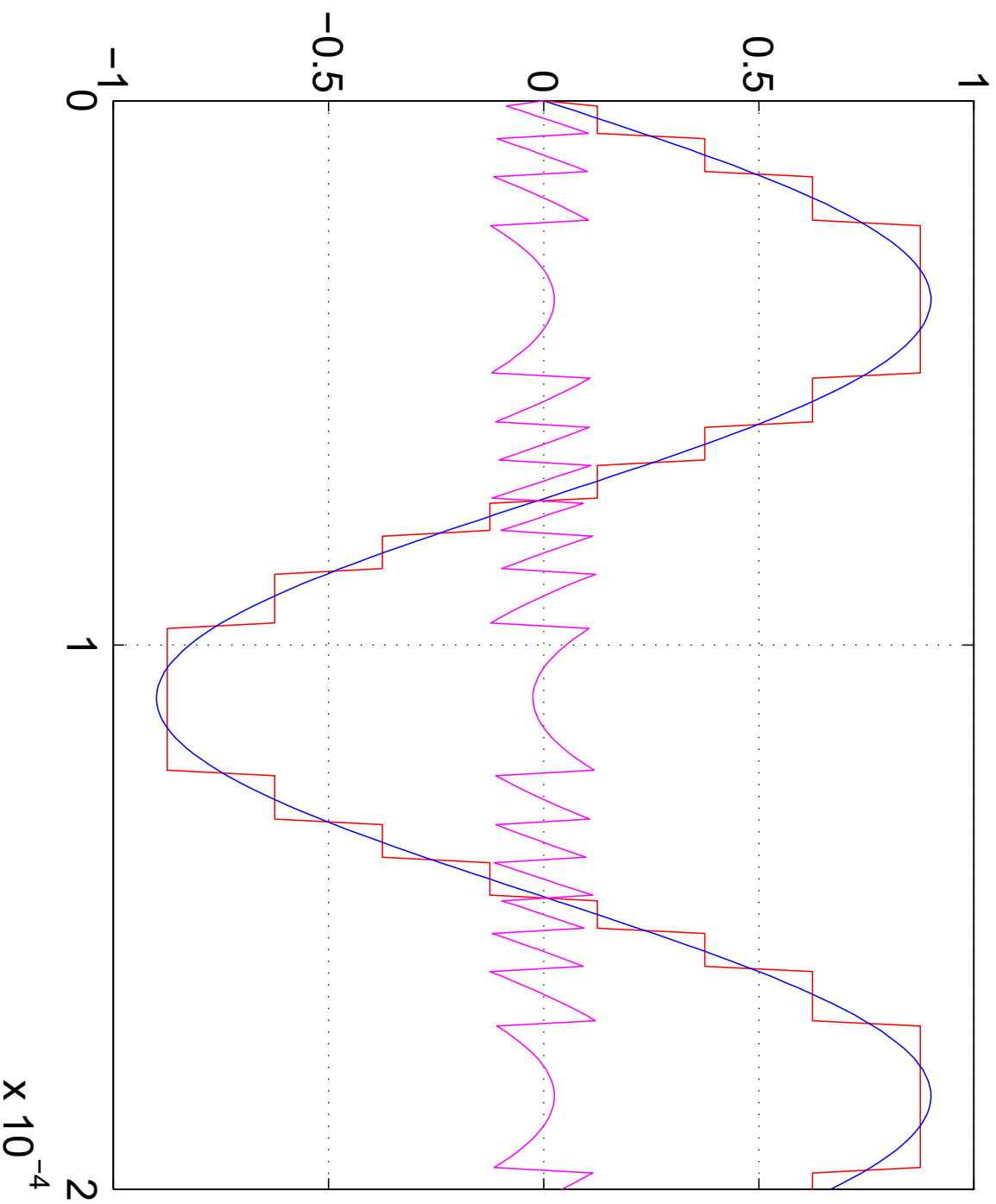
Quantizer Spectrum



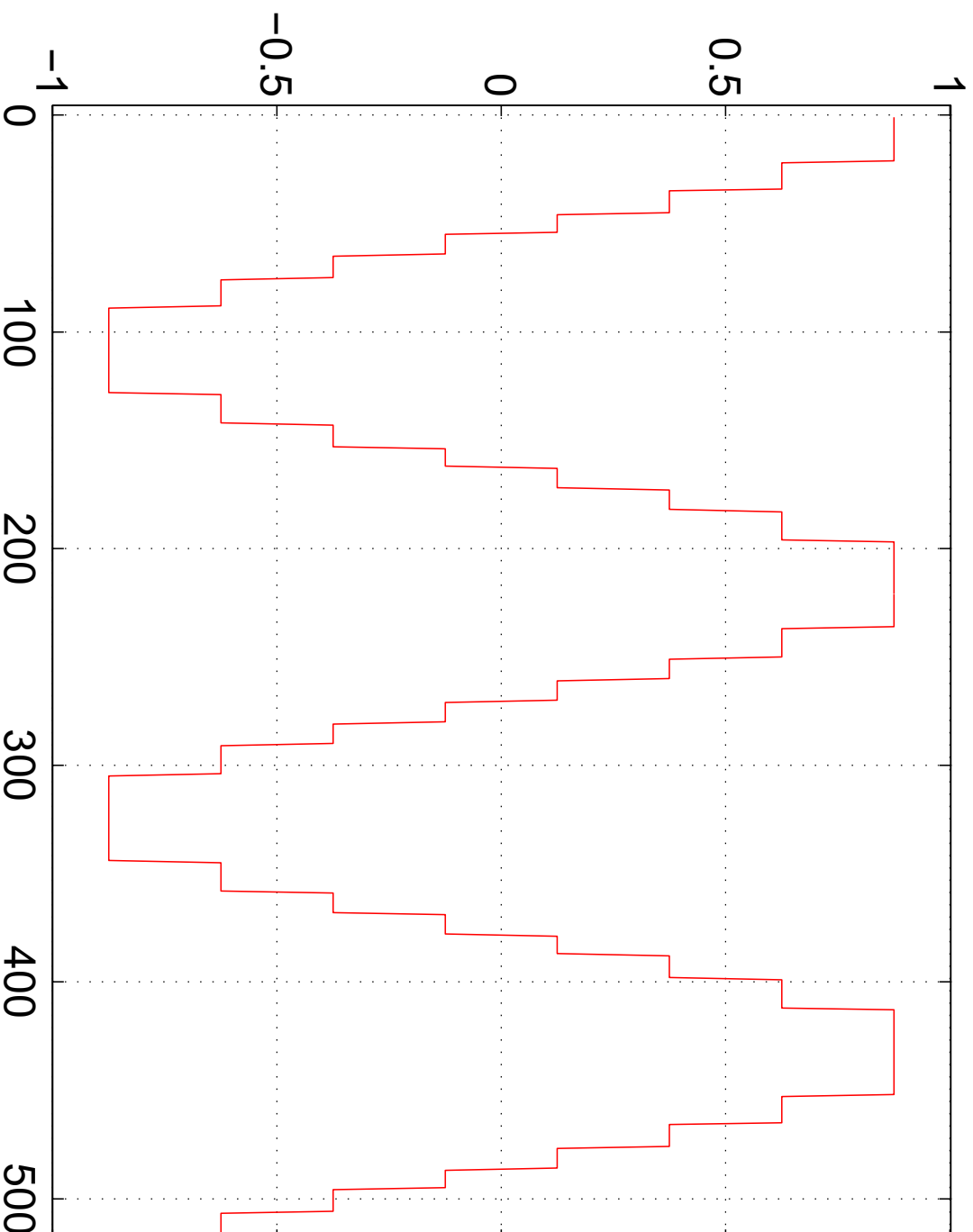
Quantizer Spectrum : $f_{in} = \frac{19}{4096}f_s$, LSB : $2/8$ and $2/16$



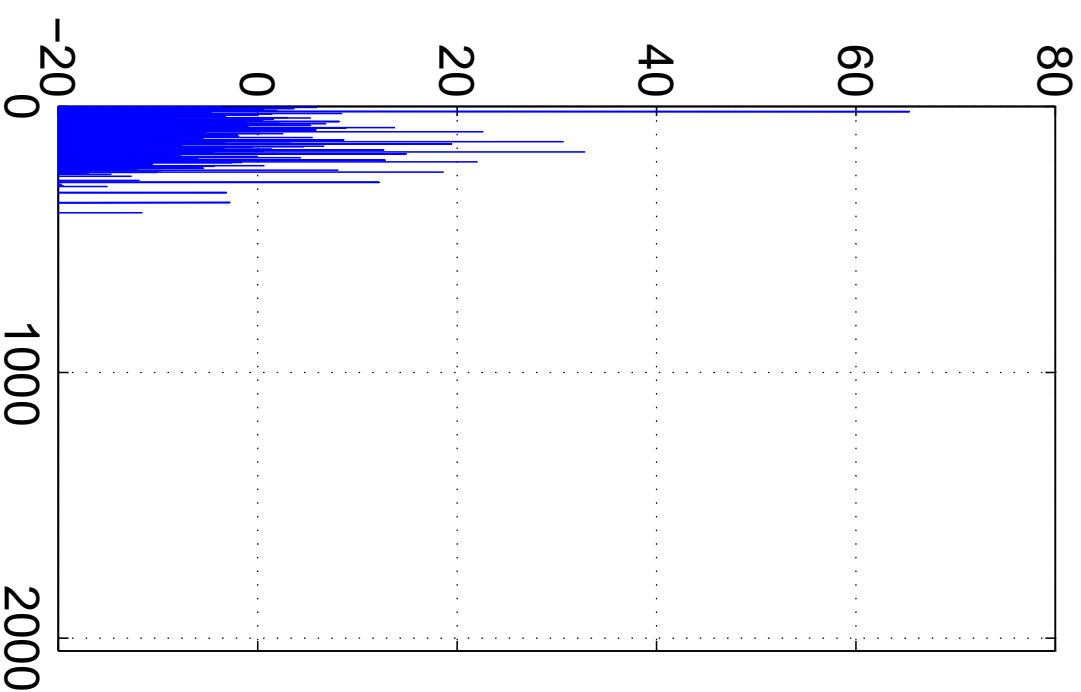
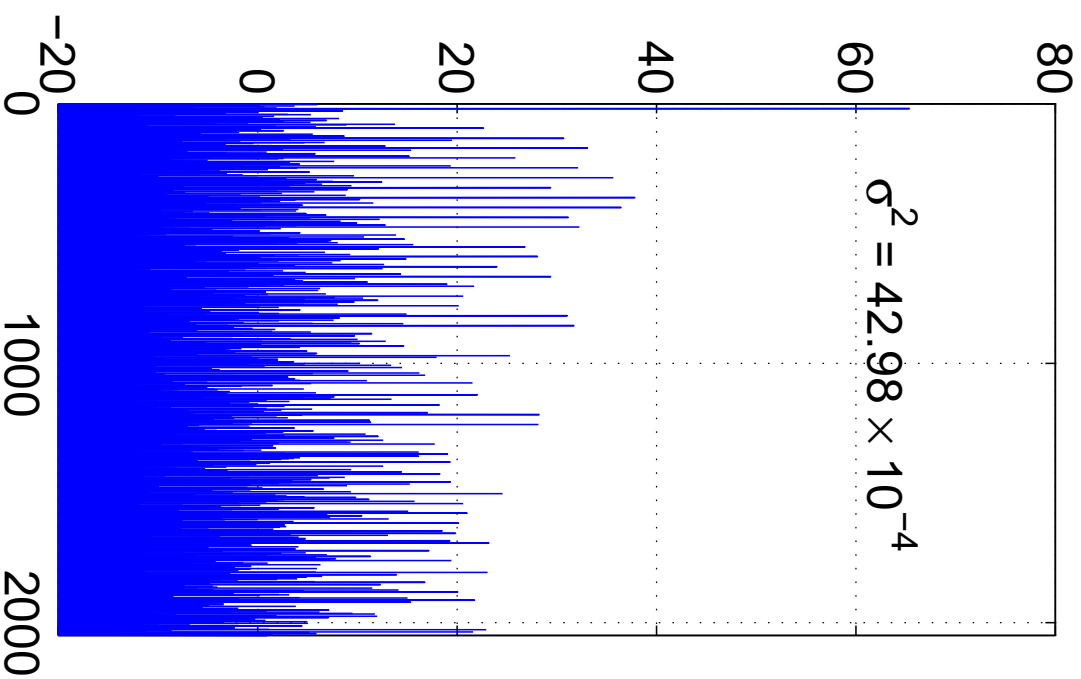
Sinusoid : Amplitude = 0.9, step size = 0.25



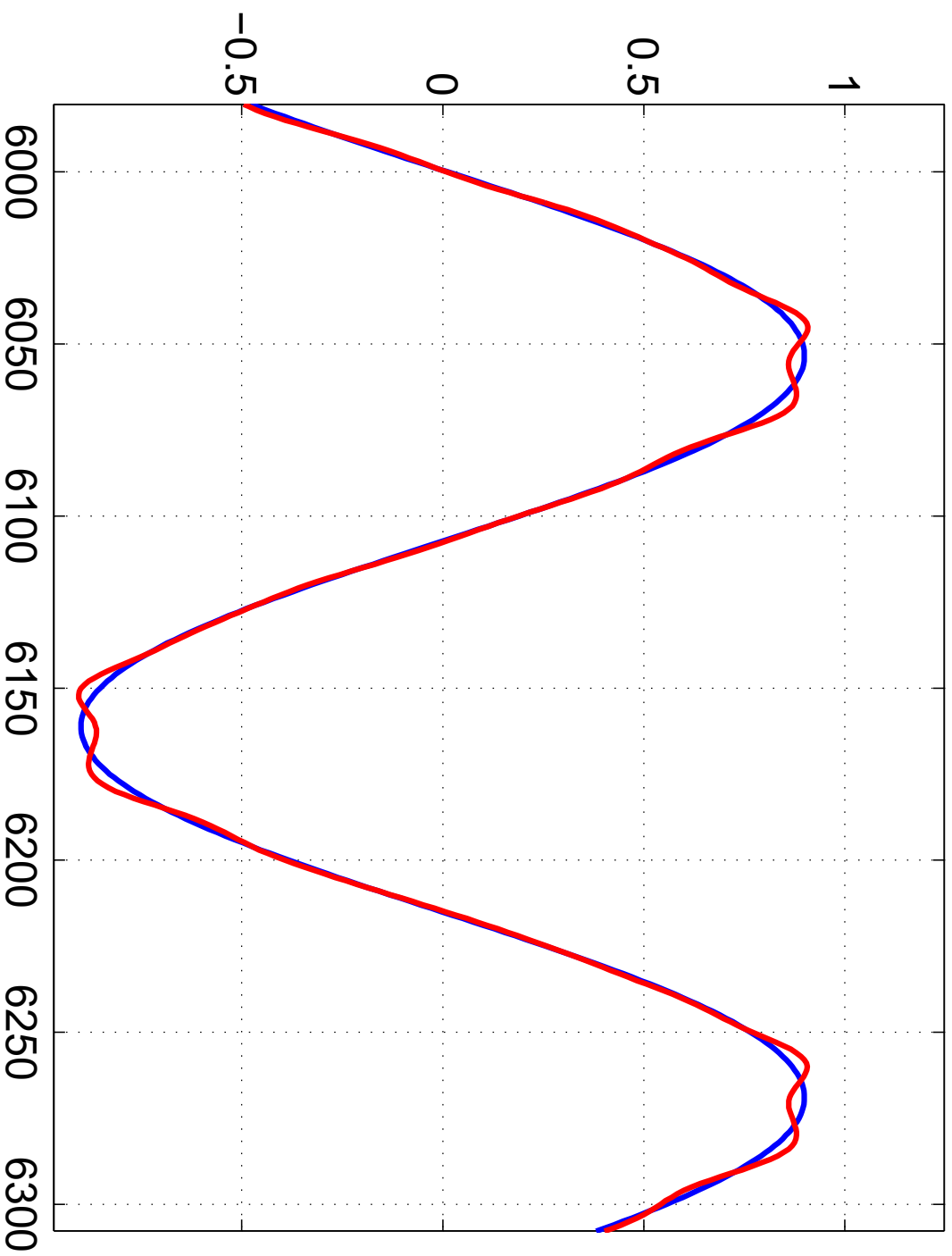
Can you guess the signal ?



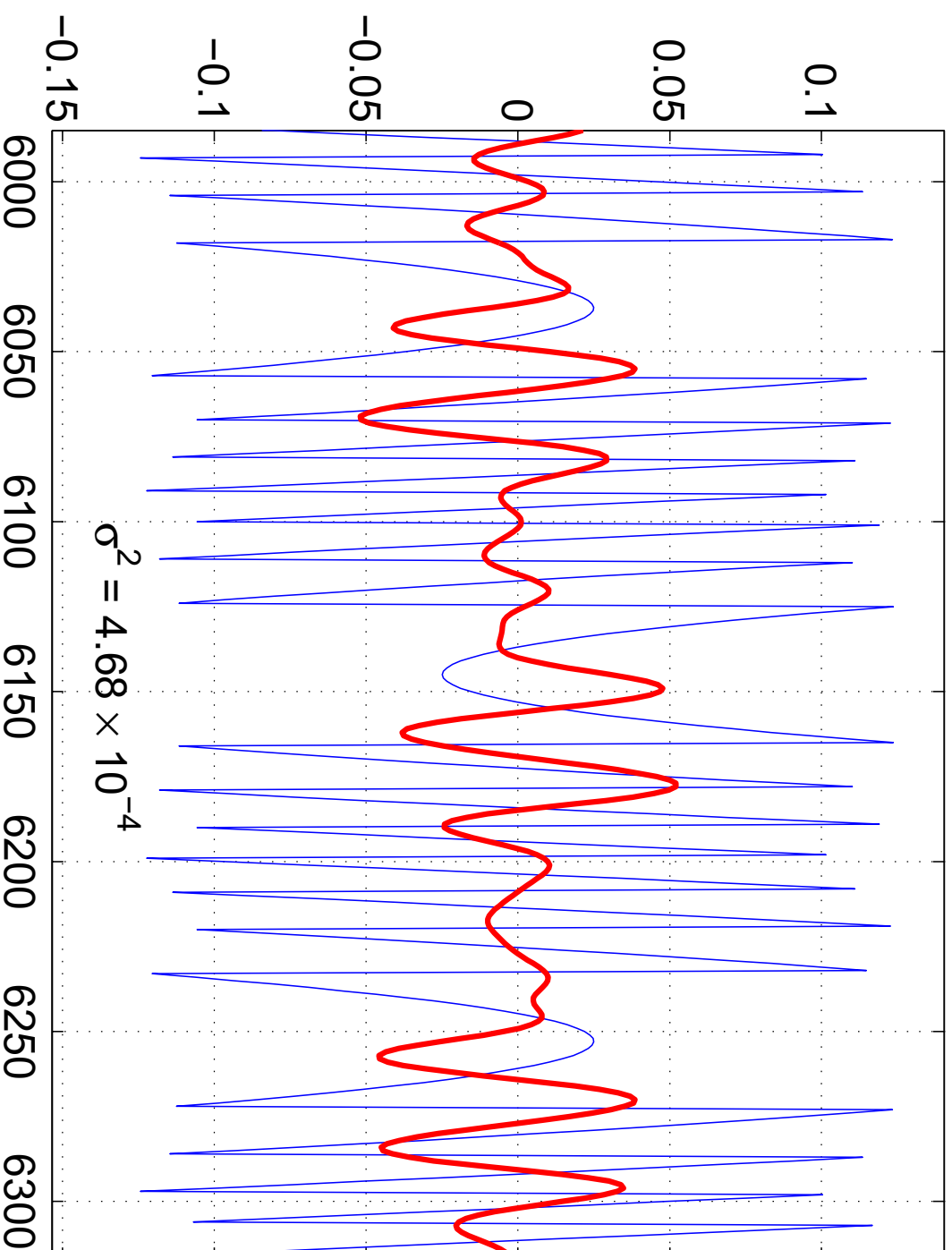
Spectral interpretation



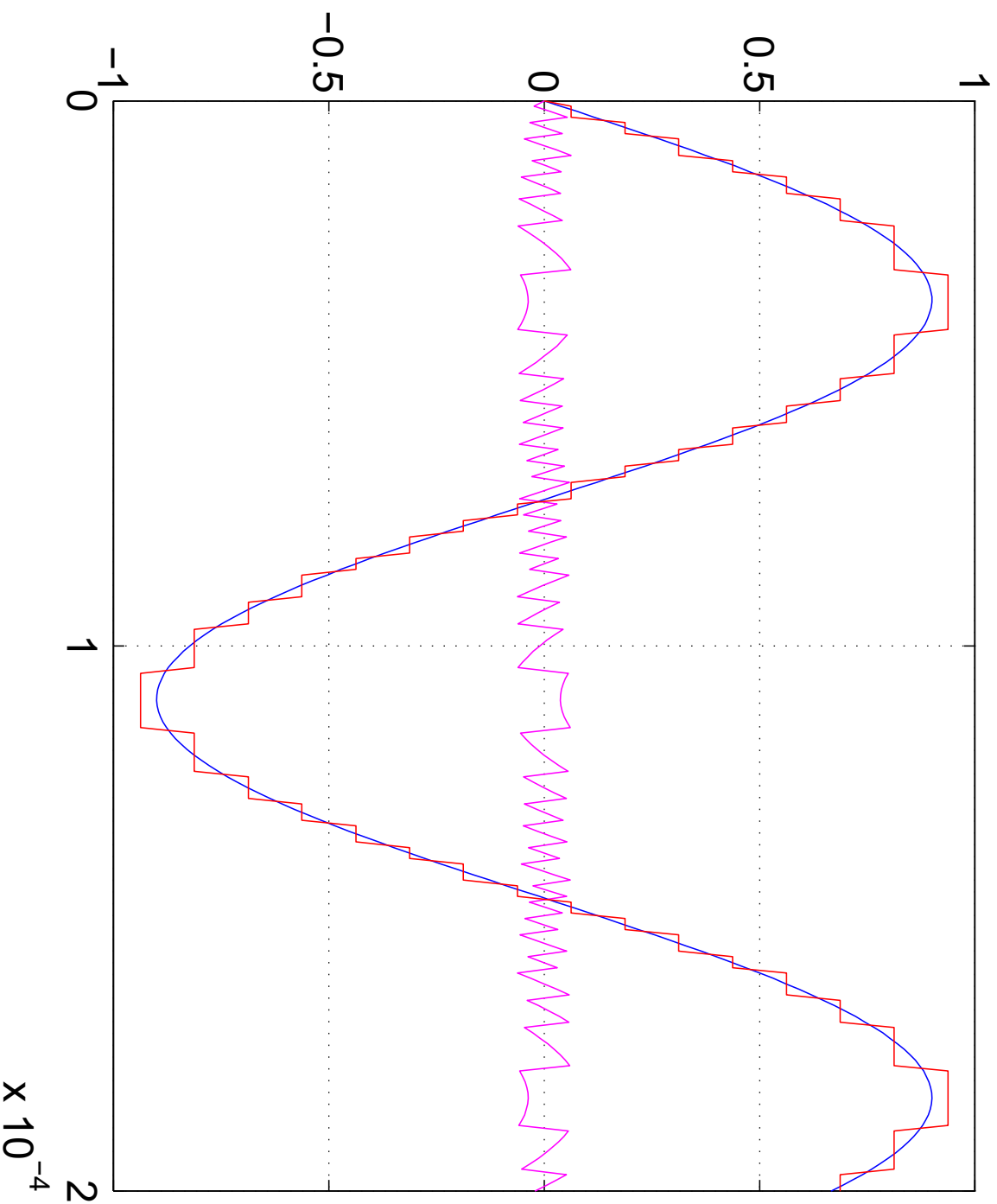
In the time domain



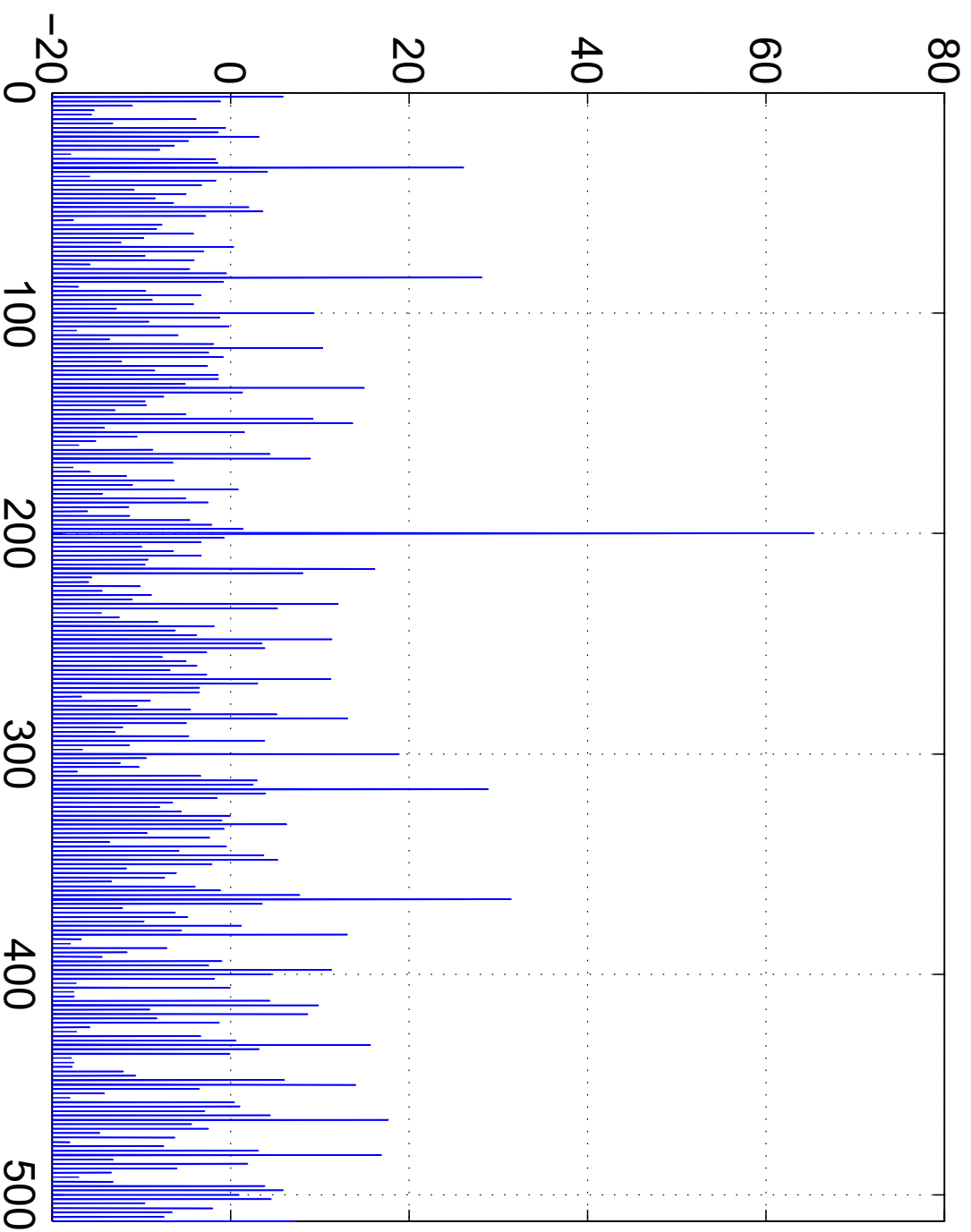
In the time domain



Sinusoid : Amplitude = 0.9, step size = 0.125



Quantizer Spectrum

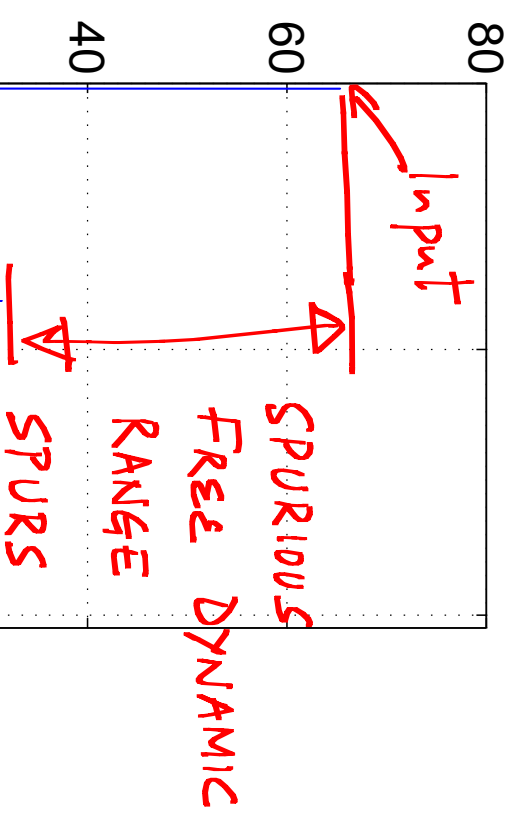
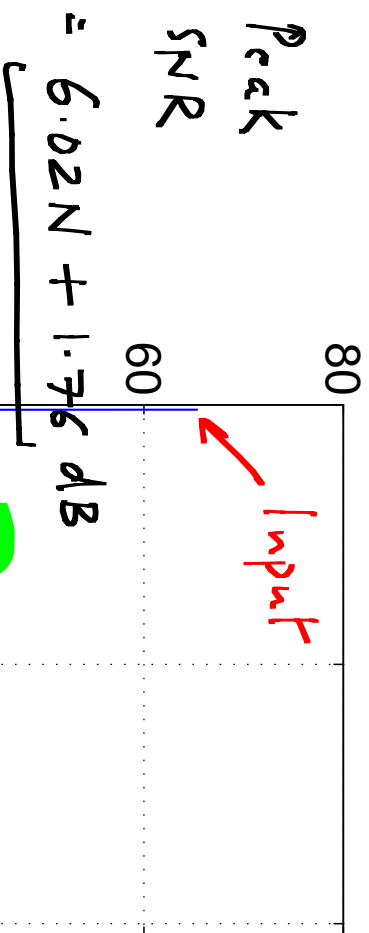


Lecture 17

Quantizer Spectrum : $f_{in} = \frac{19}{4096} f_s$, LSB : 2/8 and 2/16

$$\Delta = 2/8$$

$$\Delta = 2/16$$



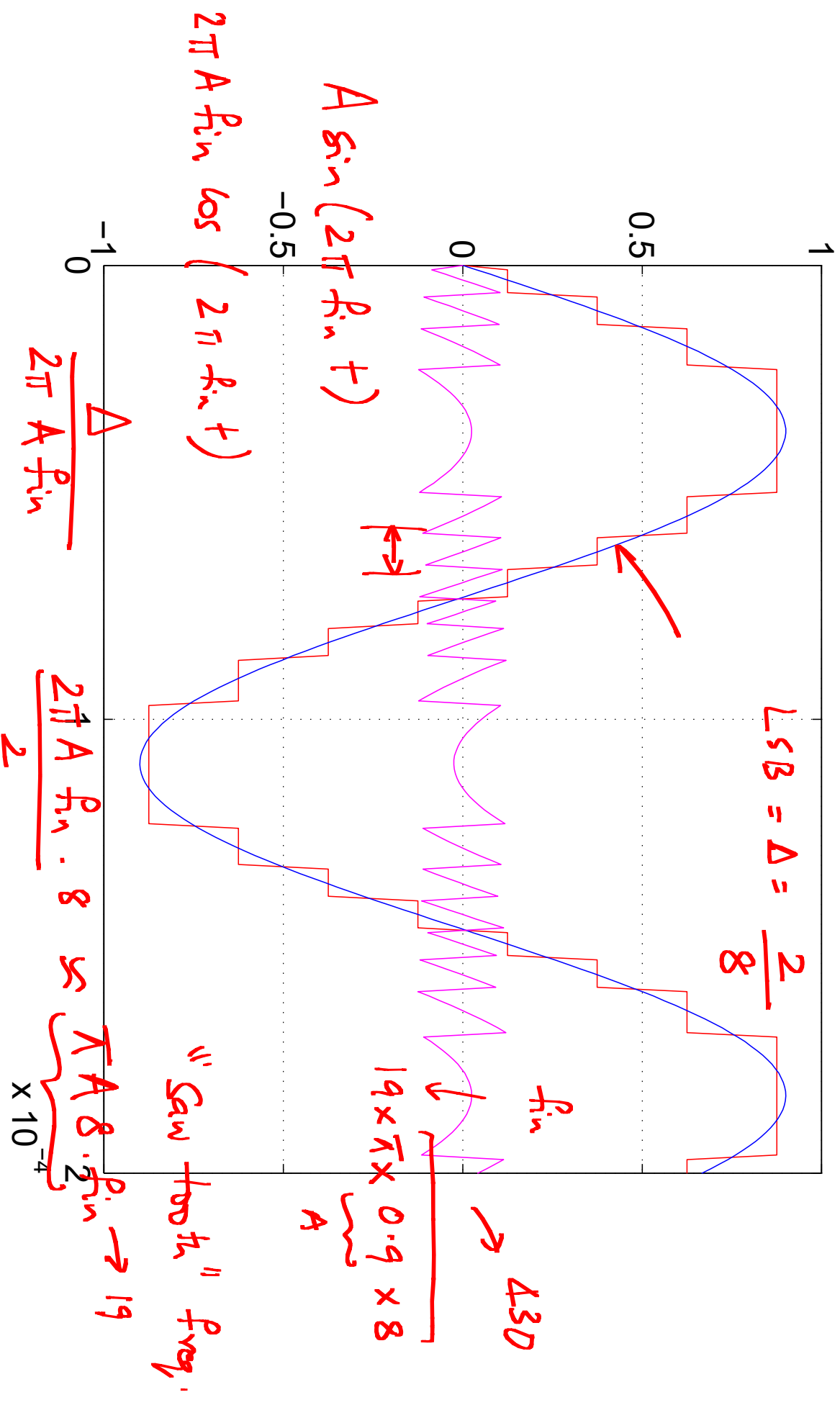
$$6.02N + 1.76 \text{ dB}$$

Dynamic Range (dB) = $10 \log 10$

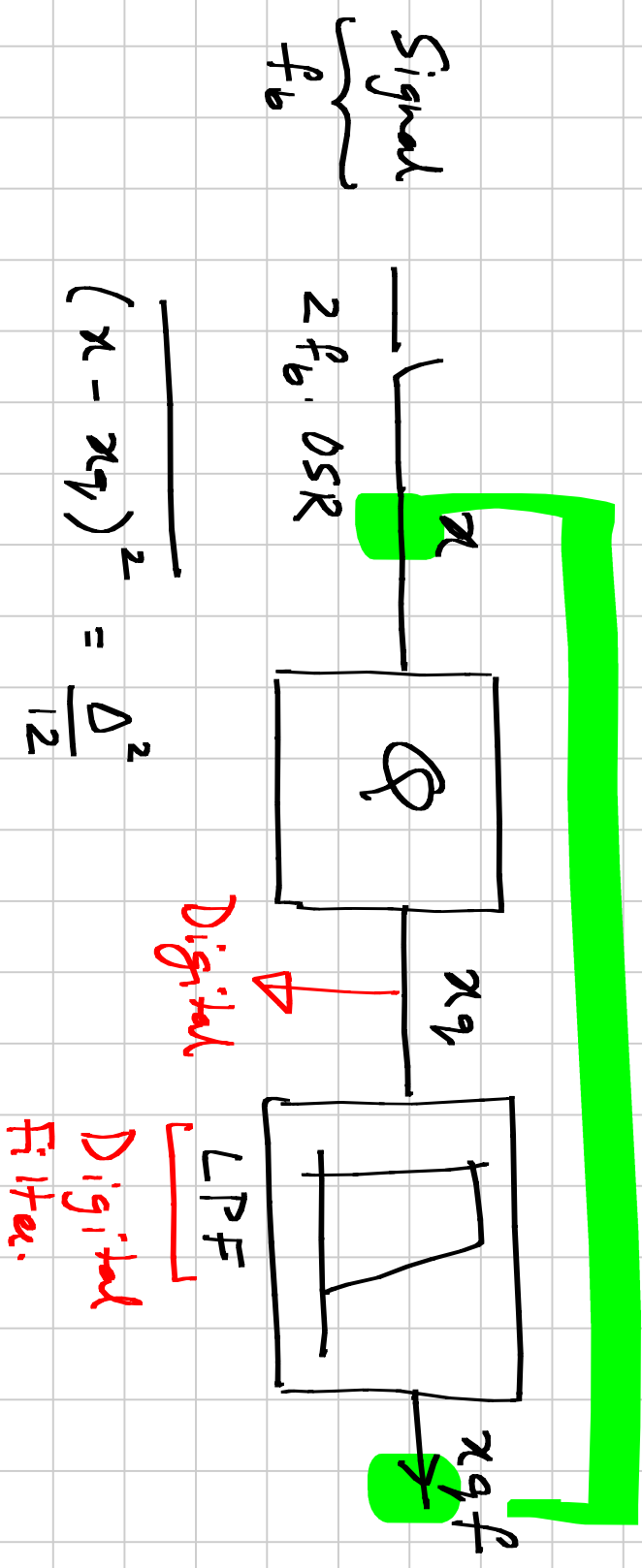
Max. Signal Power

Noise Power

Sinusoid : Amplitude = 0.9, step size = 0.25



Oversampling can reduce quantization error

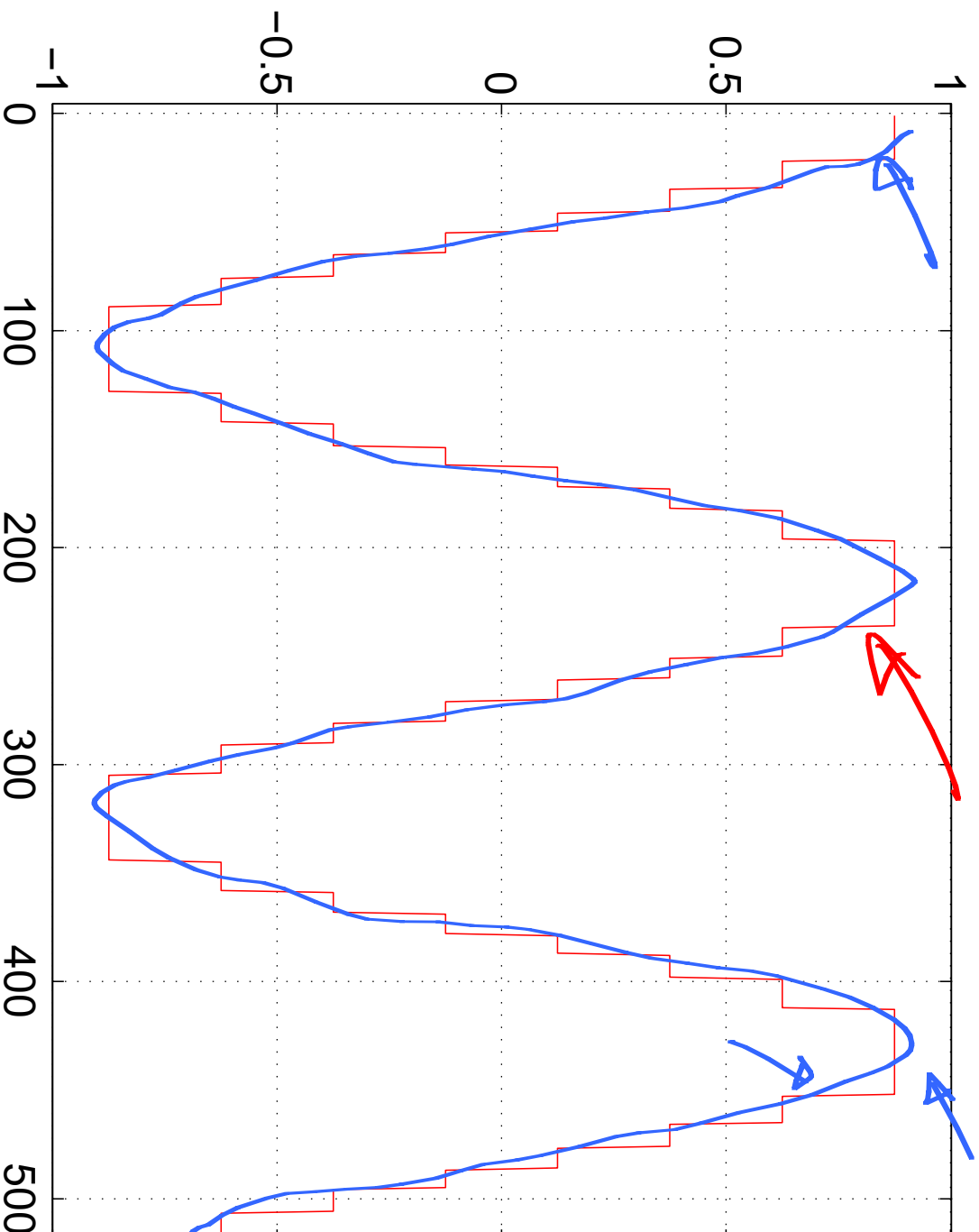


$$\overline{(x - x_q)^2} = \frac{\Delta^2}{12}$$

Can you guess the signal ?

$$\Delta = \frac{2}{8}$$

$$\overline{\sum x^2} = \Delta^2 / 12$$



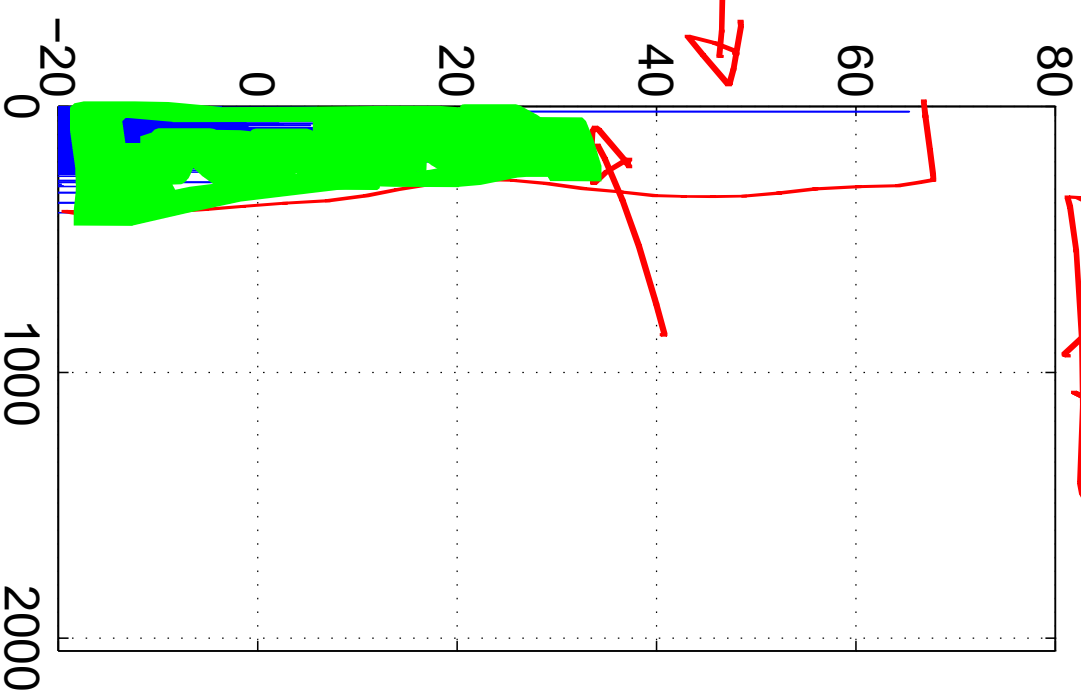
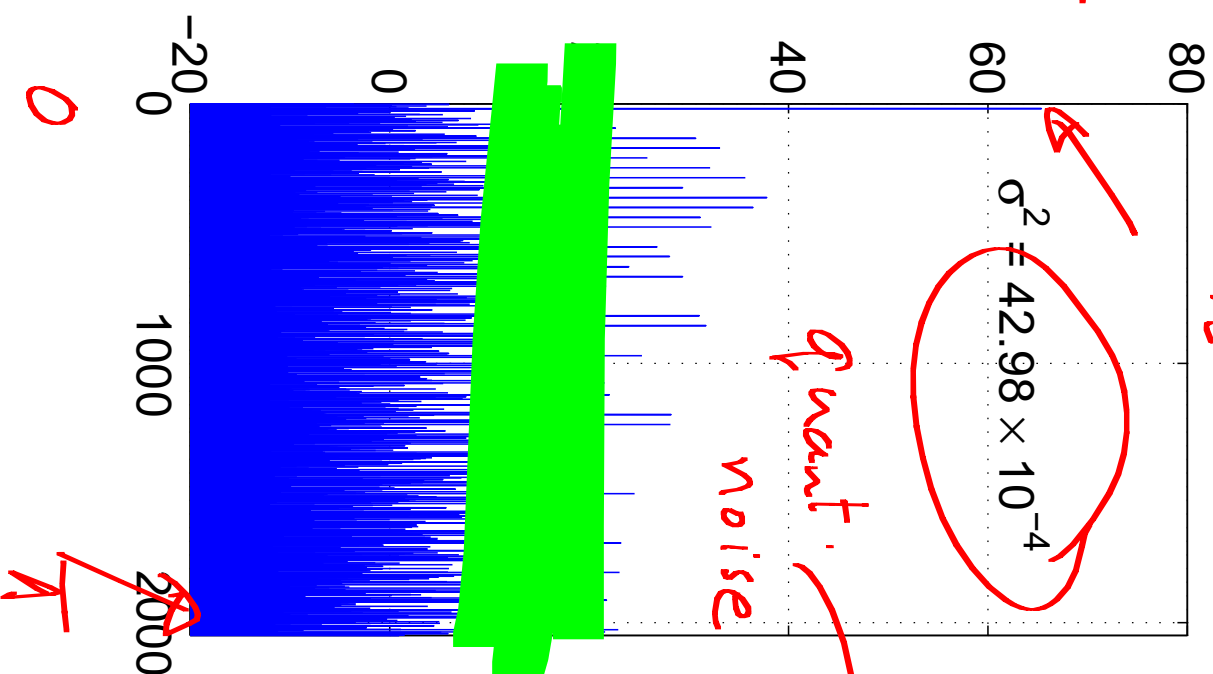
(Samples)

Spectral interpretation

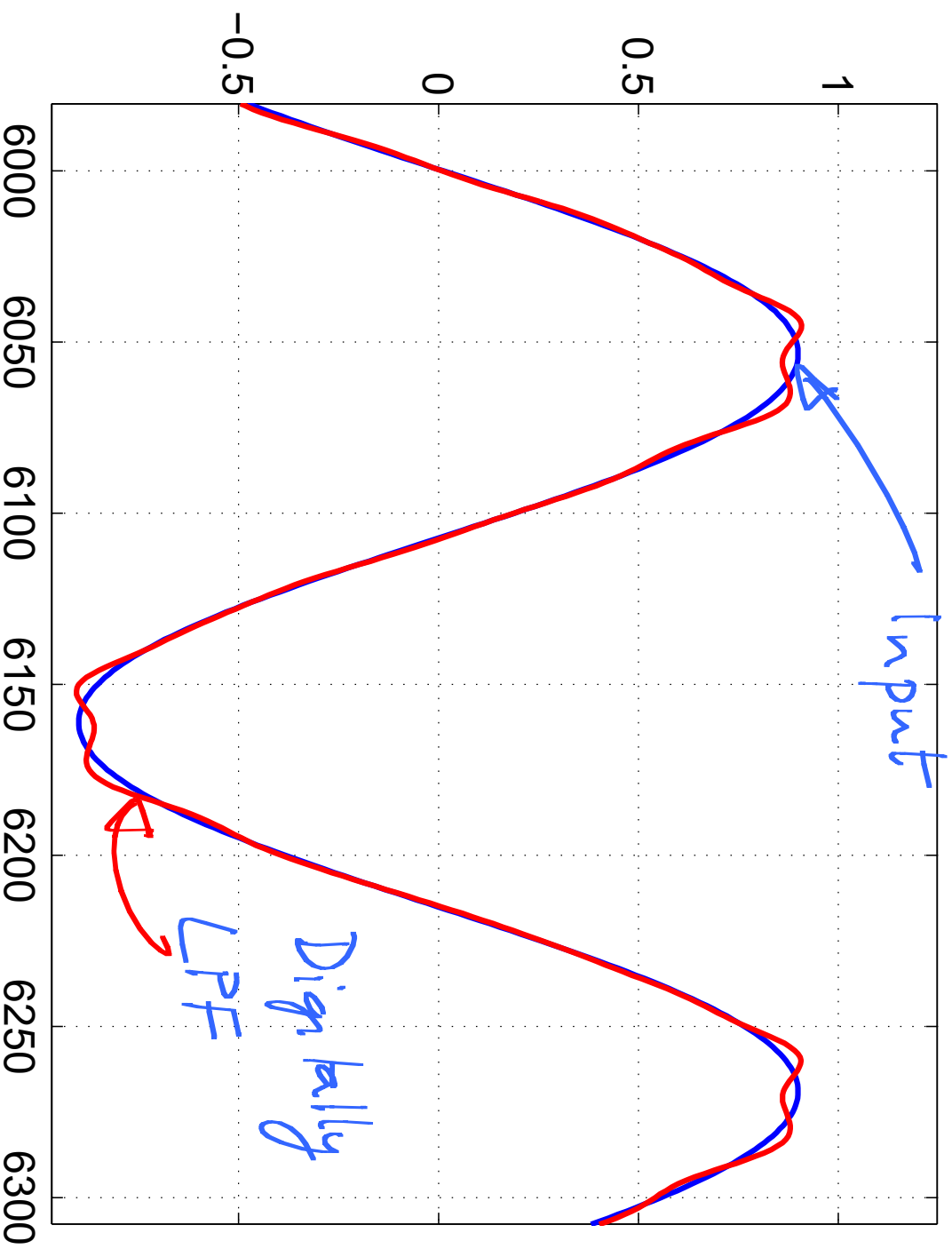
$$f_m/f_s = 19/4096 \rightarrow$$

$$\boxed{\frac{\Delta}{\pi/16}}$$

$$\Delta = \frac{2}{8}$$

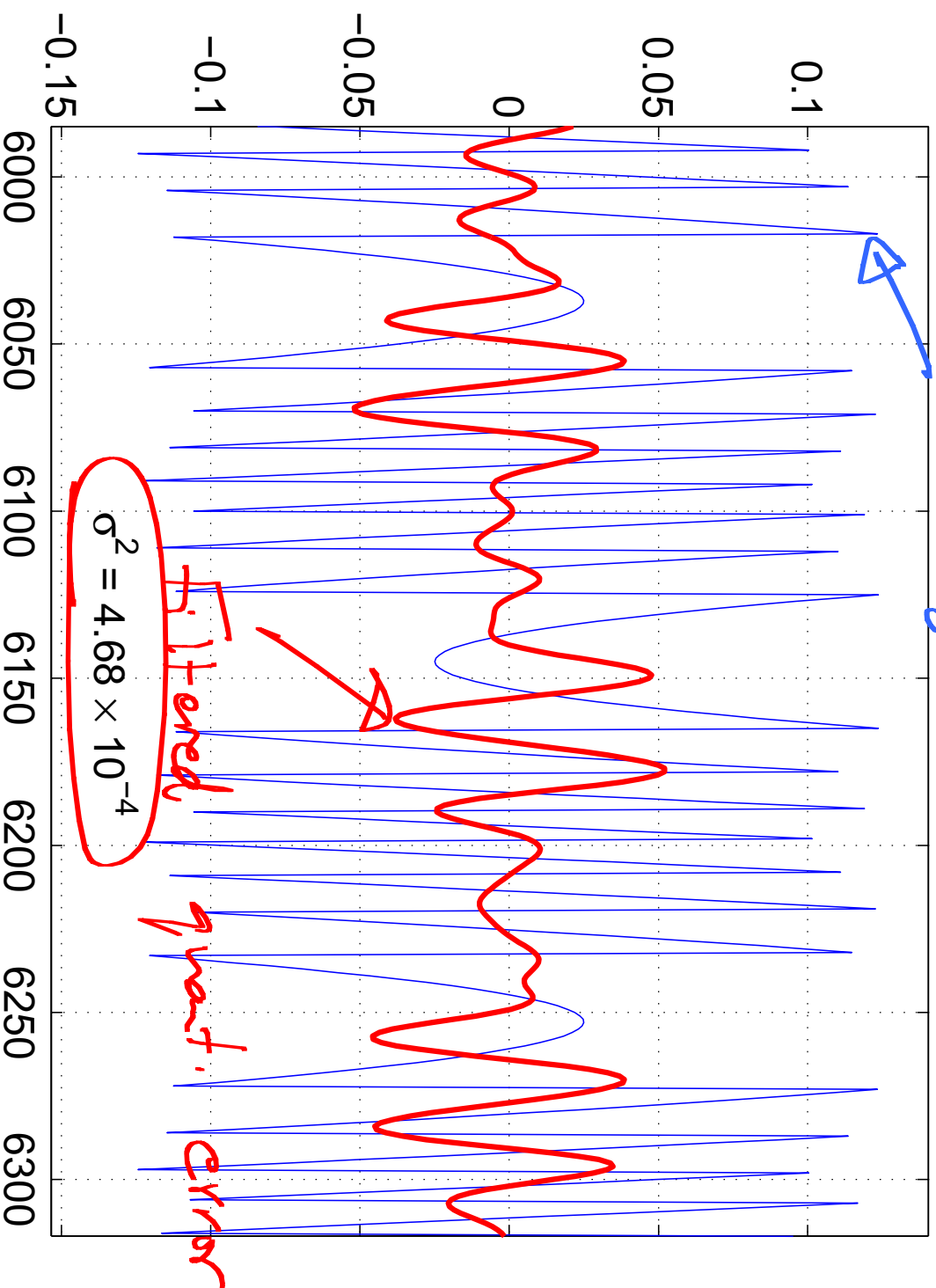


In the time domain



In the time domain

Quantization noise



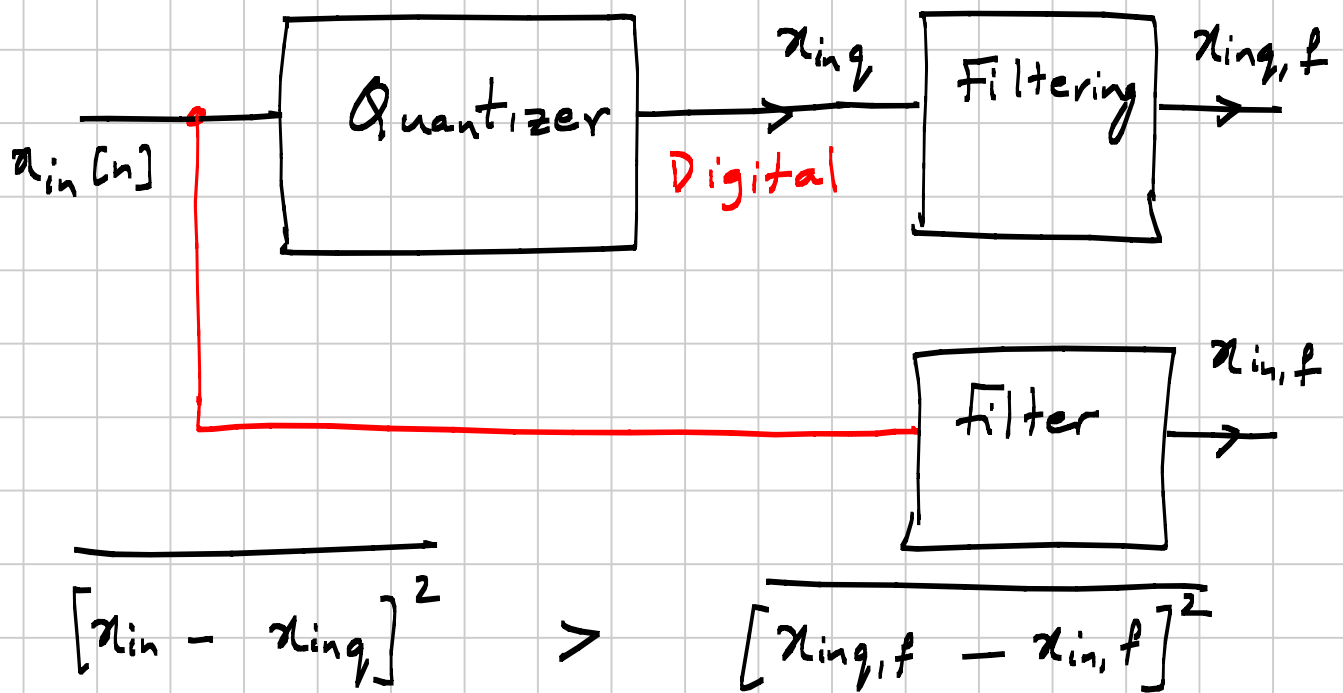
Lecture 18

VLSI Data Conversion Circuits

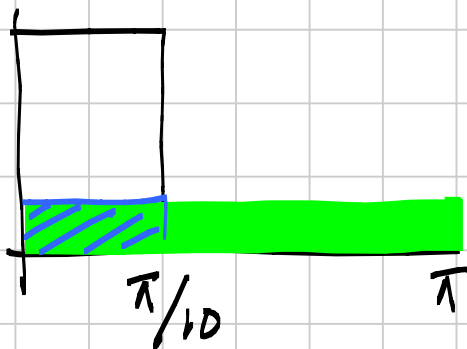
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February 2, 2011

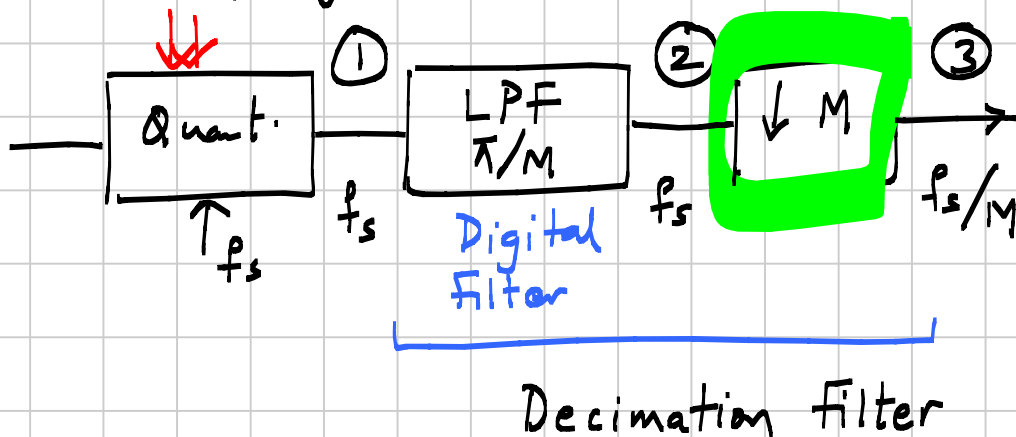


Example:

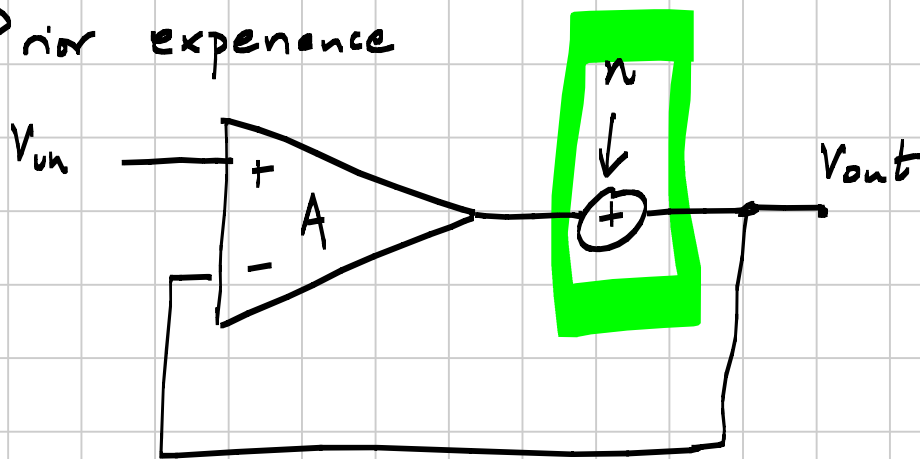


Mean square noise $\downarrow 10$

* Oversampling + Low Pass Filtering



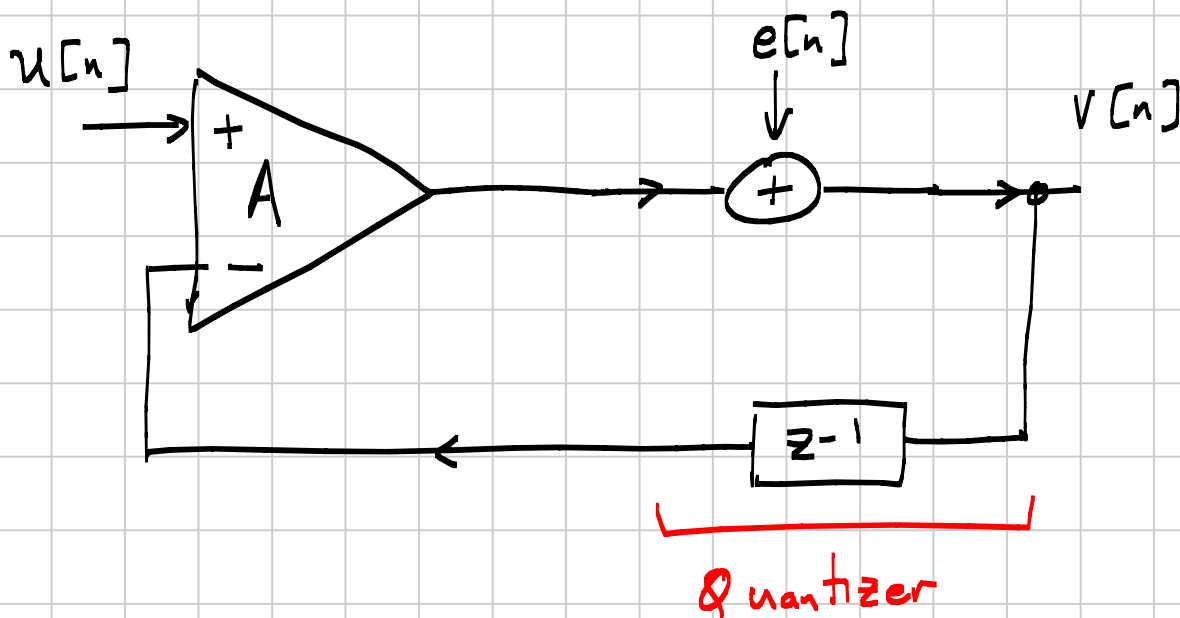
Prior experience



$$V_{out} = V_{in} \frac{A}{1+A} + \frac{n}{1+A}$$

as $A \rightarrow \infty$,

$$\underline{V_{out} = V_{in}}$$



$$\{u(z) - z^{-1}v(z)\}A + E(z) = V(z)$$

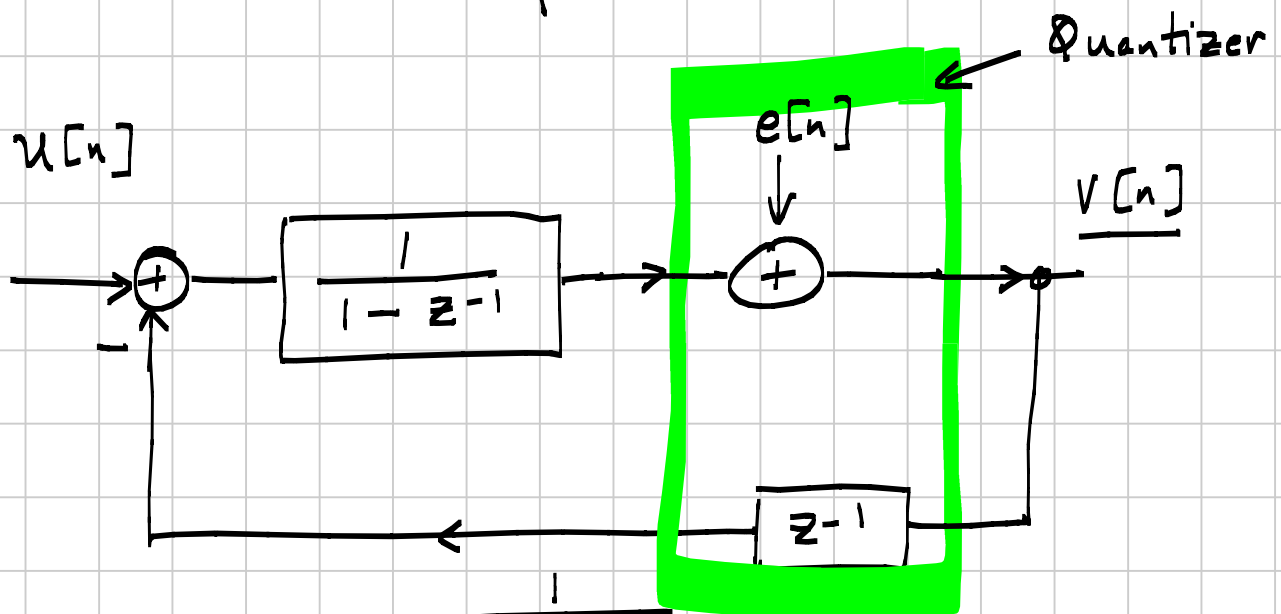
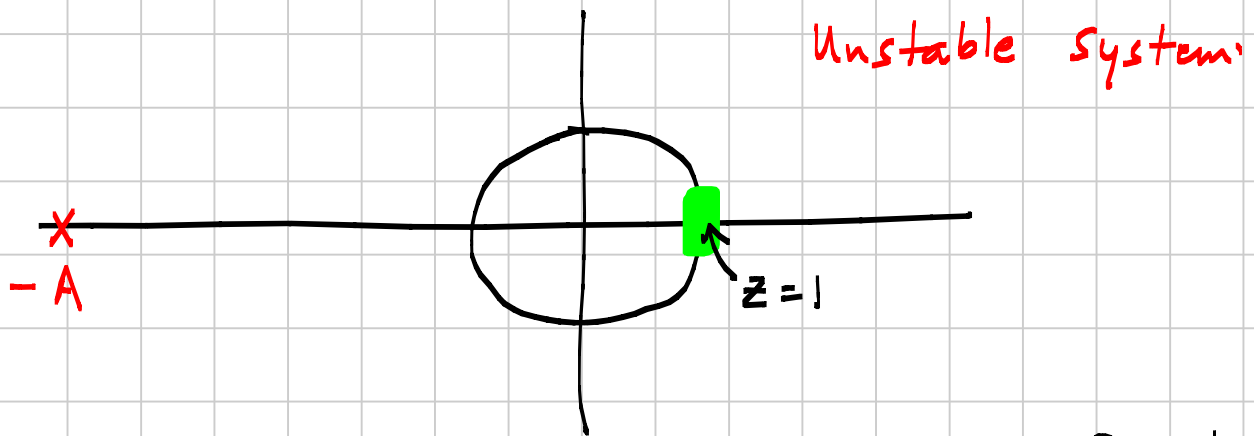
$$\Rightarrow V(z) \{Az^{-1} + 1\} = A u(z) + E(z)$$

$$\Rightarrow V(z) = \underbrace{1}_{\text{STF}} u(z) + \underbrace{\frac{1}{1 + Az^{-1}}}_{\text{NTF}} E(z)$$

Signal Transfer
Function

Noise Transfer
Function

$$1 + A z^{-1} = 0 \quad \Rightarrow \quad z = -A$$



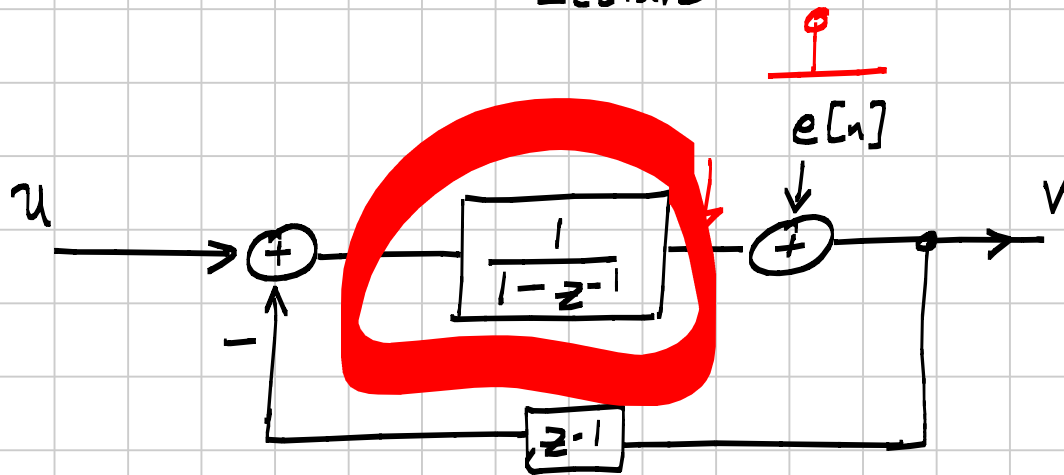
$$STF = \frac{1}{1 + \frac{z^{-1}}{1 - z^{-1}}} = 1$$

$$NTF = \frac{1}{1 + \frac{z^{-1}}{1 - z^{-1}}} = \underline{(1 - z^{-1})}$$

Poles @ $z = 0$

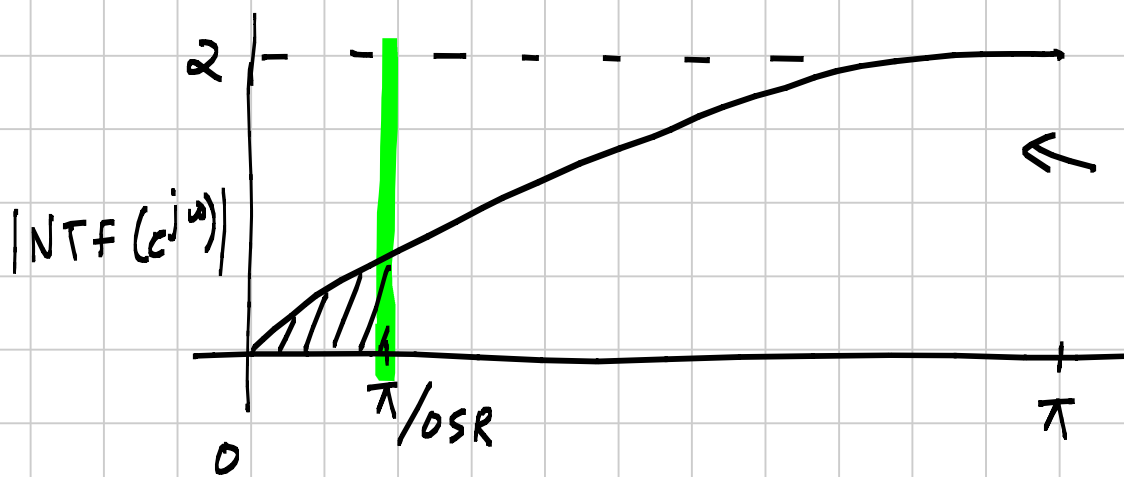
VLSI Data Conversion Circuits

Lecture 19



$\Delta\Sigma, \Sigma\Delta$
Noise shaped,
Oversampled
Converter

$$STF = 1 \quad NTF = 1 - z^{-1}$$



← High pass
Characteristic

$$\int_0^{\pi/OSR} \frac{\Delta^2}{12\pi} |NTF(e^{j\omega})|^2 d\omega \quad \leftarrow \text{In-band quantization noise}$$

$$|NTF(e^{j\omega})| = |1 - e^{-j\omega}| = |e^{j\omega/2} - e^{-j\omega/2}|$$

$$= 2 \sin \frac{\omega}{2}$$

@ low freq. $|NTF| = \omega$

$$\text{In band noise} = \frac{\Delta^2}{12\pi} \int_0^{\pi/OSR} \omega^2 d\omega = \frac{\Delta^2}{12\pi} \cdot \frac{\pi^3}{3 OSR^3}$$

$$\frac{\Delta^2}{36\pi} \frac{\pi^3}{OSR^3}$$

OSR $\uparrow$ 2 , Noise $\downarrow$ 8 (= 9 dB)

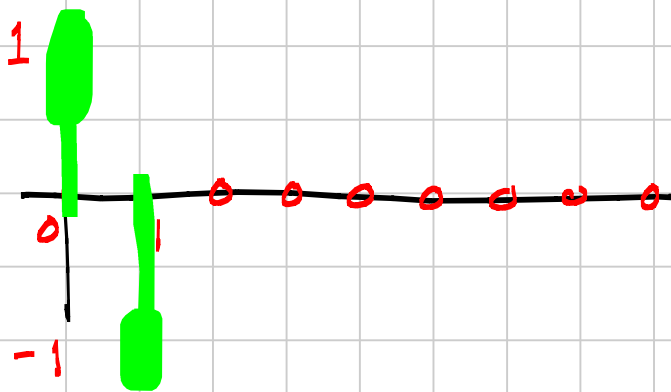
= 1.5 bits / doubly OSR

Noise Shaping

$$1 - z^{-1} = \frac{z-1}{z}$$

NTF

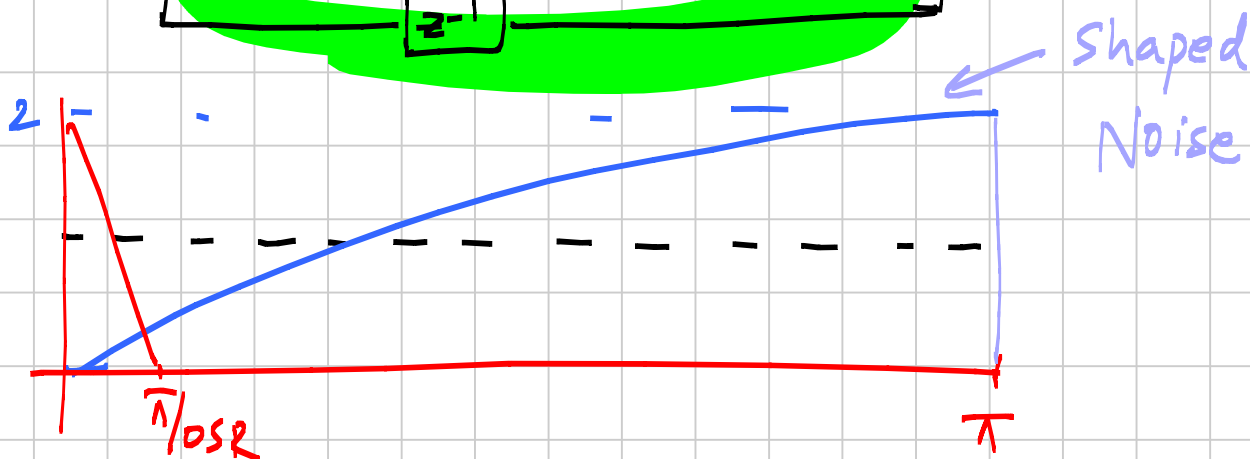
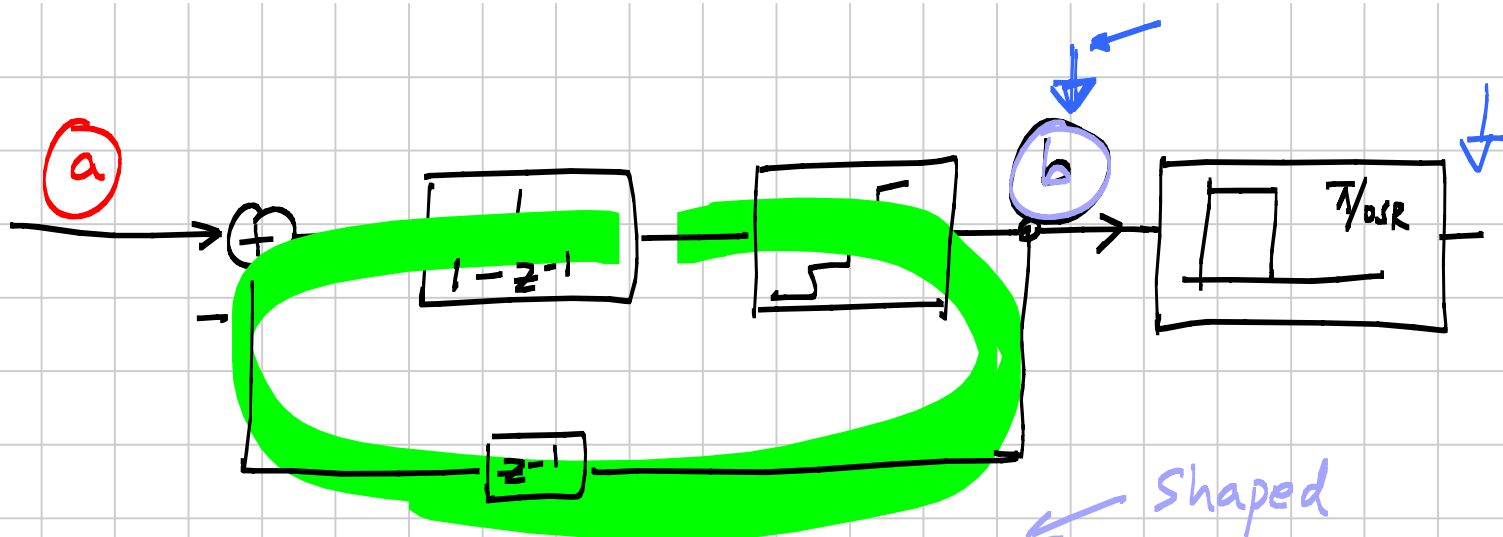
①



zero @ $z=1$
pole @ $z=0$

$$z^{-1} \{ NTF(z) \} \equiv h[n]$$

$$\sum h[n] = 0$$



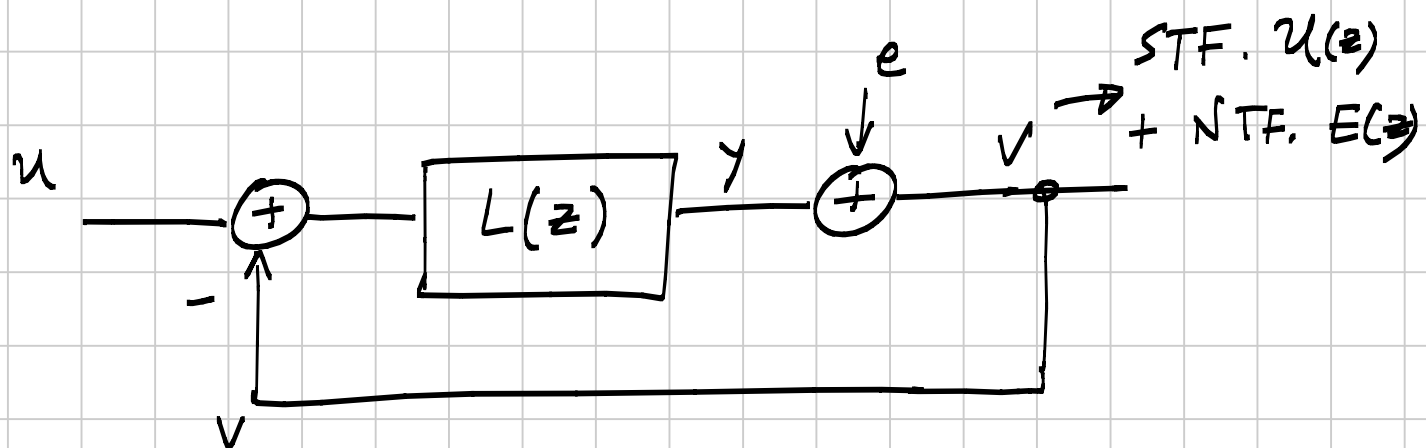
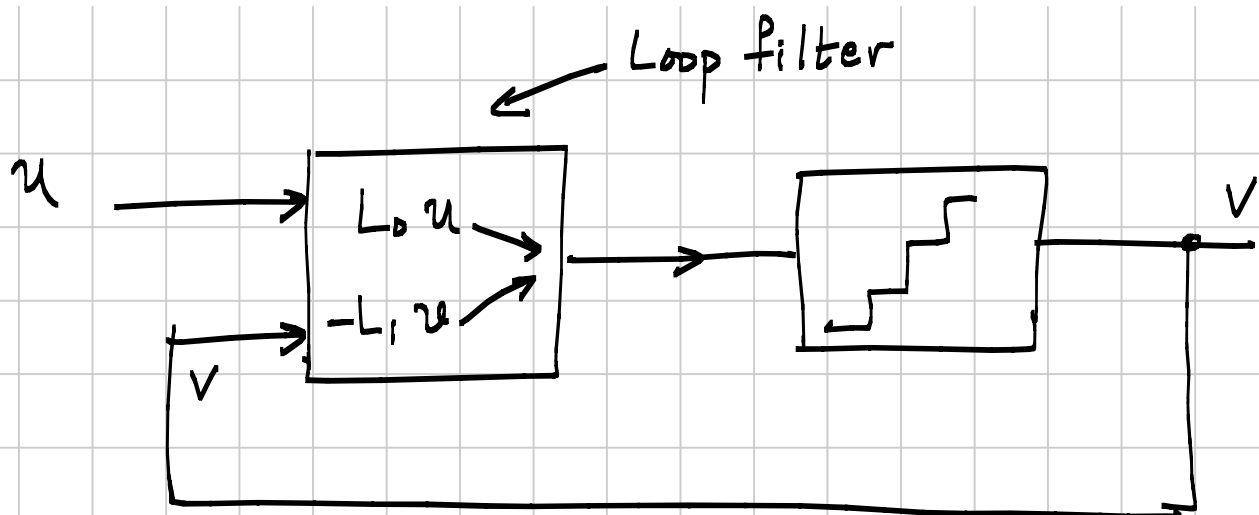
$$\frac{1}{\pi} \int_0^{\pi} |NTF(e^{jw})|^2 dw = \sum_{n=0}^{\infty} h^2(n)$$

* The first sample of the NTF impulse response $h[0] = 1$

$$NTF(z) = h[0] + h[1]z^{-1} + \dots$$

$$NTF(z = \infty) = 1$$

$\Rightarrow$ No "delay free" loop



$$STF = \frac{L(z)}{1 + L(z)}$$

$$NTF = \frac{1}{1 + L(z)}$$

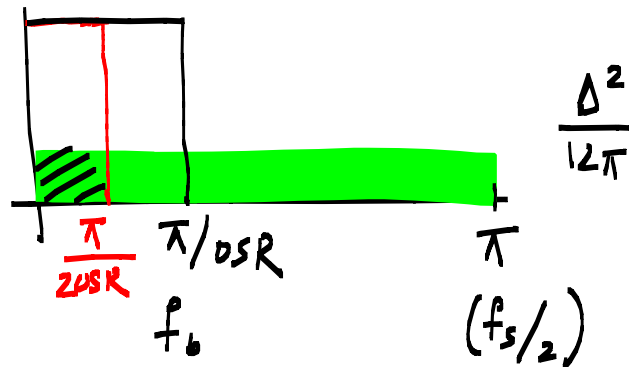
STF: $u(z)$
+ NTF: $e(z)$

$$f_b \rightarrow 2f_b \text{ (Nyq. rate)}$$

$$\frac{f_s}{2f_b} \rightarrow \text{OSR}$$

Outline

Decimation
Filter
Response



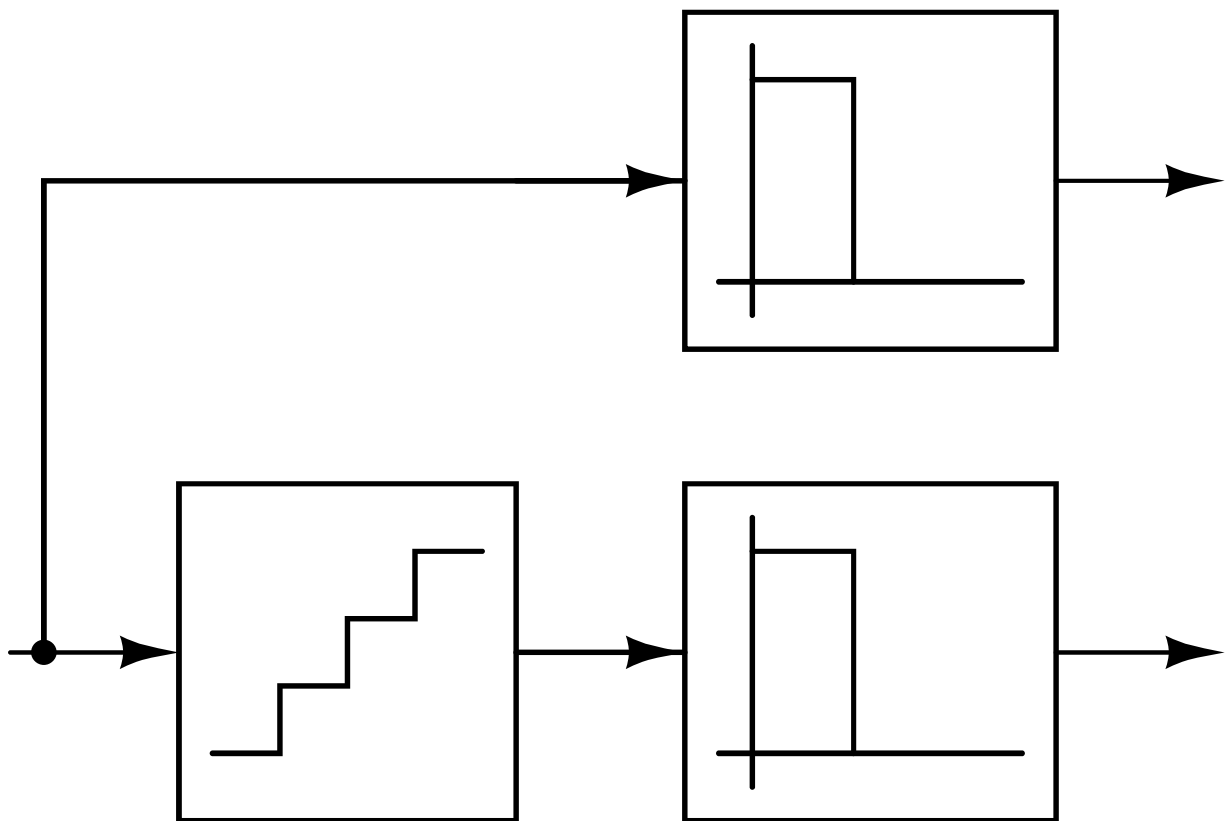
In-band SNR

$$\text{OSR} \uparrow 2, \quad \text{SQNR} \uparrow 2 = 3 \text{ dB}$$

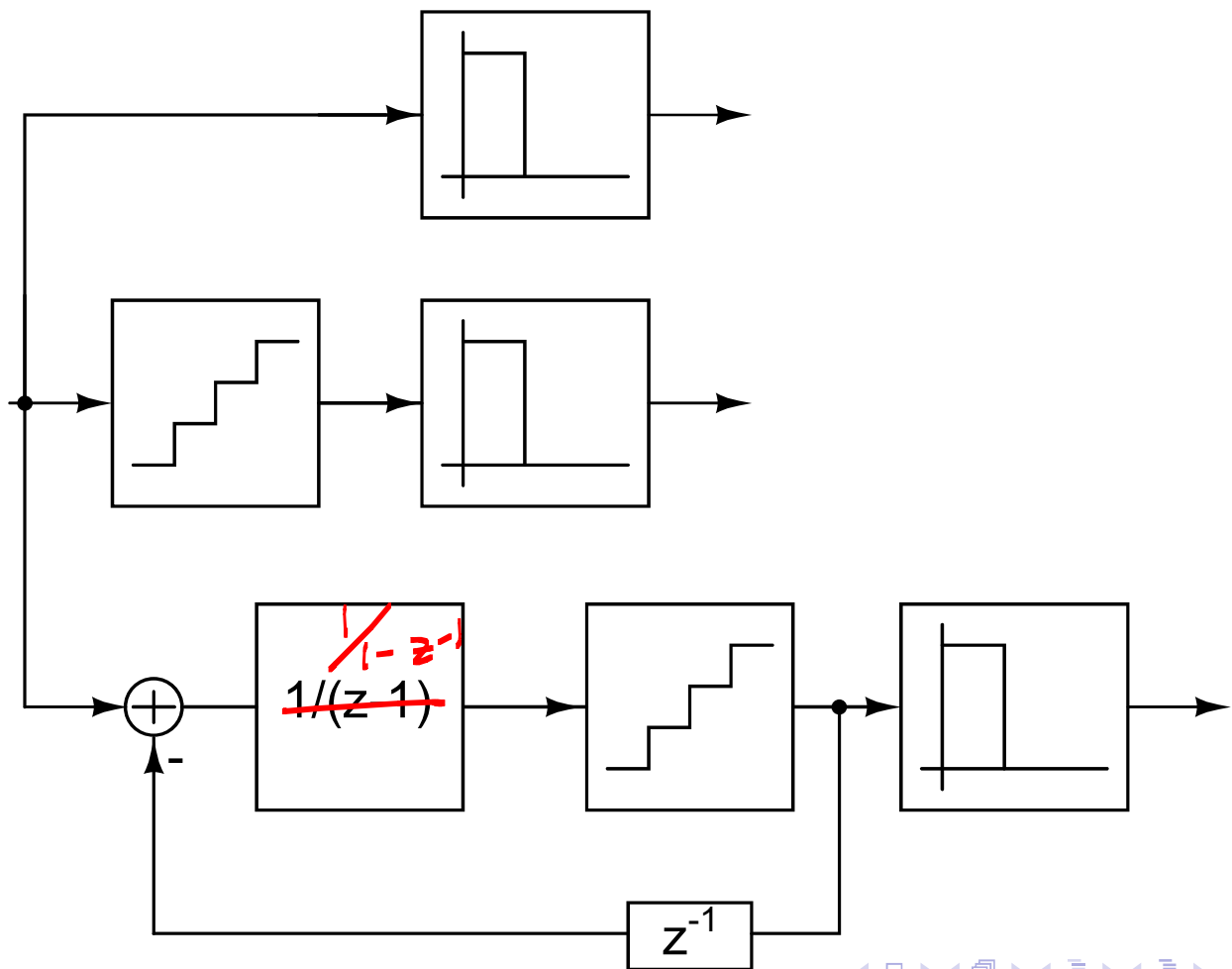
$$\uparrow 4, \quad \text{SQNR} \uparrow 4 = 6 \text{ dB}$$

$\Rightarrow$ Every doubling of OSR gives 3 dB, or 0.5 bit

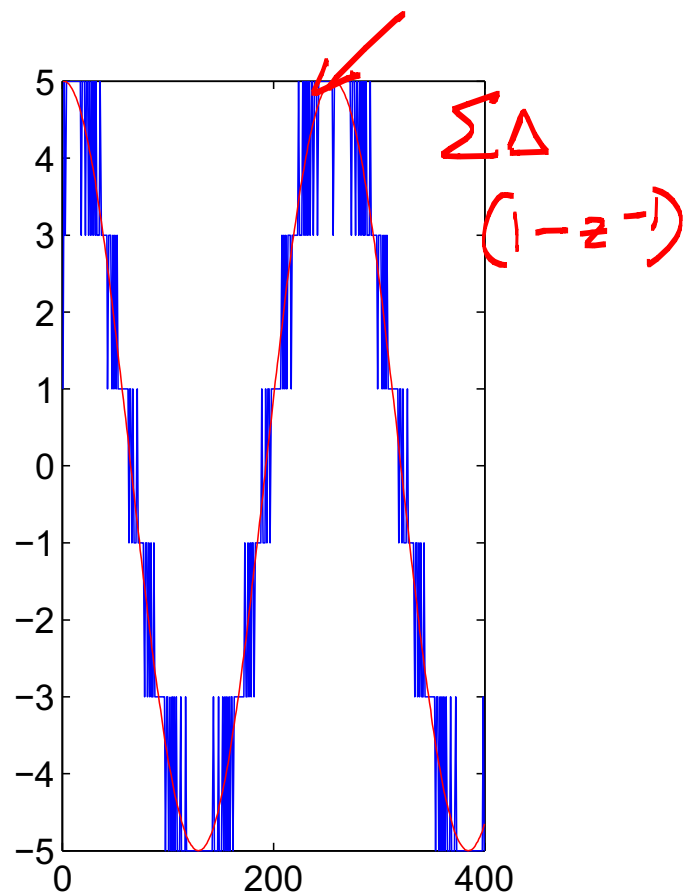
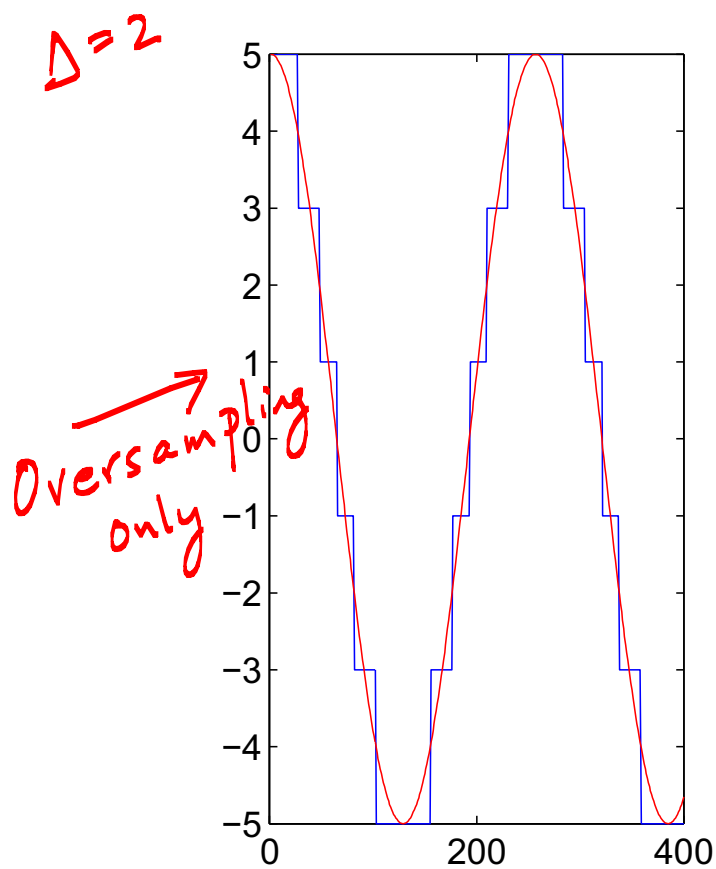
Oversampling System Diagram



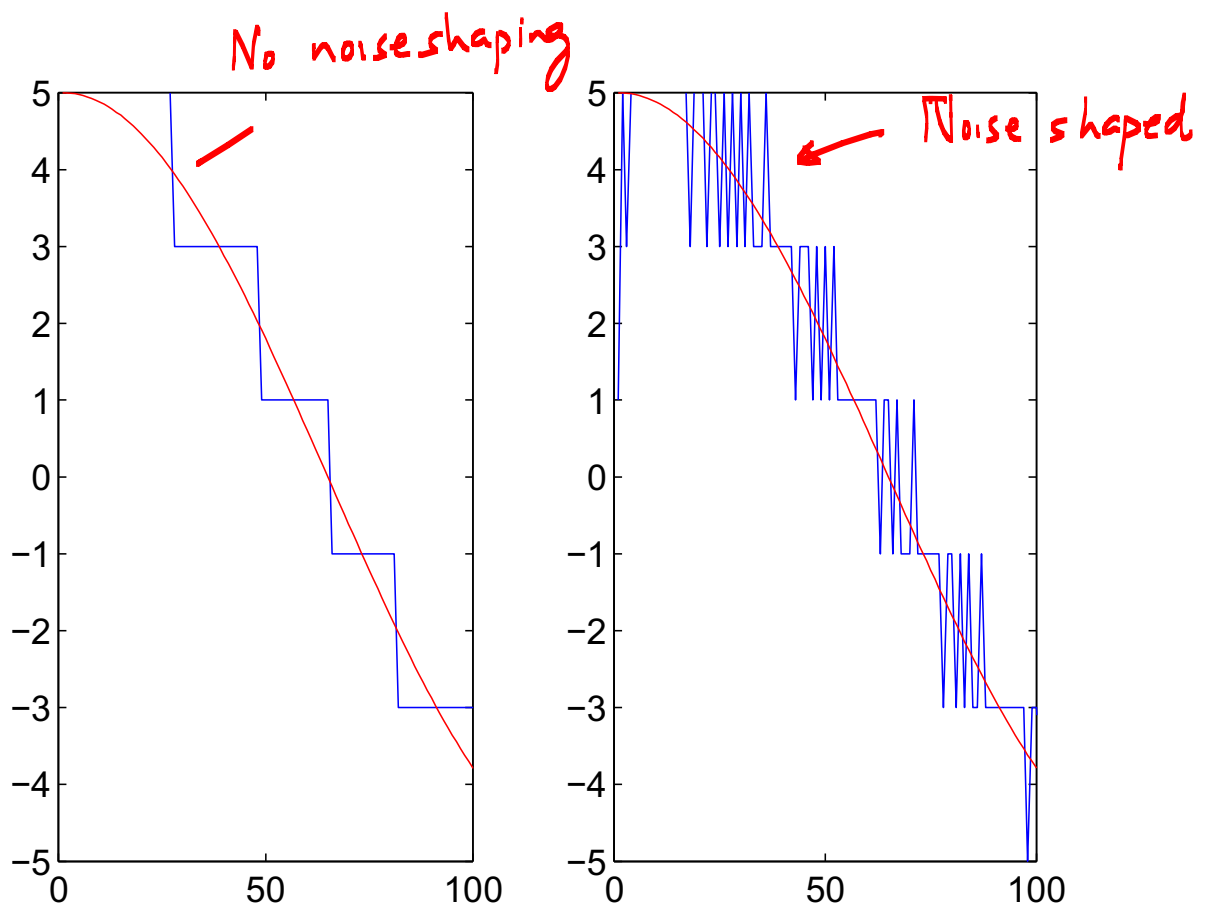
ΣΔ Oversampling + Noise Shaping System Diagram



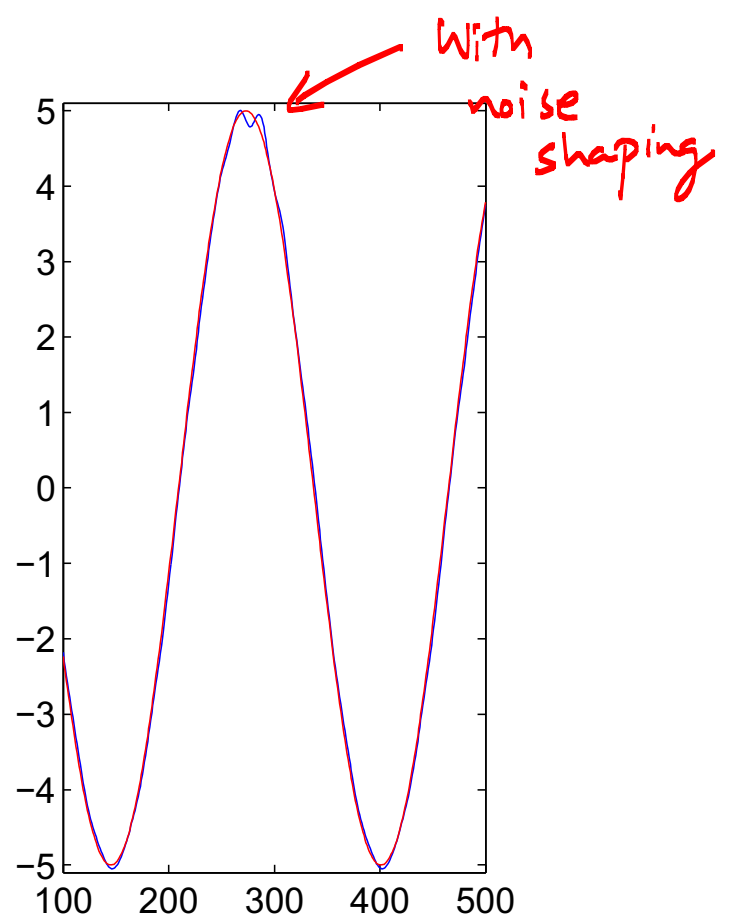
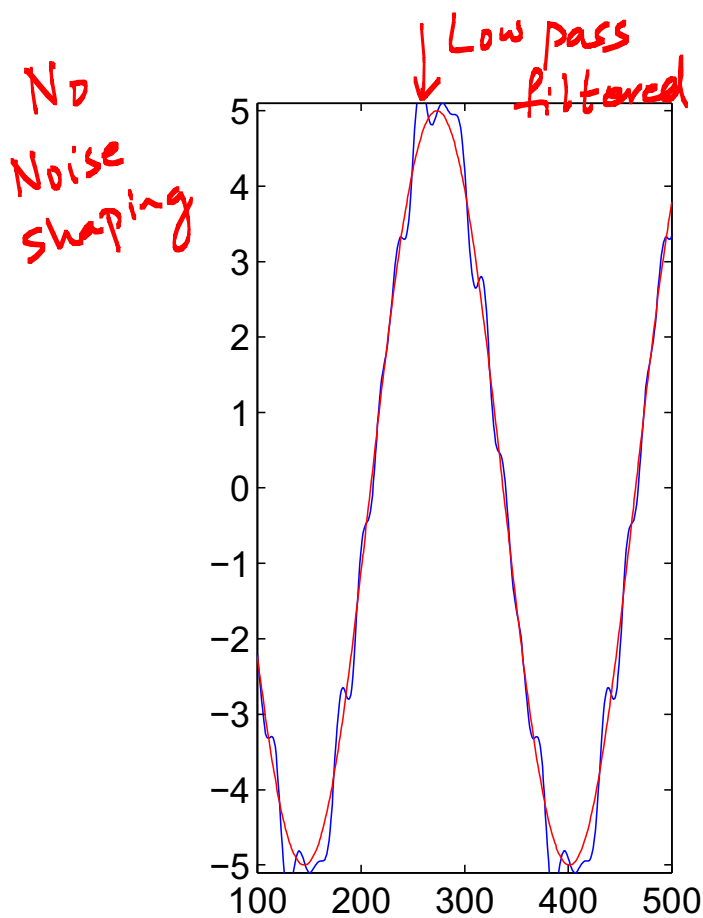
Sinusoid : Oversampling vs Noise Shaping



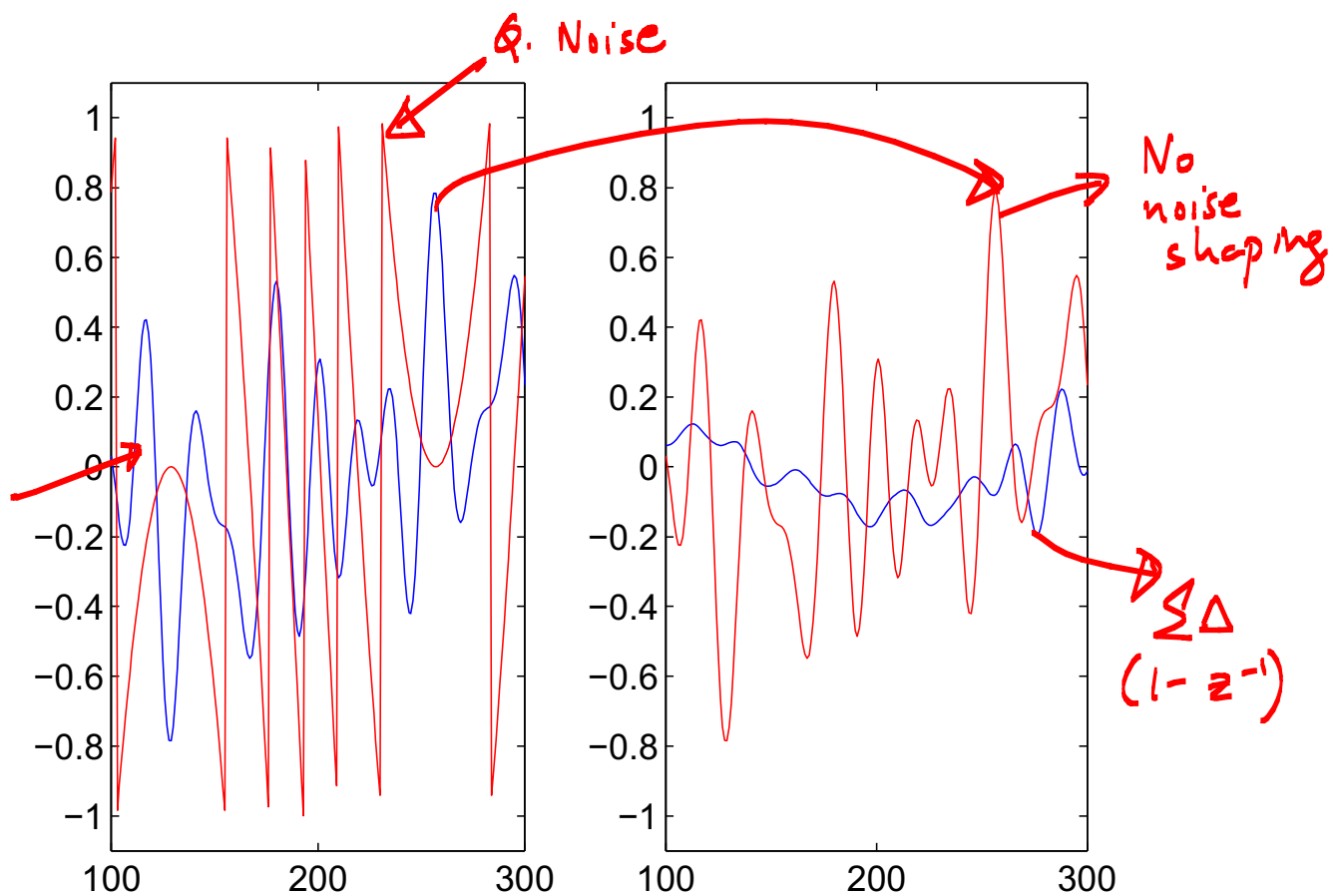
Sinusoid : Oversampling vs Noise Shaping



Sinusoid : Oversampling vs Noise Shaping



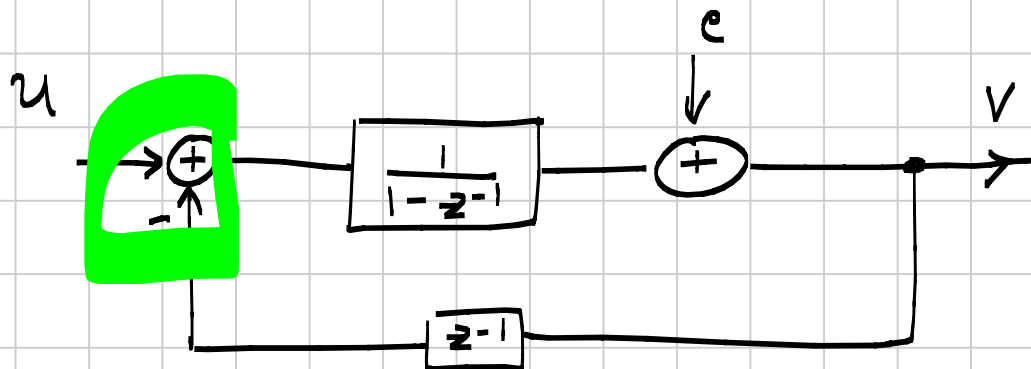
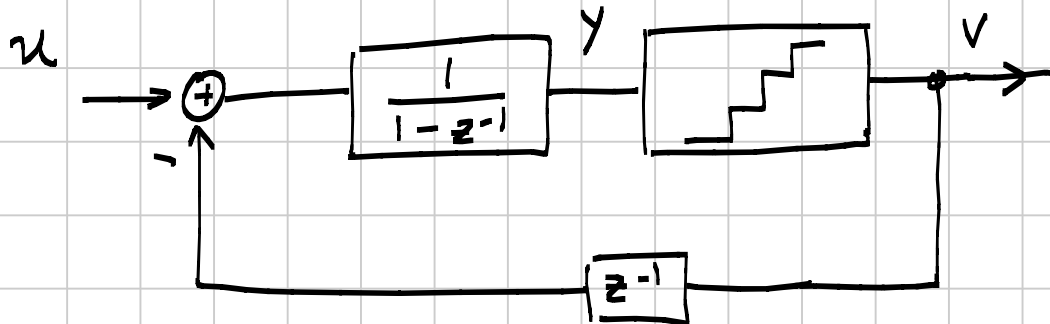
Sinusoid : Oversampling vs Noise Shaping



VLSI Data Conversion Circuits: Lecture 20

Note Title

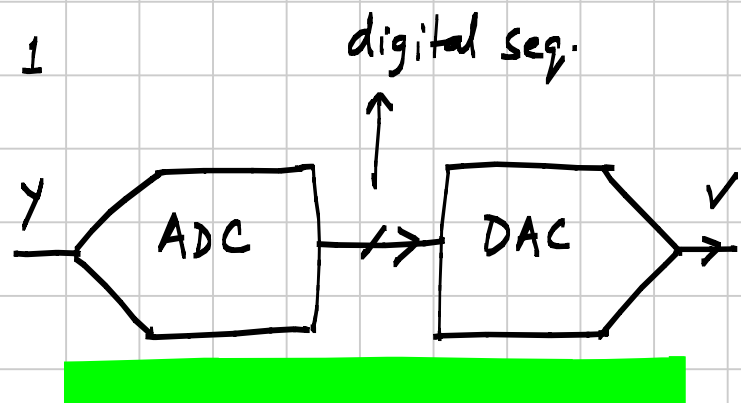
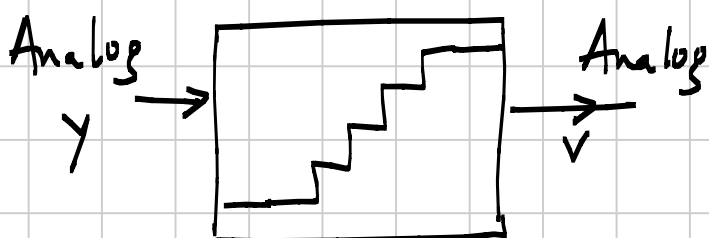
05-02-2011

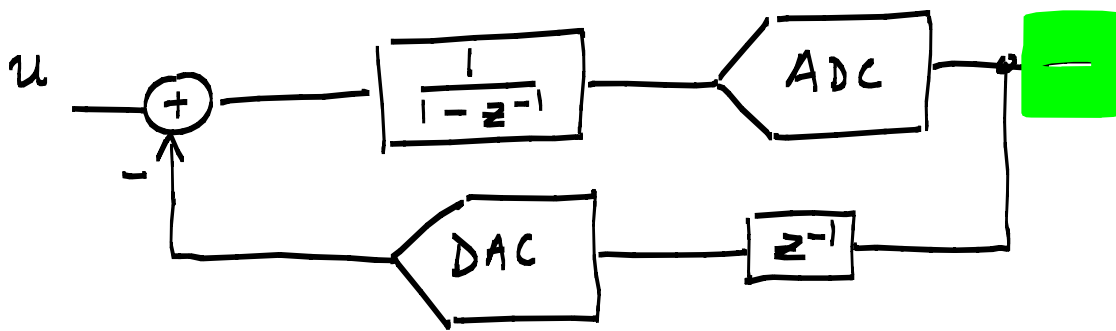


$$V(z) = \underbrace{STF}_{\downarrow 1} U(z) + \underbrace{NTF}_{(1-z^{-1})} E(z)$$

$$* \sum_{n=0}^{\infty} h[n] = 0 \quad \left\{ \begin{array}{l} DC \text{ gain} = 0 \end{array} \right.$$

$$* h[0] = 1 \\ \equiv NTF(z=\infty) = 1$$





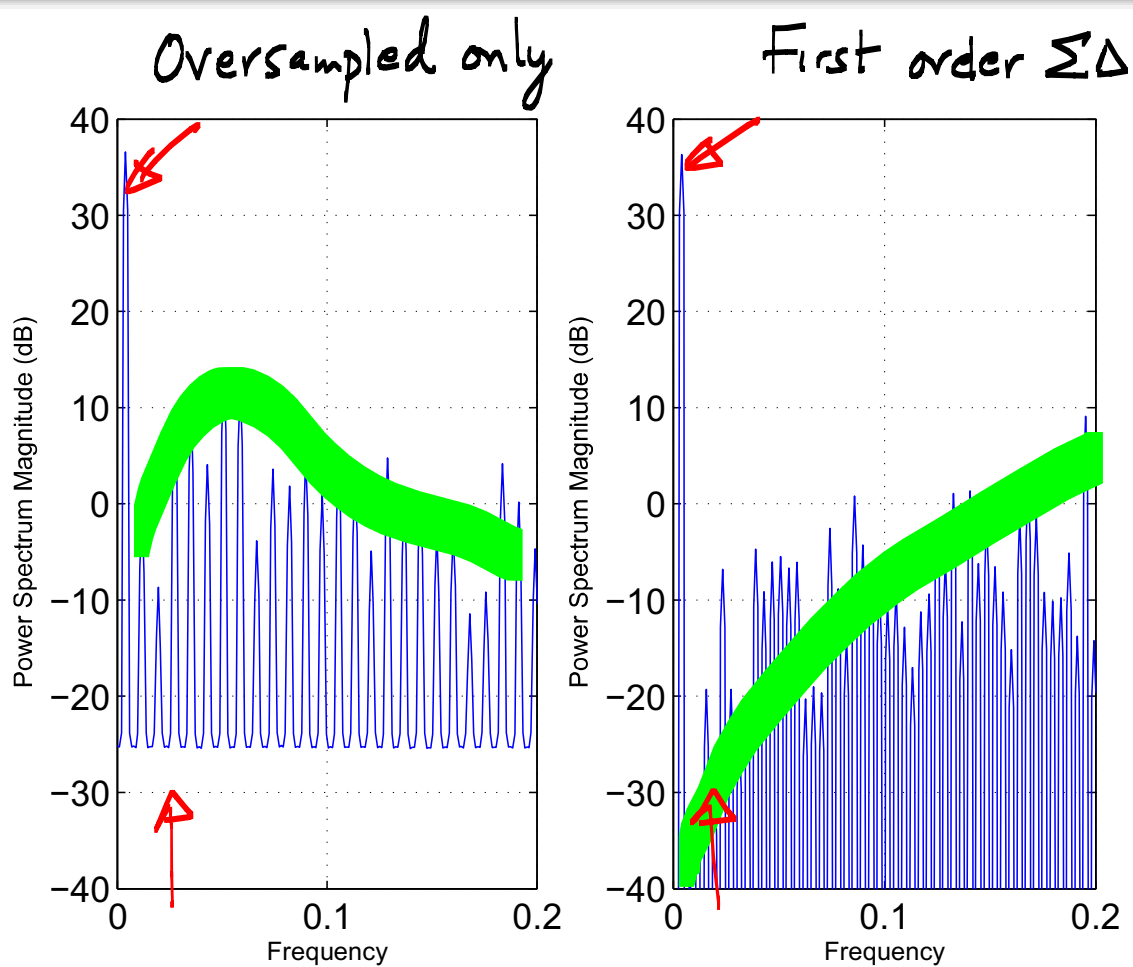
VLSI Data Conversion Circuits

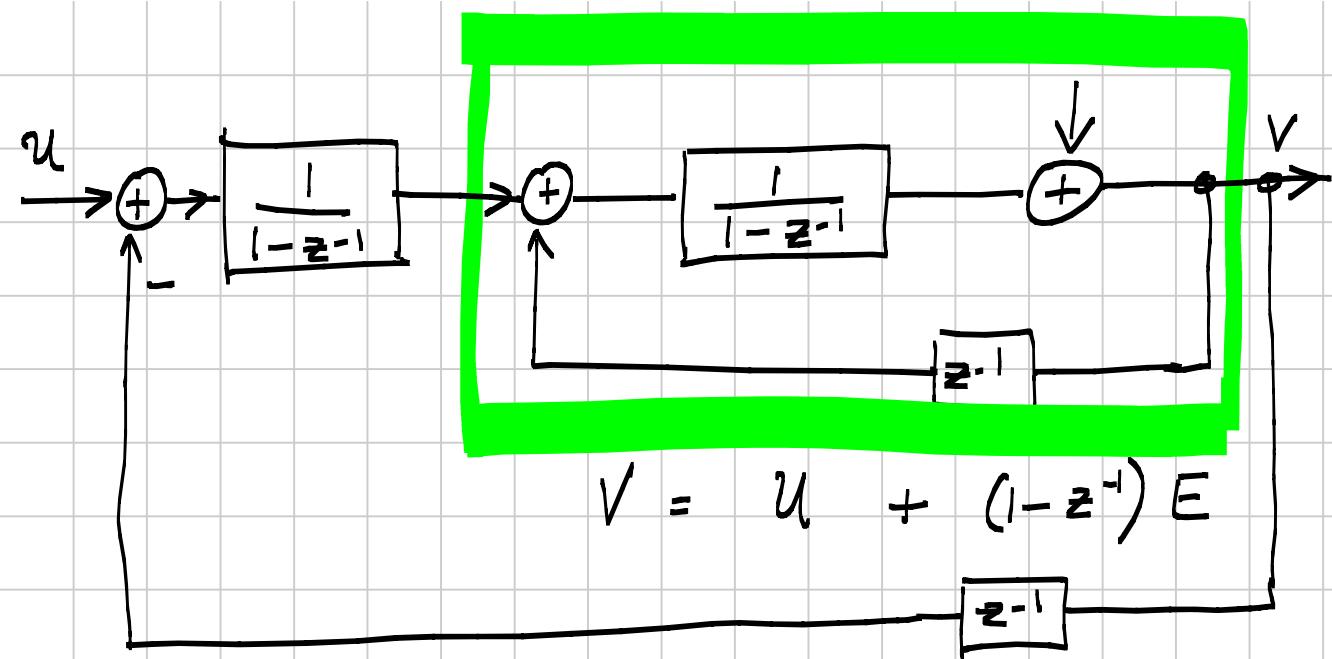
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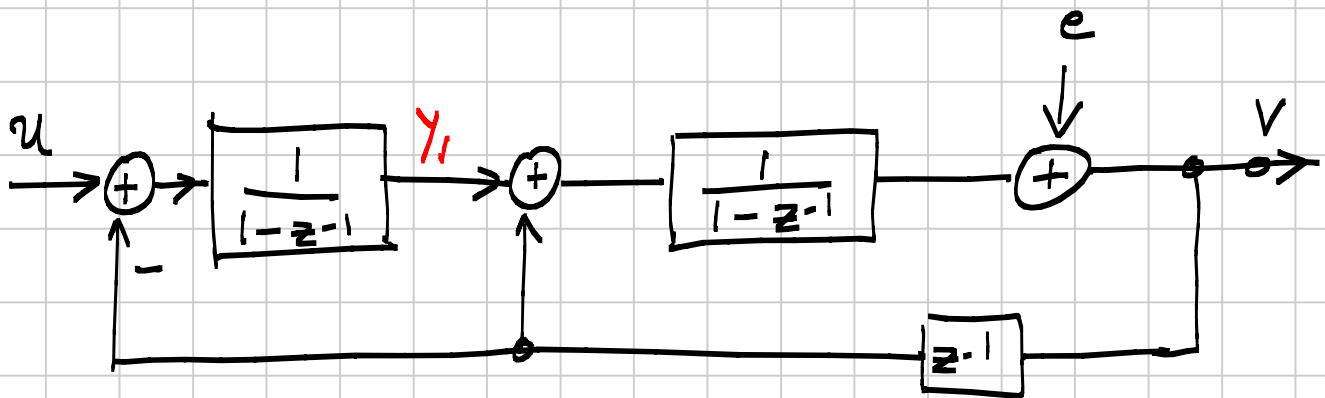
February 5, 2011

Spectrum : Oversampling vs Noise shaping





$$V = u + (1 - z^{-1}) E$$



$$V = Y_1 + (1 - z^{-1}) E$$

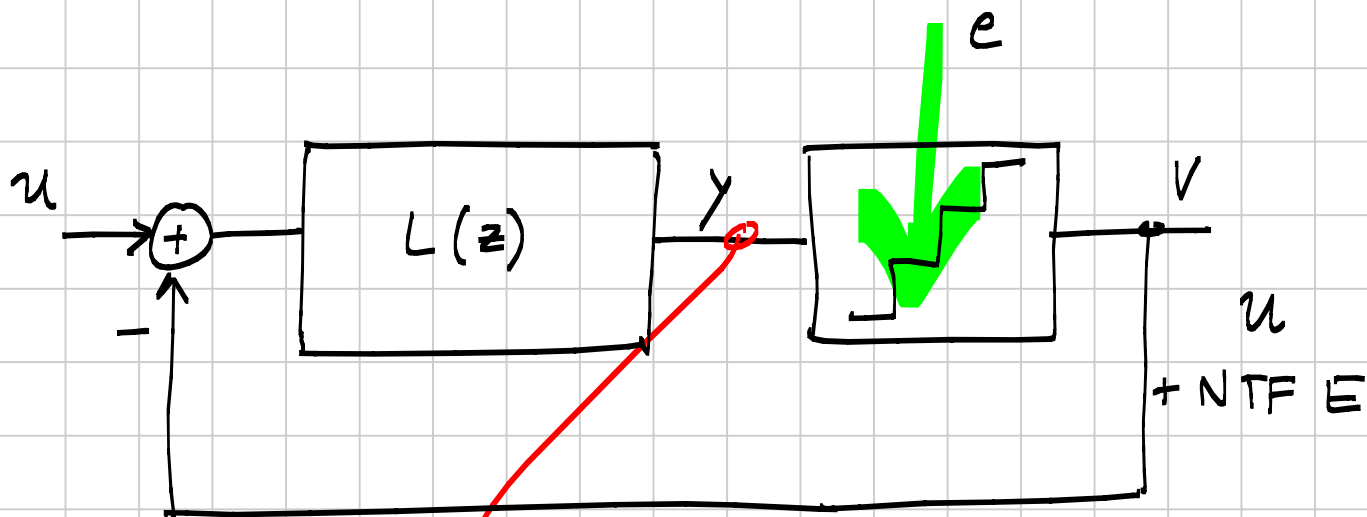
$$V = u + (1 - z^{-1})^2 E$$

$$STF = 1 \quad NTF = (1 - z^{-1})^2$$

Second order $\Delta\Sigma M$

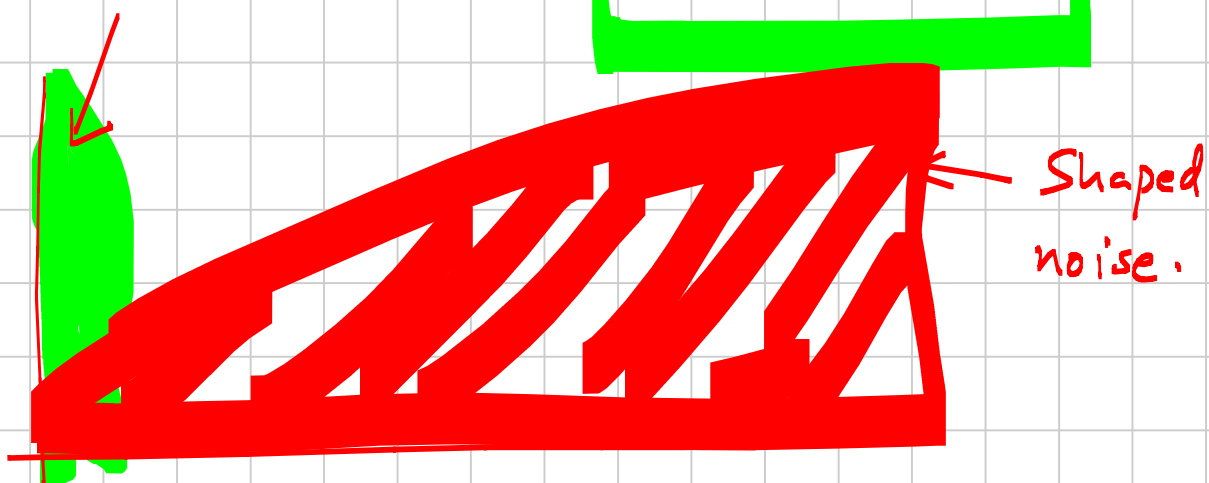
$$NTF = (1 - z^{-1})^2 \quad h[n] = 1, -2, 1$$

$$\sum_{n=0}^{\infty} h[n] = 0, \quad h[0] = 1$$



Input

$$u + (NTF(z) - 1) E(z)$$



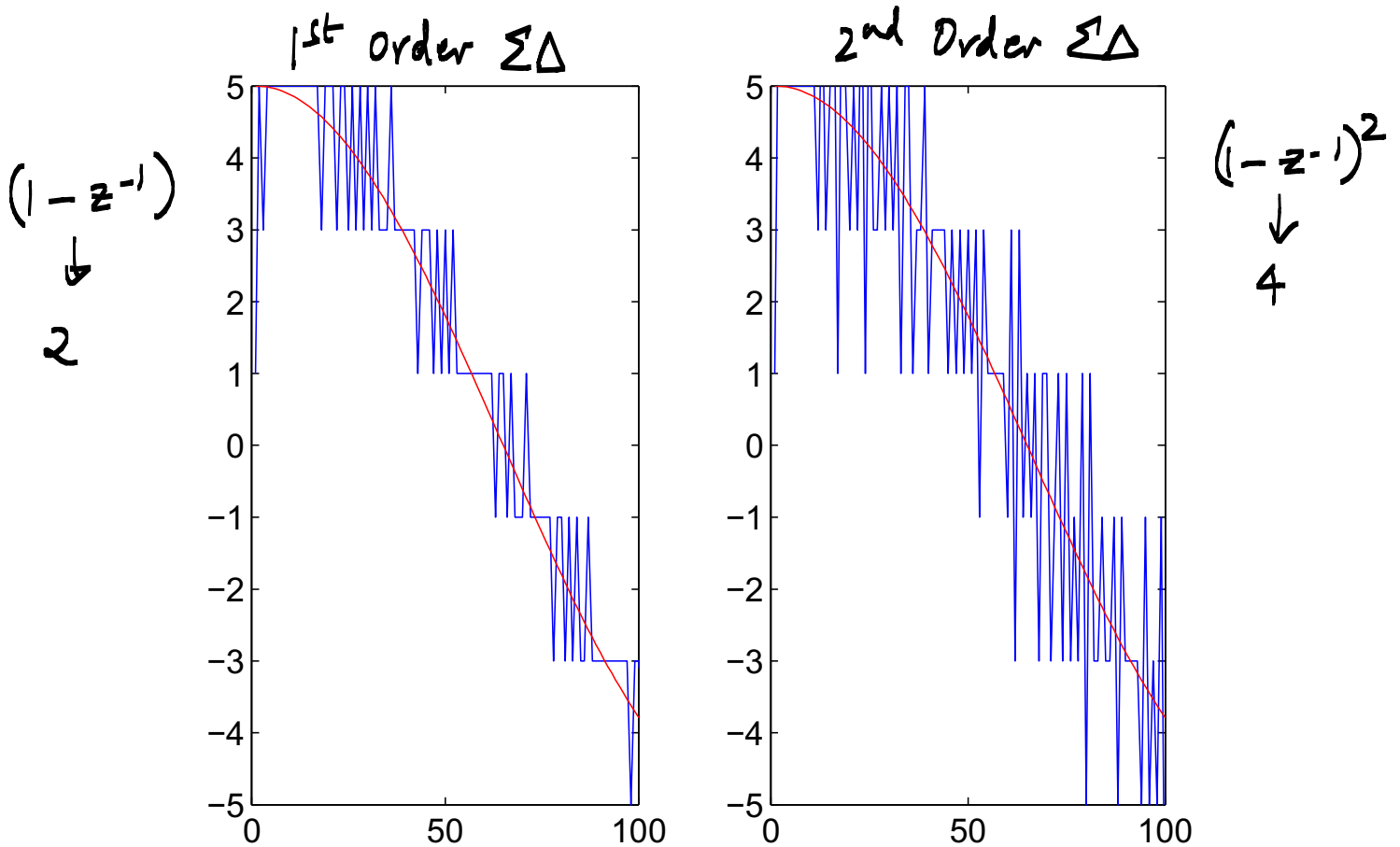
Shaped
noise.

NTF @ low freq $\approx \omega^2$

$$\text{Inband Noise} = \frac{\Delta^2}{12\pi} \int_0^{\pi/\text{OSR}} \omega^4 d\omega = \frac{\Delta^2}{12\pi} \frac{1}{5} \left(\frac{\pi}{\text{OSR}} \right)^5$$

OSR $\uparrow$ 2x $\Rightarrow$ Noise power $\downarrow$ 32 $\Rightarrow$ 15 dB or 2.5 bits

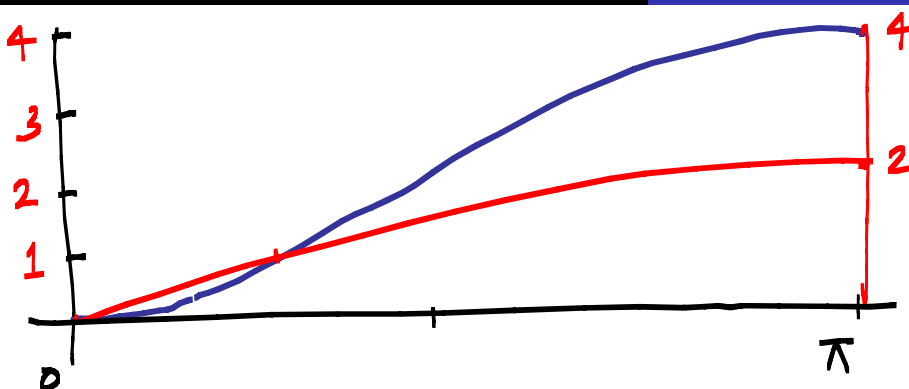
First and Second Order $\Delta\Sigma$



Navigation icons: back, forward, search, etc.

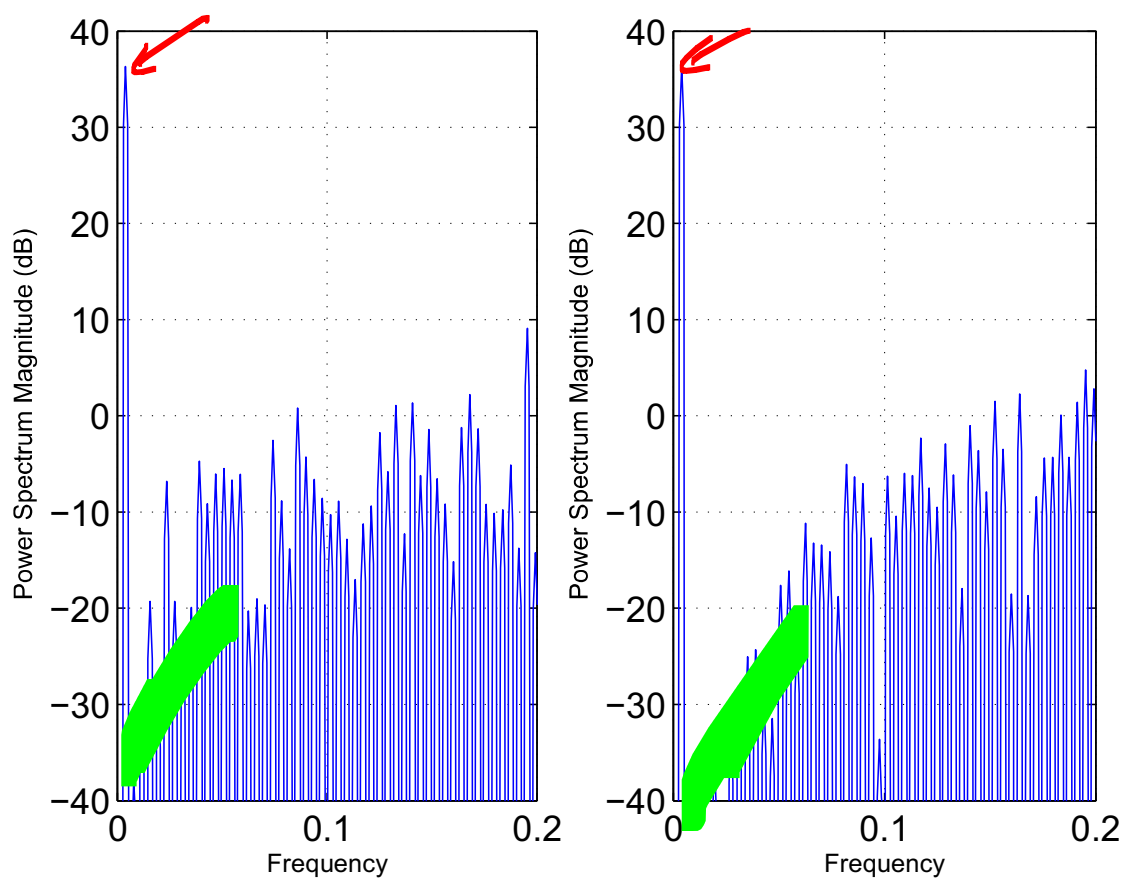
Shanthi Pavan

VLSI Data Conversion Circuits



$\frac{\Delta^2}{12} \cdot 2 \leftarrow 1^{\text{st}} \text{ Ord.}$
 $\frac{\Delta^2}{12} \cdot 6 \leftarrow 2^{\text{nd}} \text{ Ord.}$

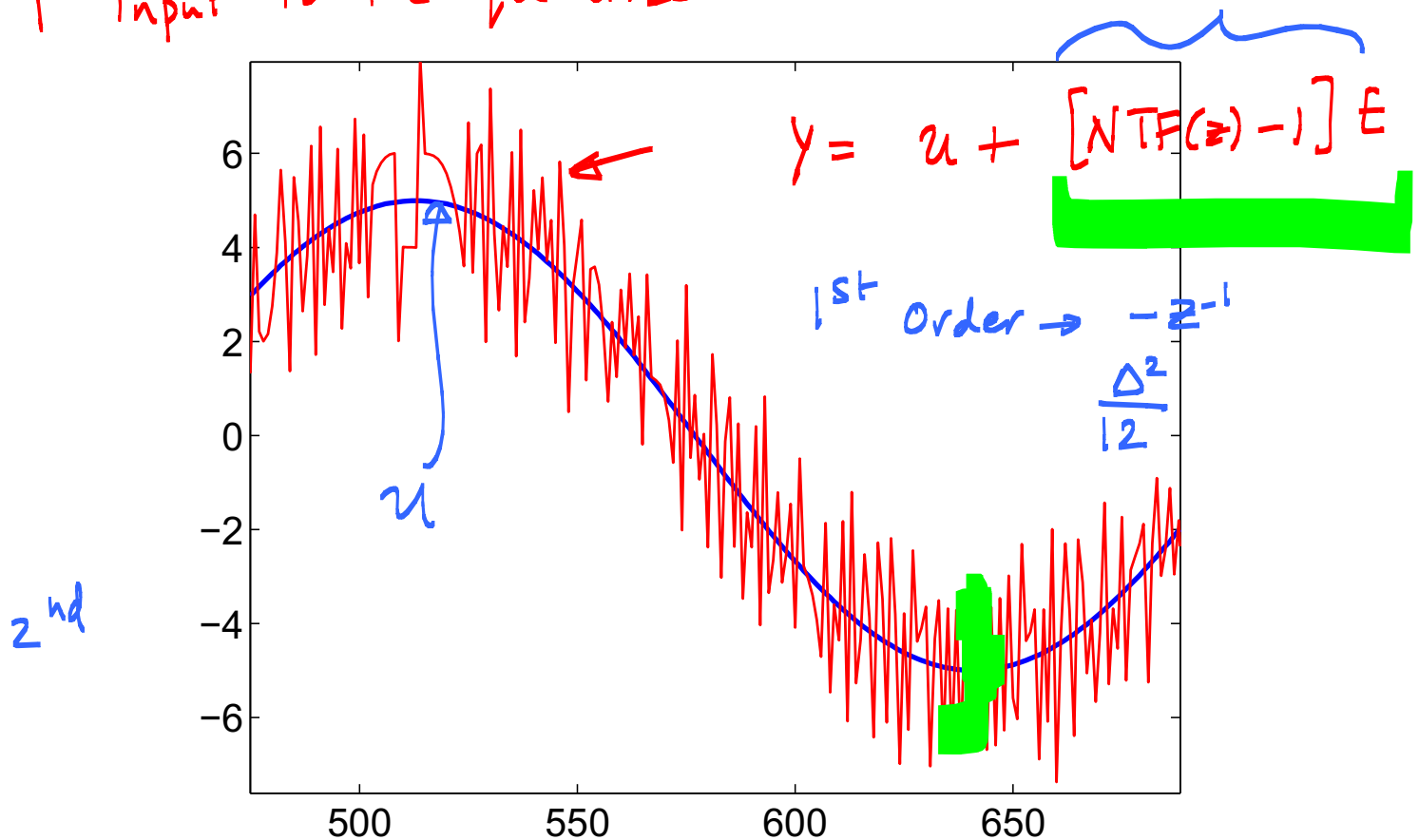
First and Second Order $\Delta\Sigma$





$y[n]$ in a Second Order $\Delta\Sigma$

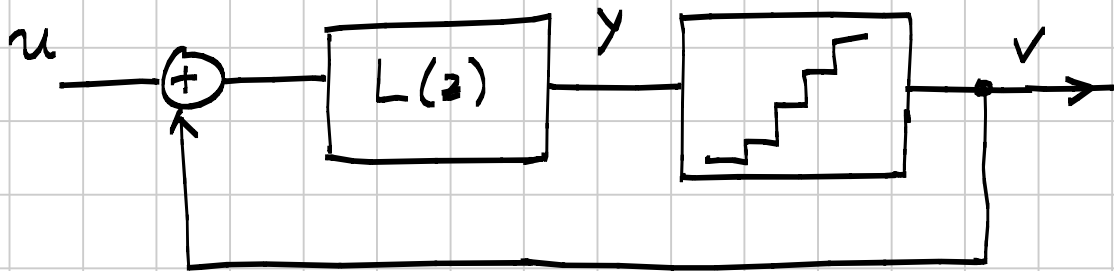
↑ Input to the quantizer



$$2^{nd} \text{ Order} \rightarrow NTF(z) - 1 = -2z^{-1} + z^{-2}$$

$$5. \frac{\Delta^2}{12}$$

VLSI Data Conversion Circuits: Lecture 21



$$Y(z) = U(z) + \{NTF(z) - 1\} E(z)$$

$$e[n] * \{h[n] - \delta[n]\}$$

$h_1[n]$

$$\sum_{k=0}^{\infty} e[k] h_1[n-k]$$

$|e[k]| \leq \frac{\Delta}{2}$

$$\leq \sum_{k=0}^{\infty} \frac{\Delta}{2} |h_1[n-k]| = \frac{\Delta}{2} \sum_{k=0}^{\infty} |h_1[k]|$$

Ex: $NTF = (1 - z^{-1})^3$

$$h[n] = 1, -3, 3, -1$$

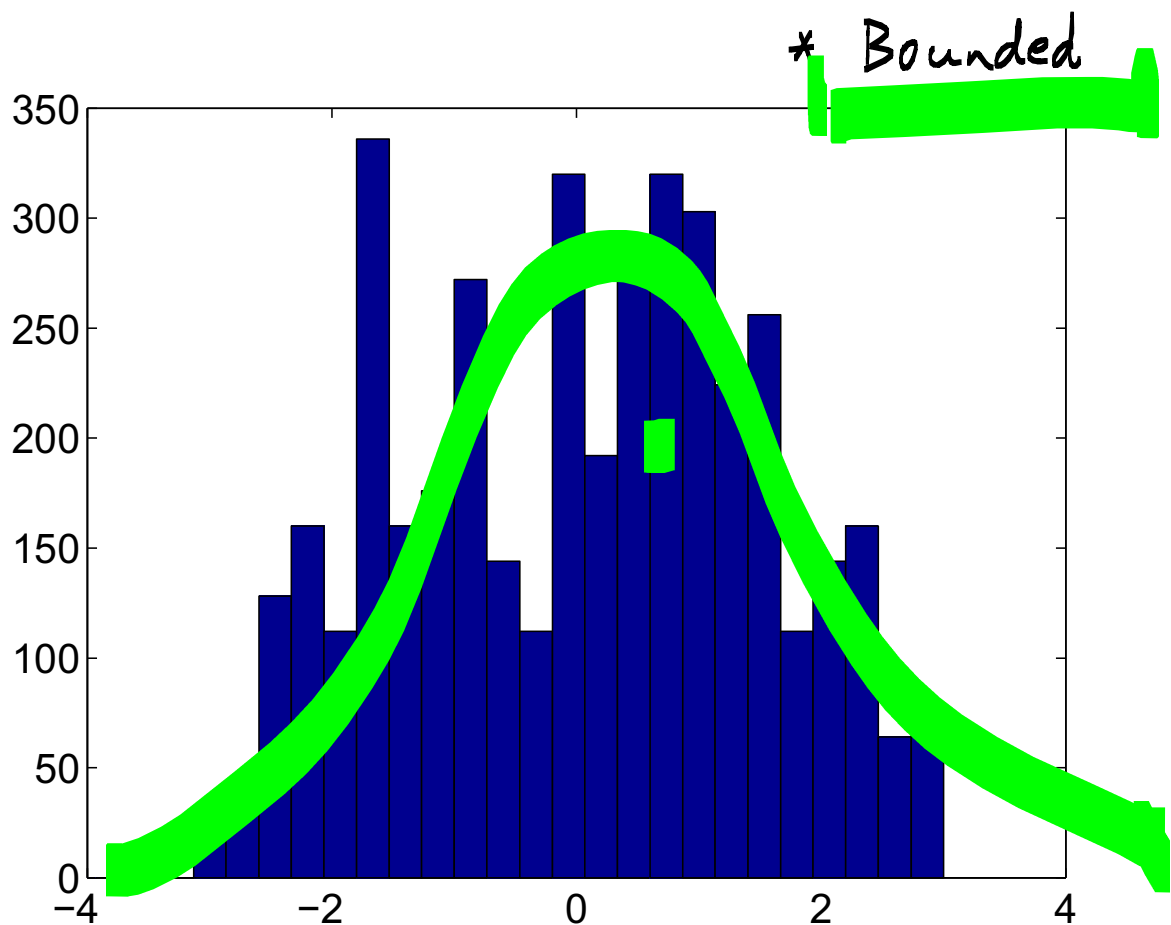
$$h_1[n] = 0, -3, 3, -1$$

	$\sum h_1 $	Gain @ π	$\sum h_1^2[n]$	
First	1	2	1	↓
Second	3	4	5	
Third	7	8	19	
Fourth	15	16	69	

$$(1 - z^{-1})^N \Rightarrow \text{IBN} \propto \text{OSR}^{-(2N+1)}$$

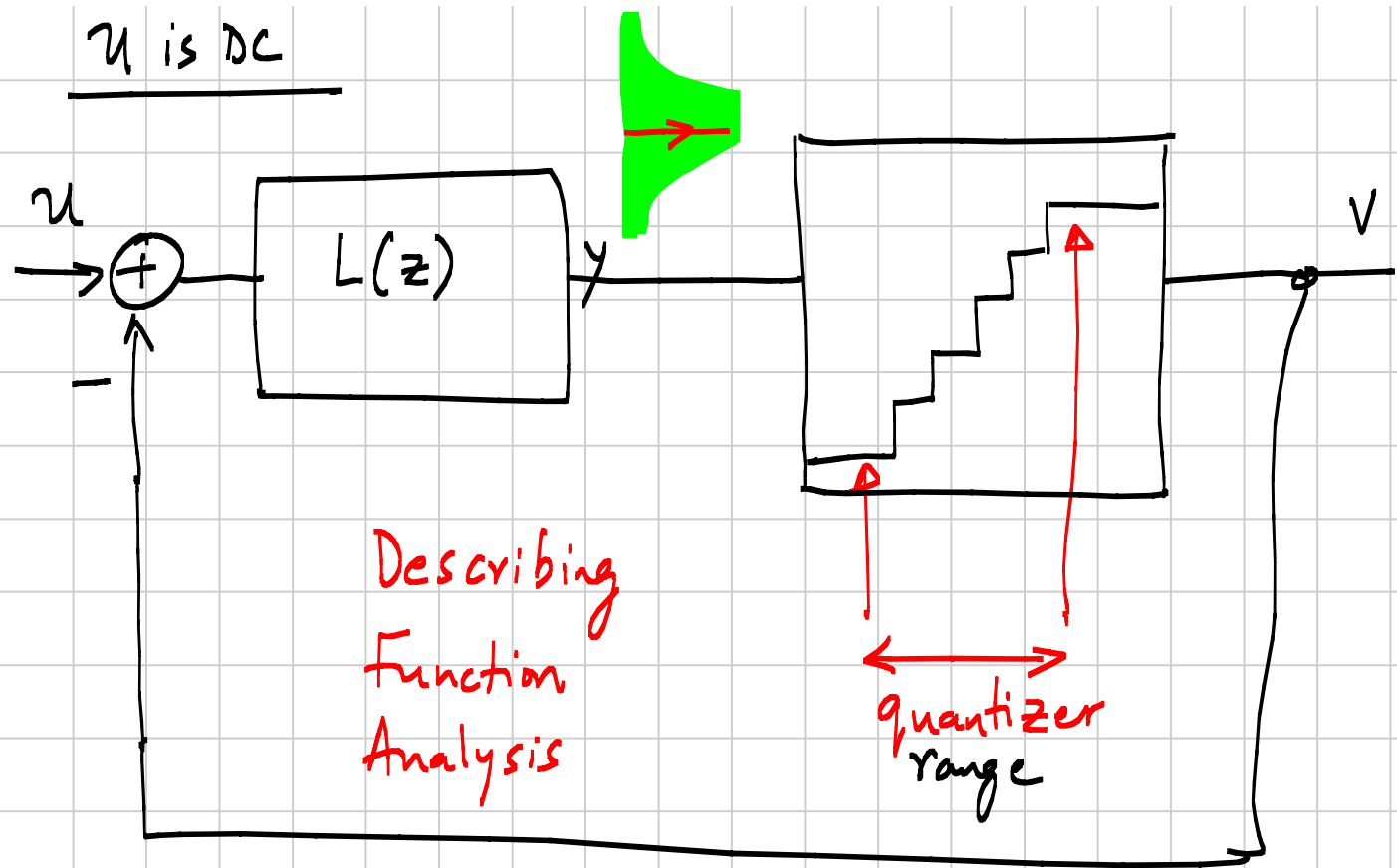
$$= (N + 0.5) \text{ bits per every doubling of the OSR}$$

Histogram of (y-u) in a Second Order $\Delta\Sigma$



$$(1 - z^{-1})^N \rightarrow 2^N$$

u is DC



$$y = y_{DC} + n_1 \Rightarrow \boxed{Q} \rightarrow v$$

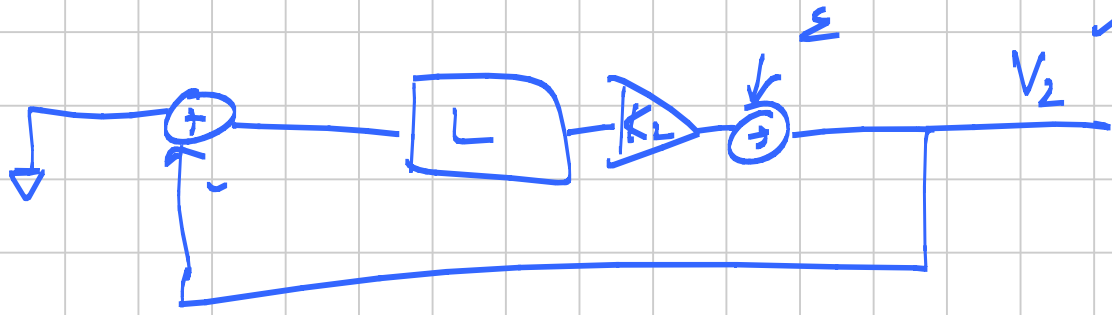
If Q was truly linear,

$$v = k_1 y_{DC} + k_2 n_1$$

$$\begin{bmatrix} y_{DC} & n_1 \end{bmatrix} \begin{bmatrix} k_1 \\ k_2 \end{bmatrix} = [v]$$

Unique k_1 & k_2

y_{DC}, n_1, v
are column
vectors



If Q was not linear,

$$V = k_1 y_{dc} + k_2 n_1 + e$$

$$\underbrace{\begin{bmatrix} y_{dc} & n_1 \end{bmatrix}}_A \underbrace{\begin{bmatrix} k_1 \\ k_2 \end{bmatrix}}_K = [v]$$

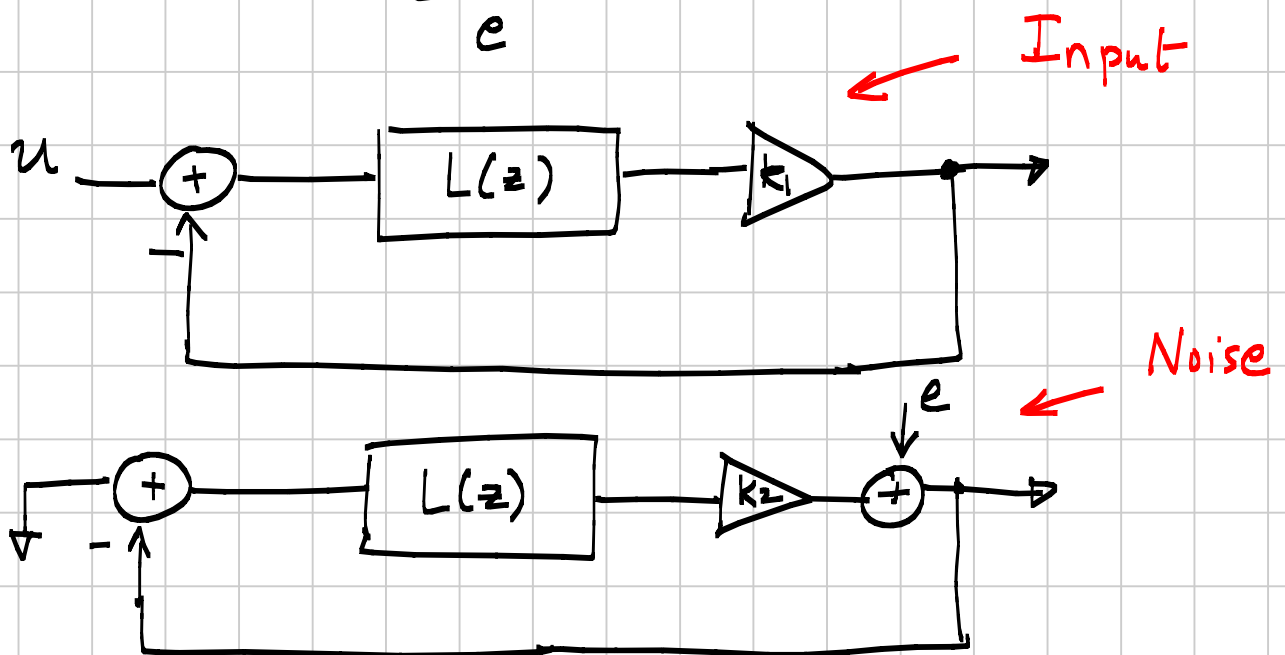
k_1 & k_2 are chosen to minimize mean square error of "e".

$$AK = V$$

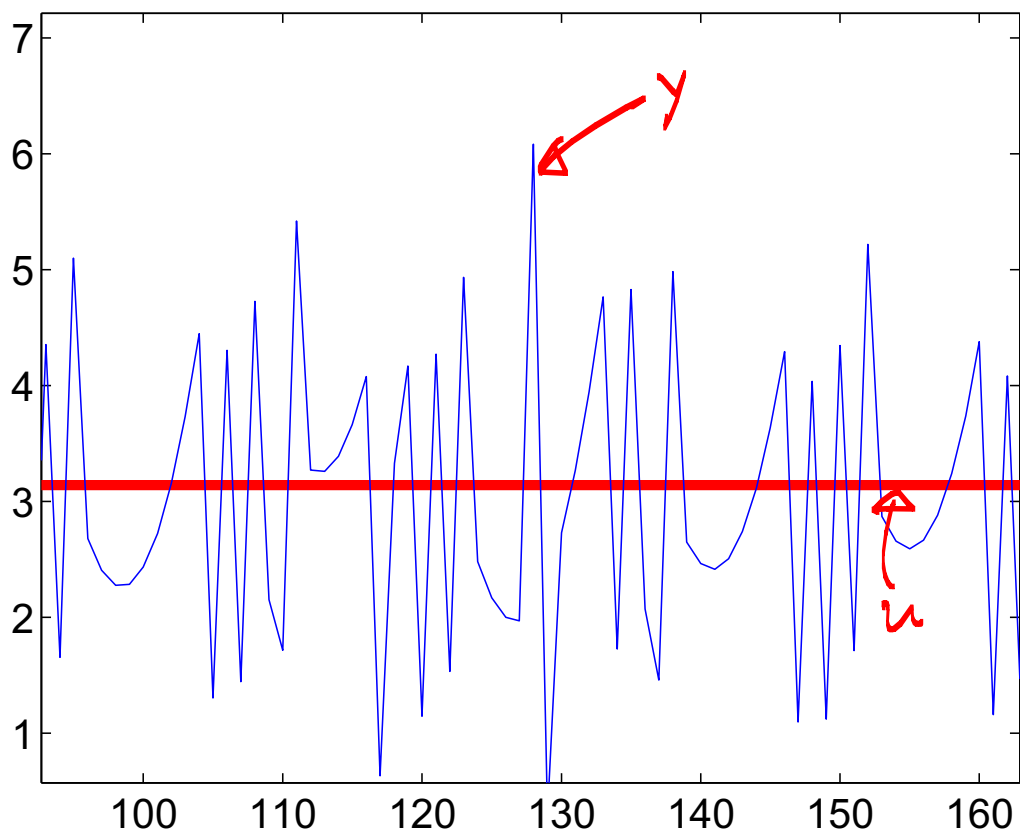
$$A^T A K = A^T V \Rightarrow K = (A^T A)^{-1} A^T V$$

K is the least squares solution to $AK = V$

$$\underbrace{(AK - V)}_e^T (AK - V)$$



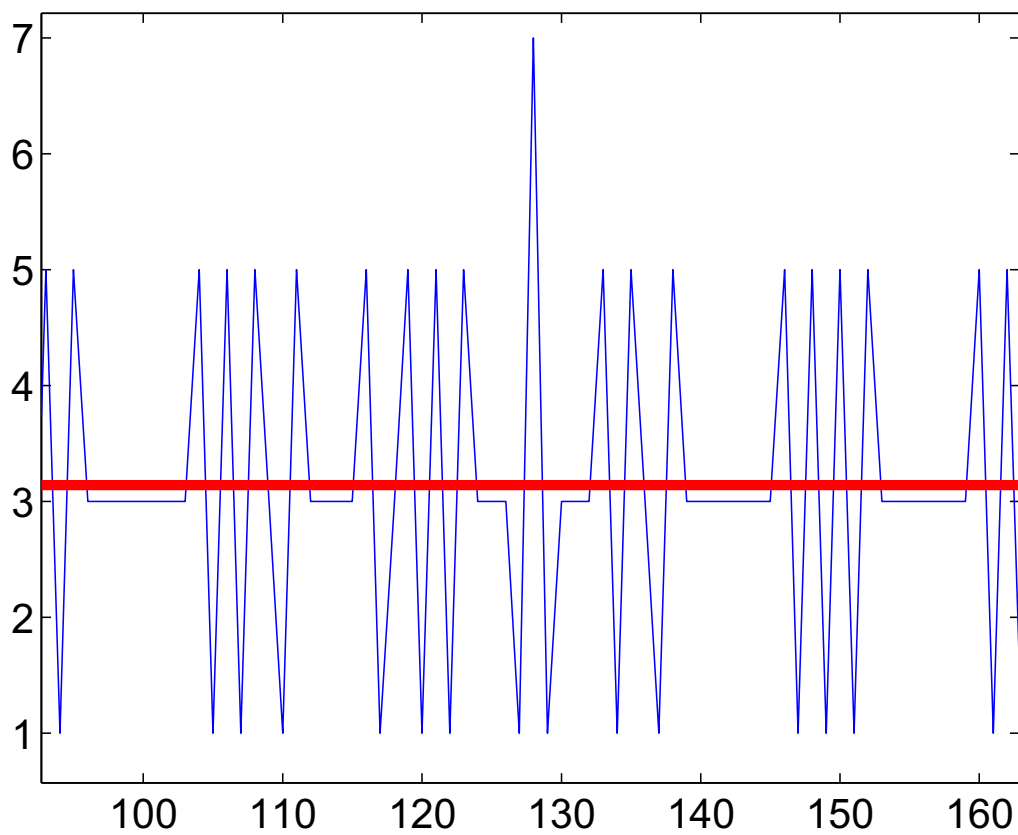
$u=3.1415$, Second Order $\Delta\Sigma$



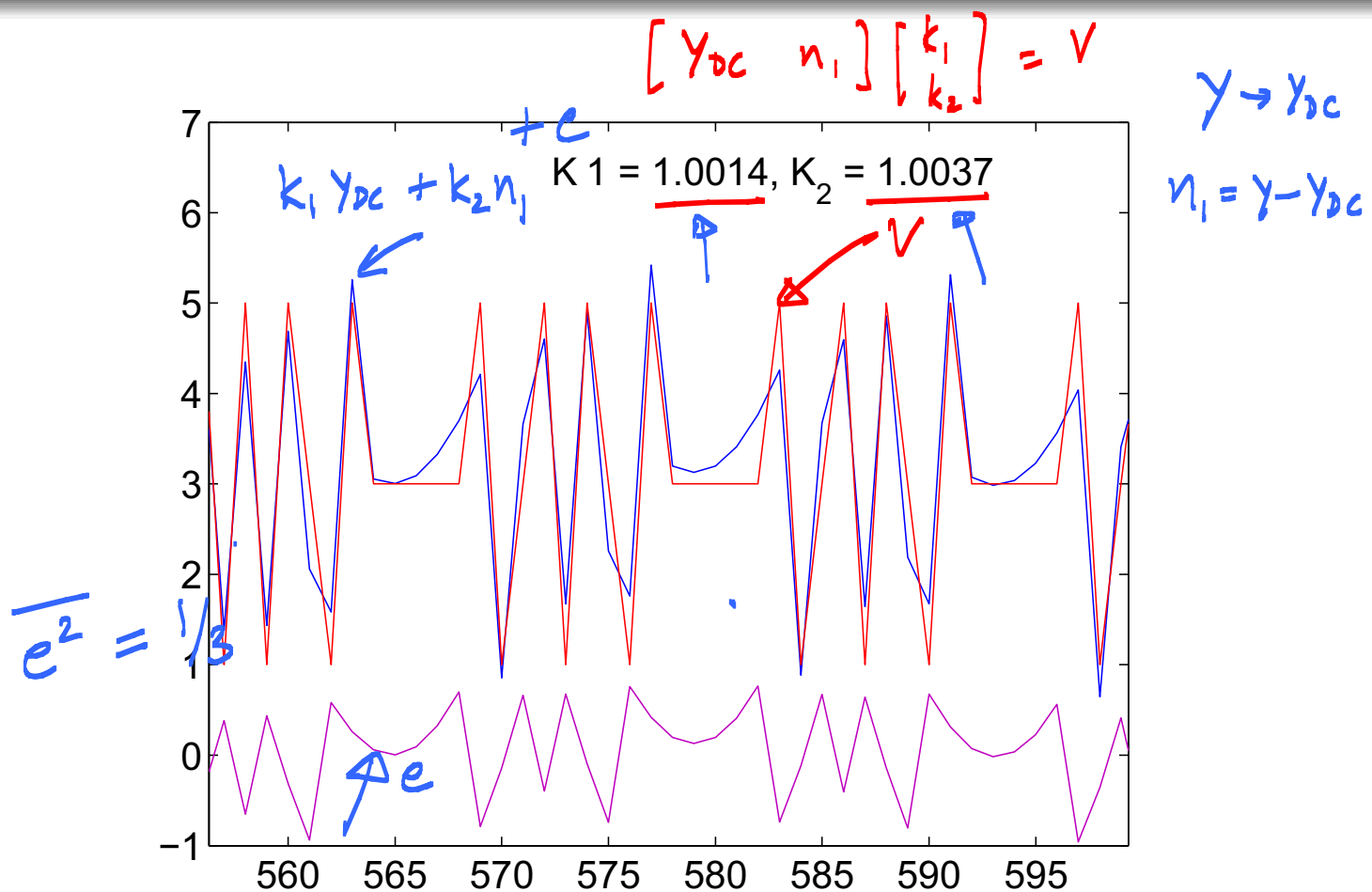
$u=3.1415$, Second Order $\Delta\Sigma$

$-7, -5, -3, -1, 1, 3, 5, 7$

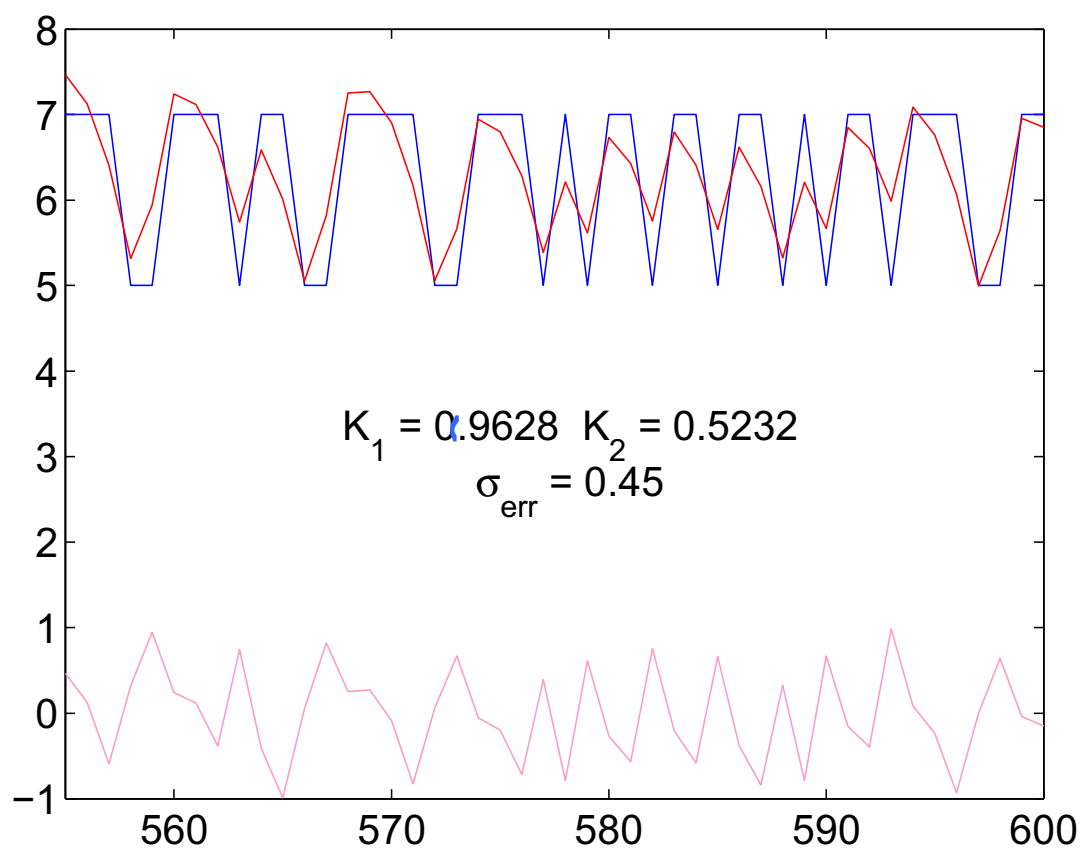
$\Delta = 2,$



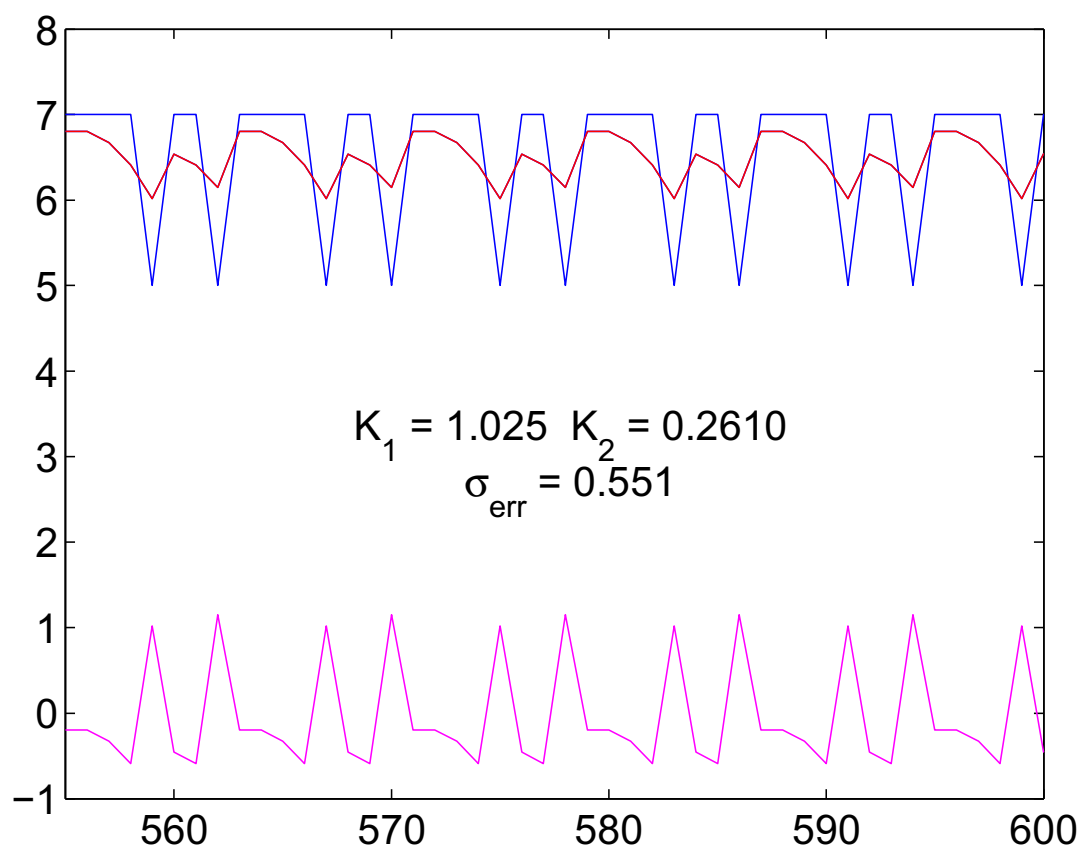
$u=3.1415$, Second Order $\Delta\Sigma$



$u=6.283$, Second Order $\Delta\Sigma$



$u=6.5$, Second Order $\Delta\Sigma$



Lecture 22

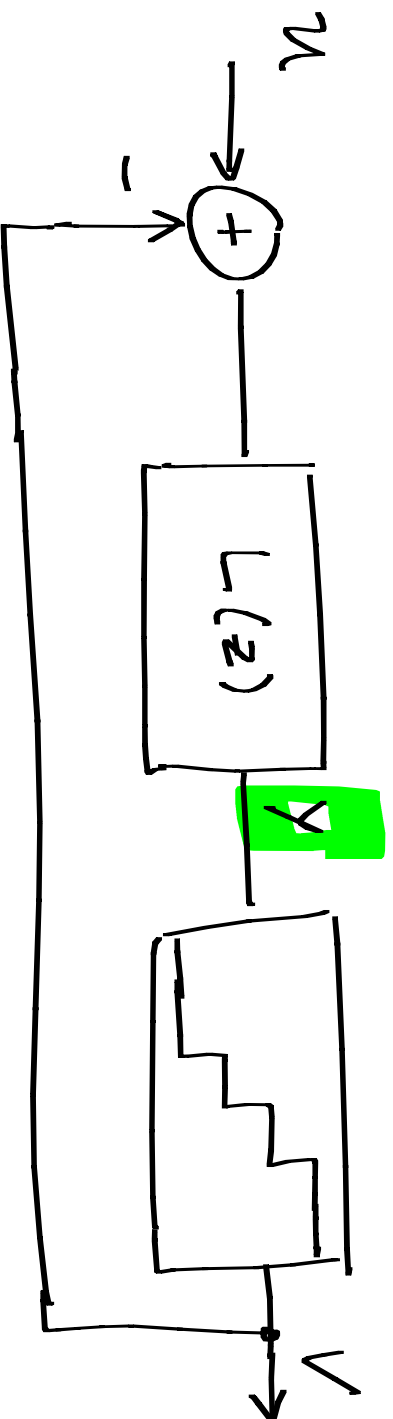
VLSI Data Conversion Circuits

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Indian Institute of Technology, Madras

February 7, 2011

Outline



* If the quantizer is ASSUMED to be an additive noise source,

$$V = \underbrace{STF}_1 u + NTF E$$

"Describing function"

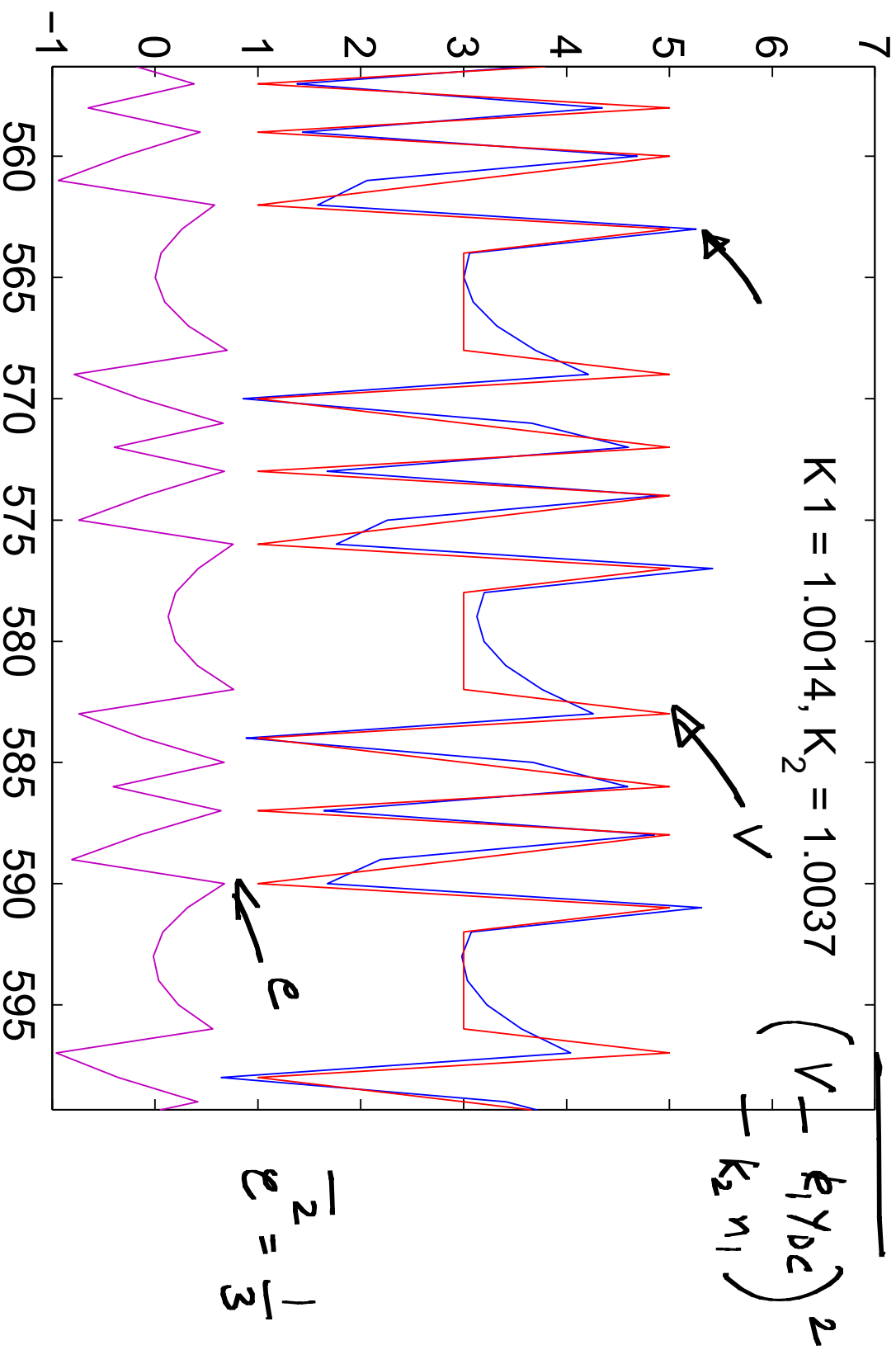
$$V = u + NTF E$$

$$\Rightarrow Y = u + (NTF - 1) E(z)$$

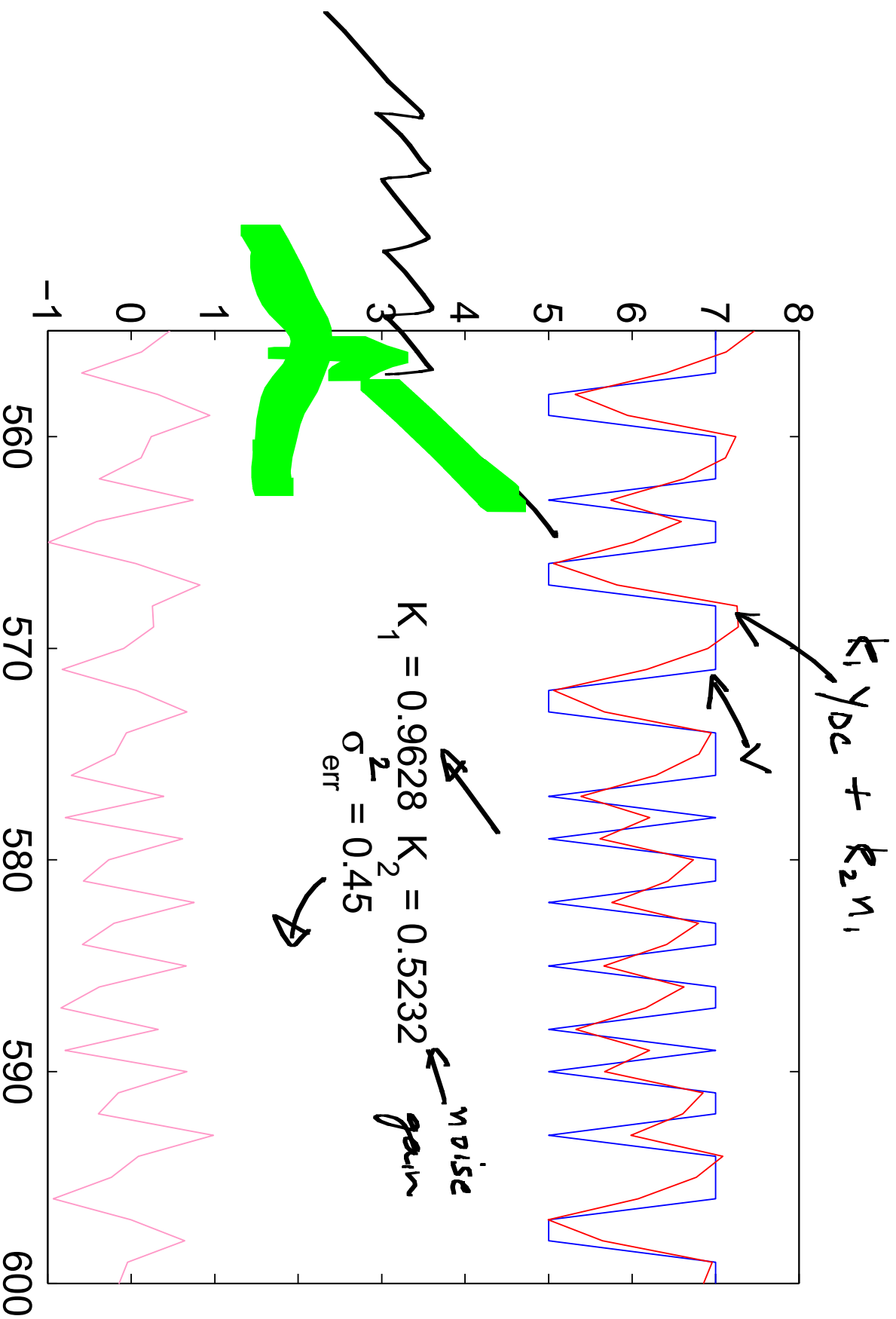
u=3.1415, Second Order $\Delta\Sigma$

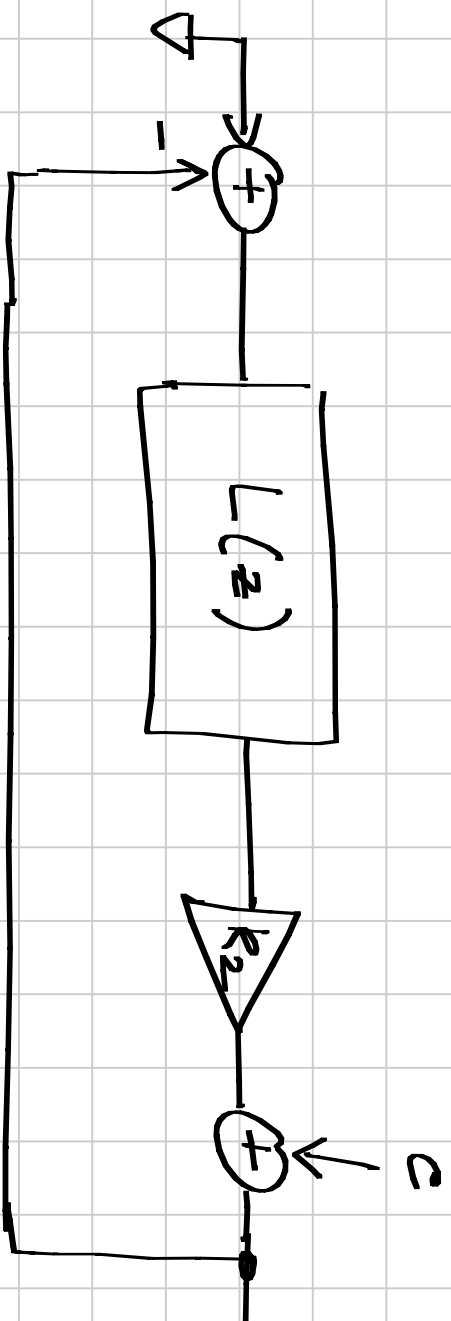
$$\Delta = 2, \quad n_1 = 8 \quad \{-7, -5, \dots, 5, 7\}$$

$$y \rightarrow y_{dc} + n_1$$



u=6.283, Second Order $\Delta\Sigma$



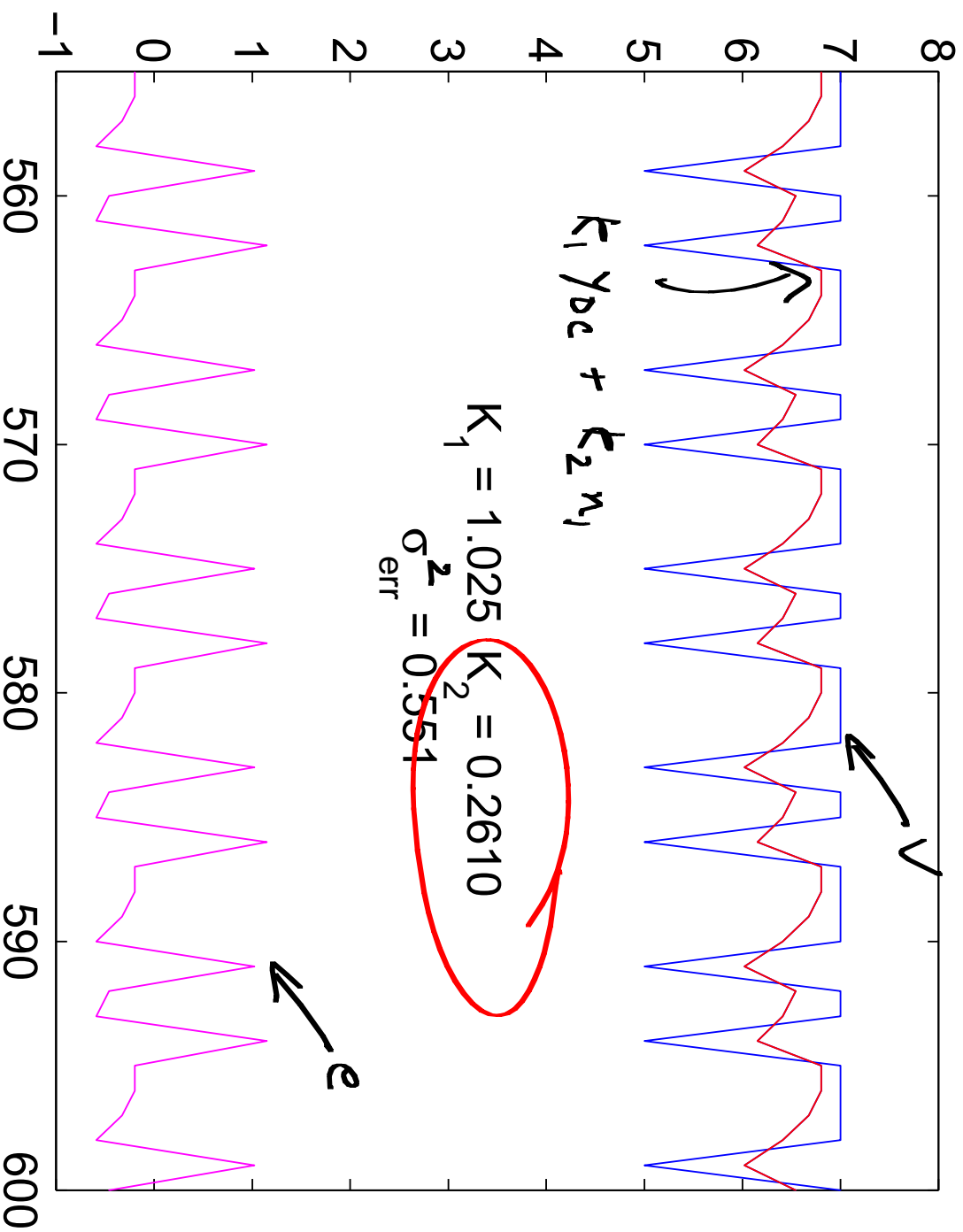


$$\frac{1}{1 + L(z)} \rightarrow \text{NTF}(z)$$

$$\text{Poles} \rightarrow 1 + \underbrace{L(z)k_2}_{=0}$$

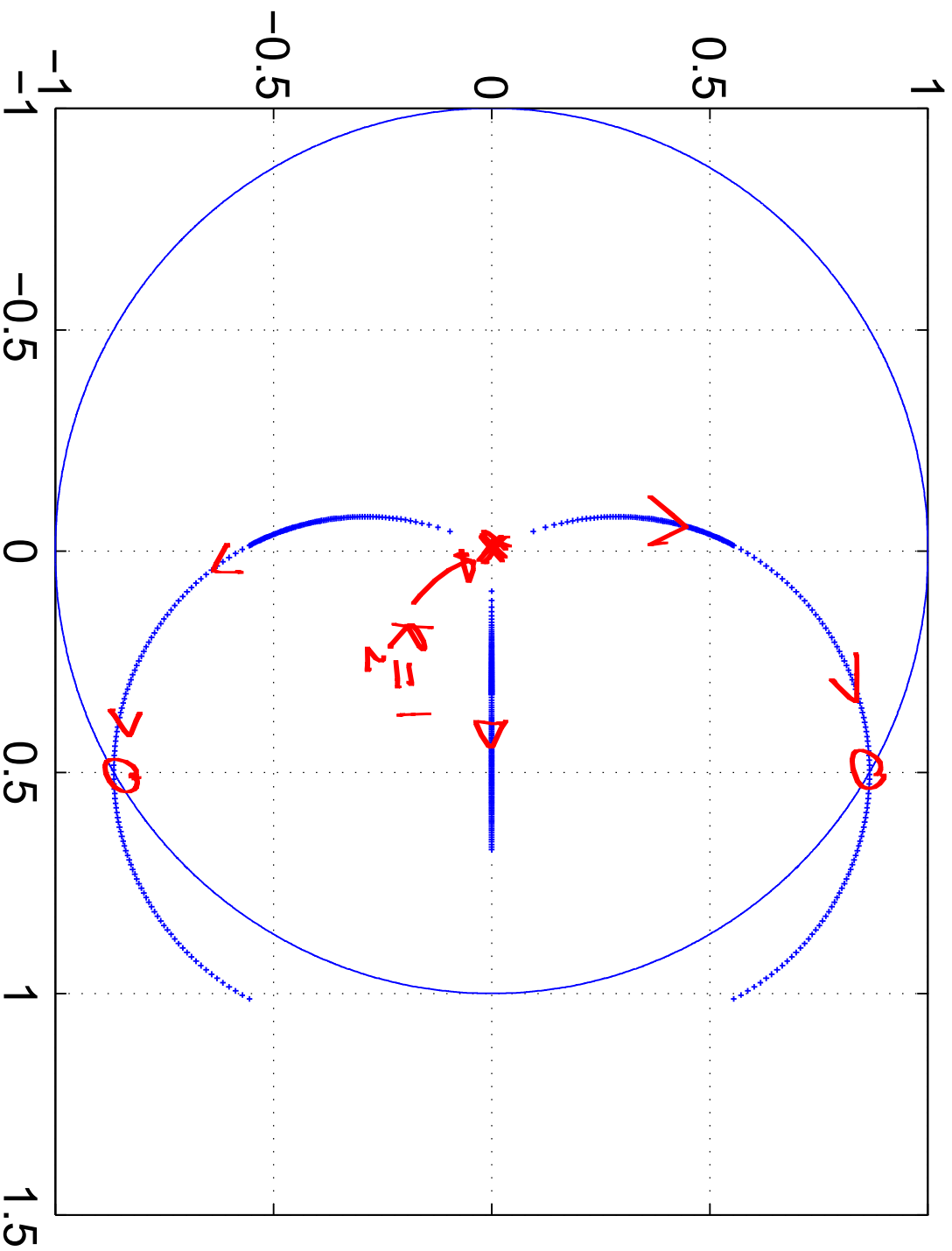
$$(1 - z^{-1})^3 = \frac{1}{1 + L(z)} \Rightarrow L(z) = \underbrace{\frac{1}{(1 - z^{-1})^3}}_{-1}$$

$u=6.5$, Second Order $\Delta\Sigma$

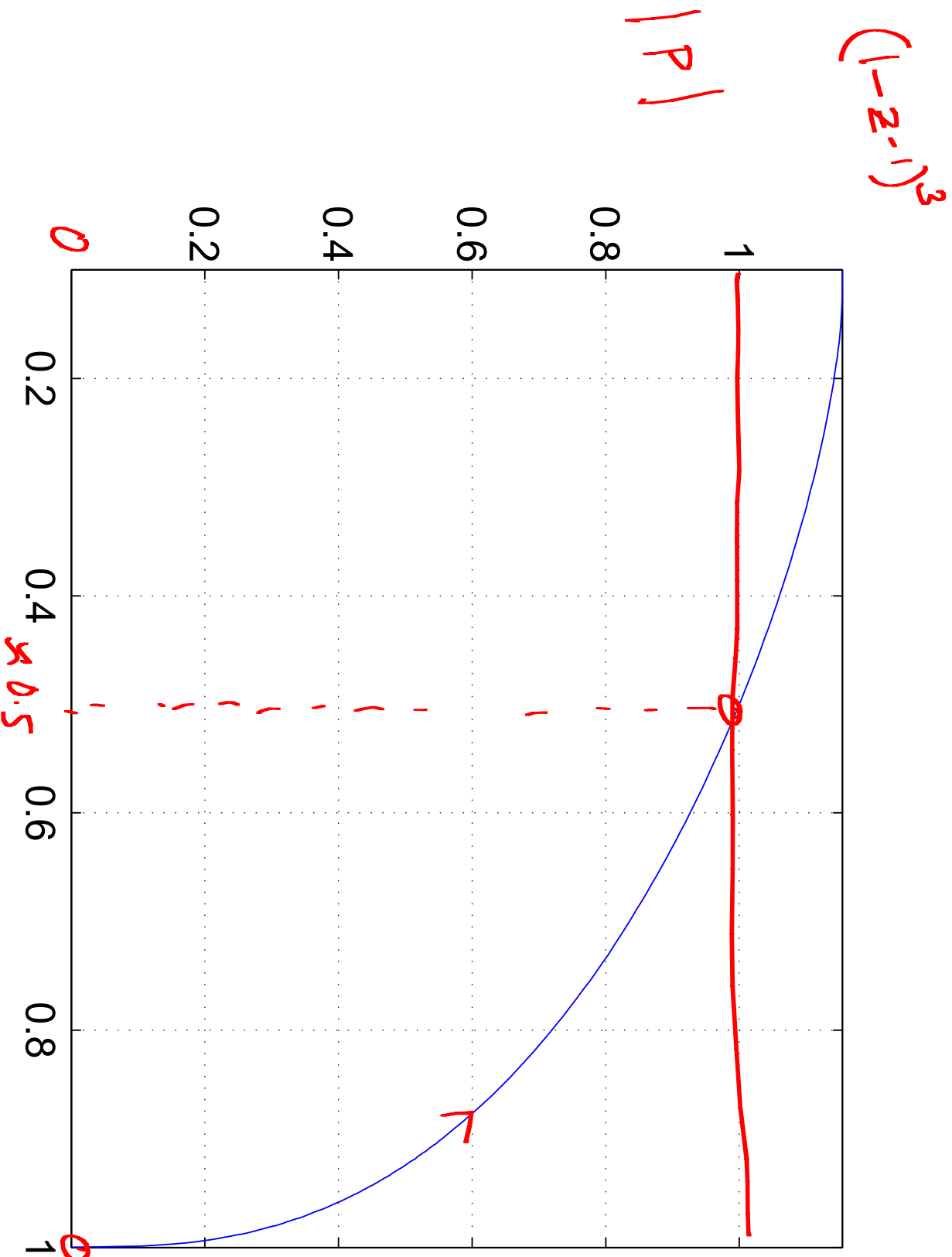


Root Locus of a Third Order $\Delta\Sigma$

$$(1 - z^{-1})^3 = \frac{(z-1)^3}{z^3}$$

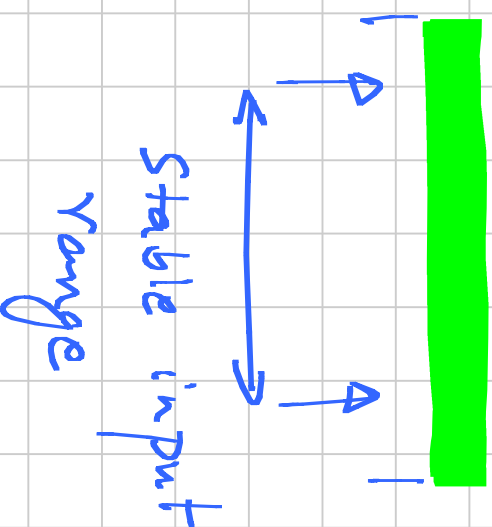
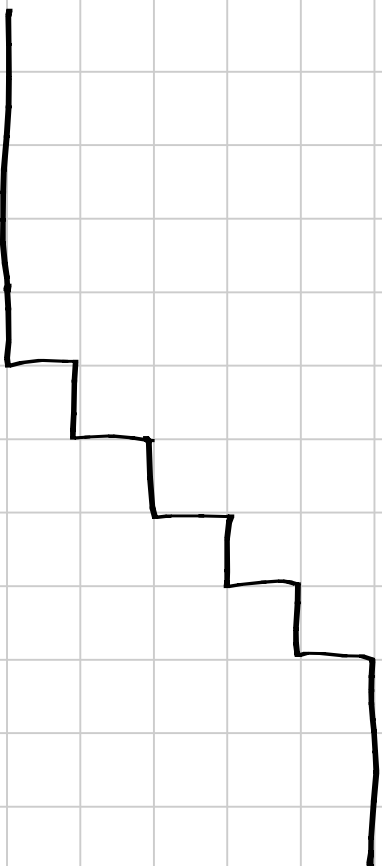


Third Order DSM : $|p|$ versus Quantizer Gain



Signal level dependent stability

$$\left[(1-2^{-1})^N \right]$$



$$\frac{\text{Stable range}}{\text{Quantizer range}} = \text{MSA}$$



Maximum

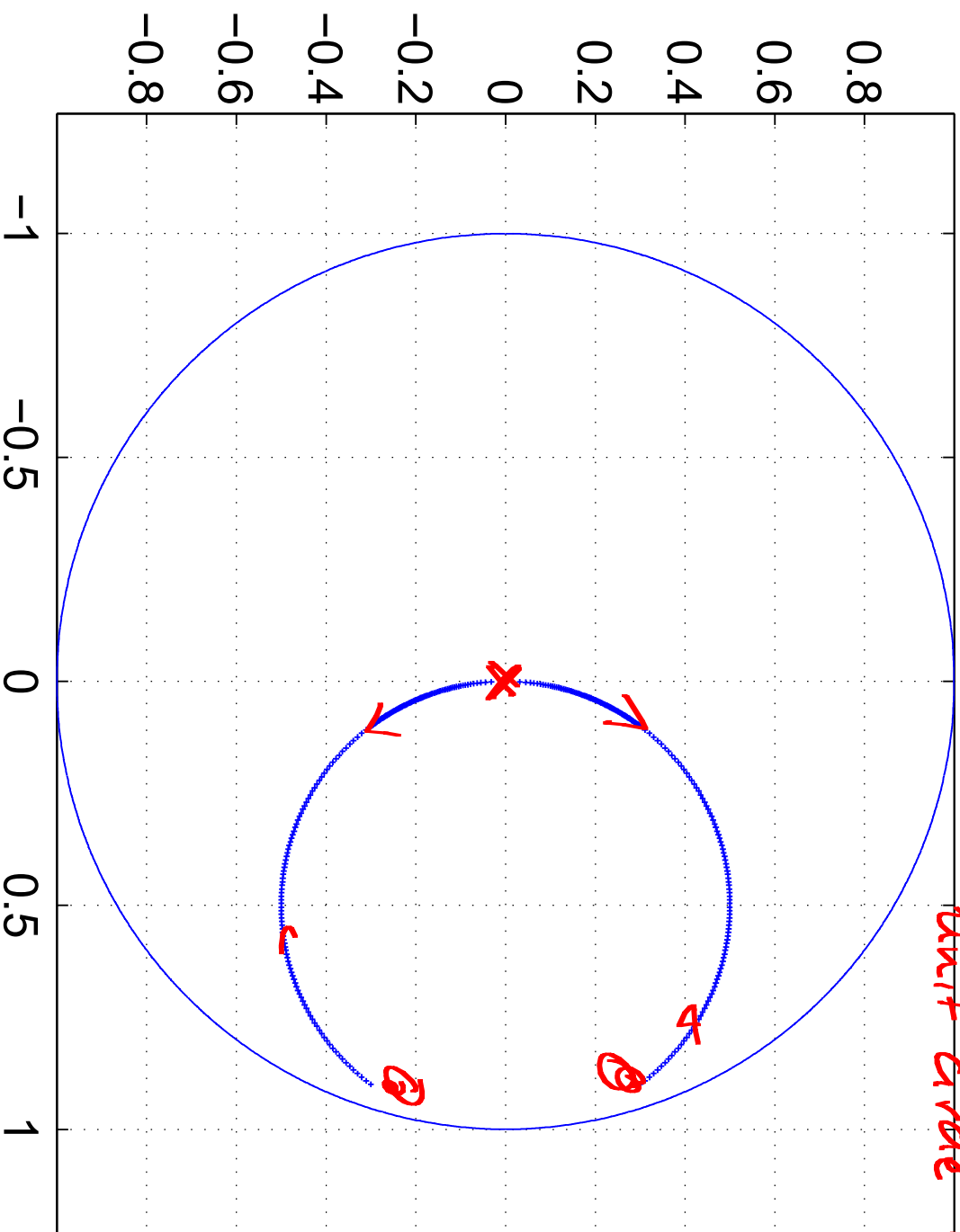
Stable

Amplitude

Root Locus of a Second Order $\Delta\Sigma$

$$NTF = (1 - z^{-1})^2 \quad k_2 = 1,$$

Poles are within the unit circle for all k_2 .

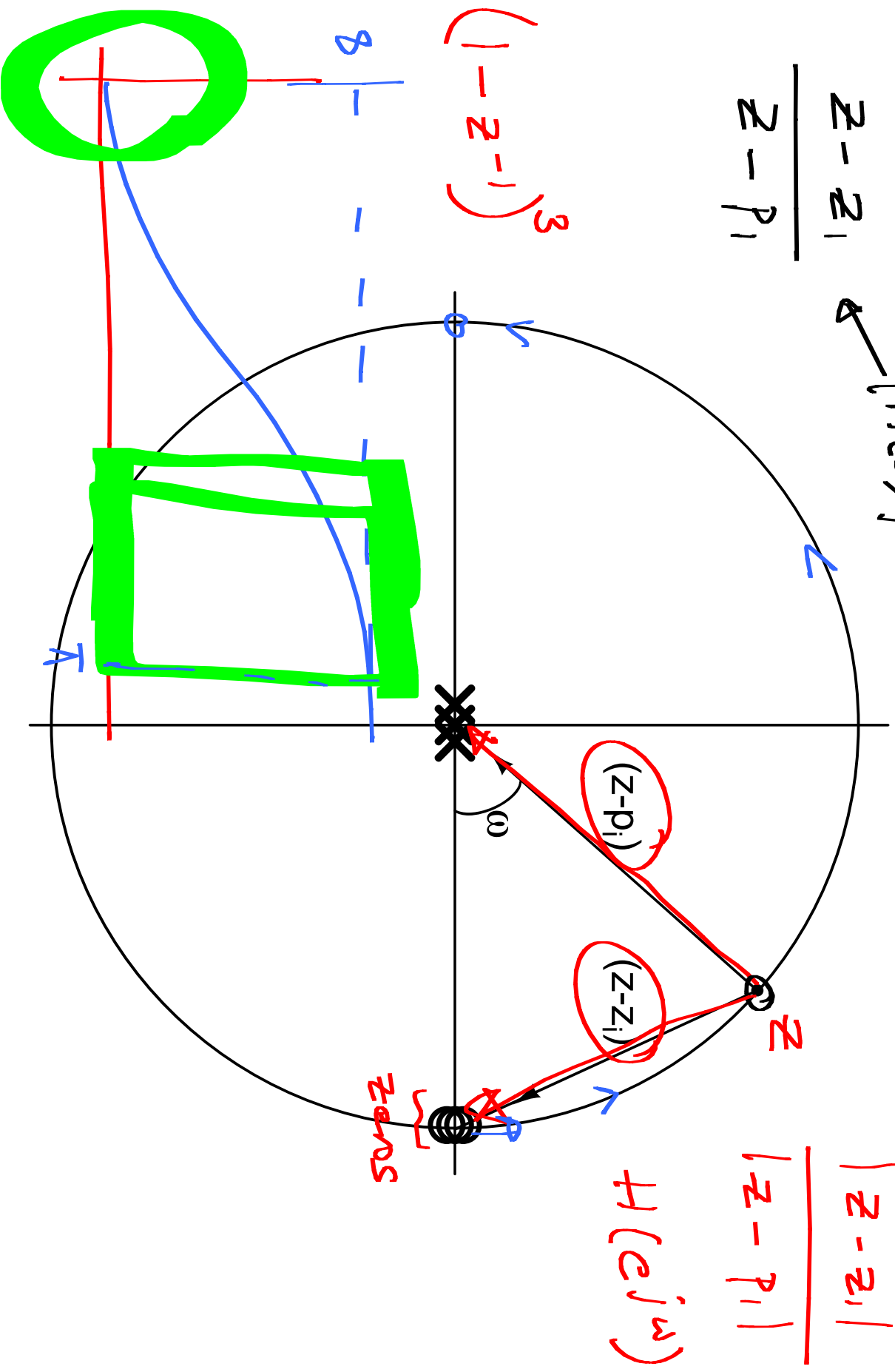


Pole-zero Plots

$$\frac{z - z_1}{z - p_1} \quad \leftarrow [H(z)]$$

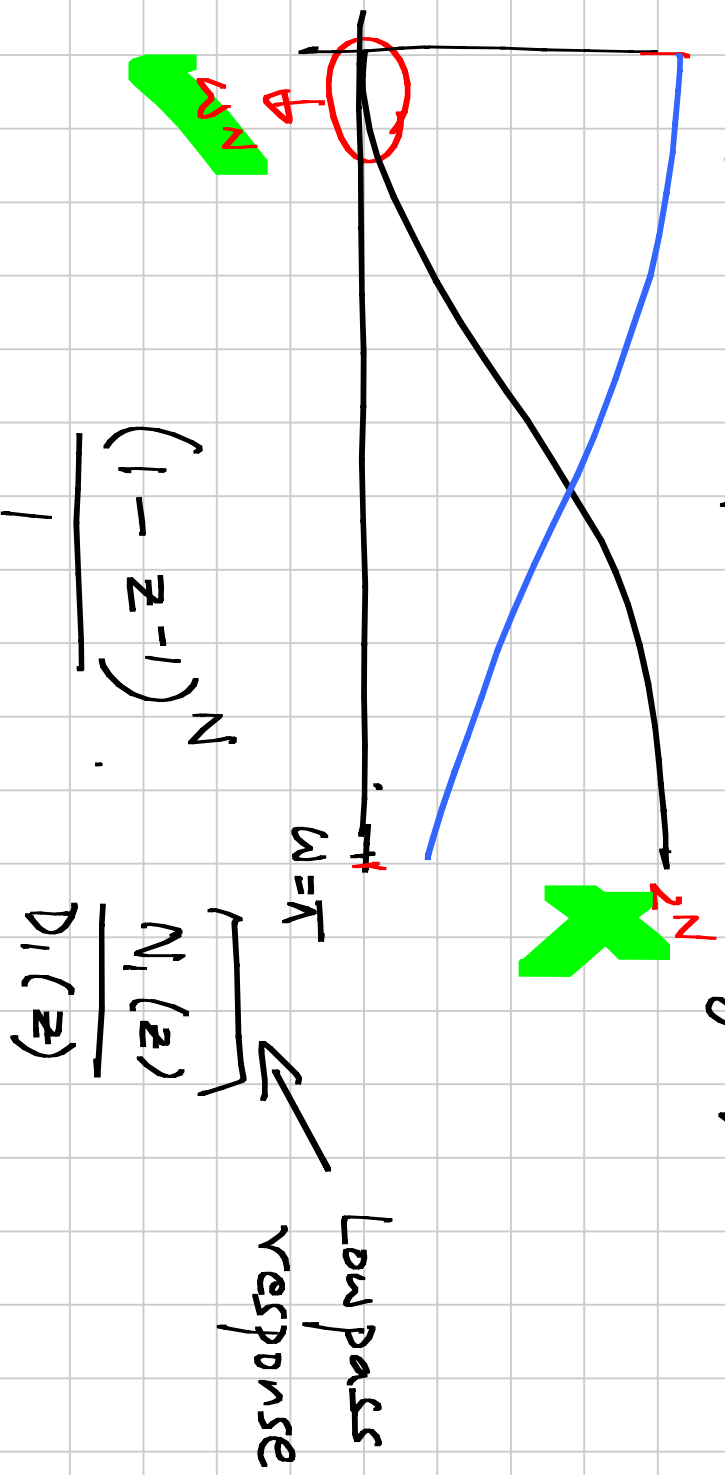
$$\frac{|z - z_1|}{|z - p_1|}$$

$$H(e^{j\omega})$$



VLSI Data Conversion Circuits: Lecture 23

* Amplitude dependent stability of a SDN

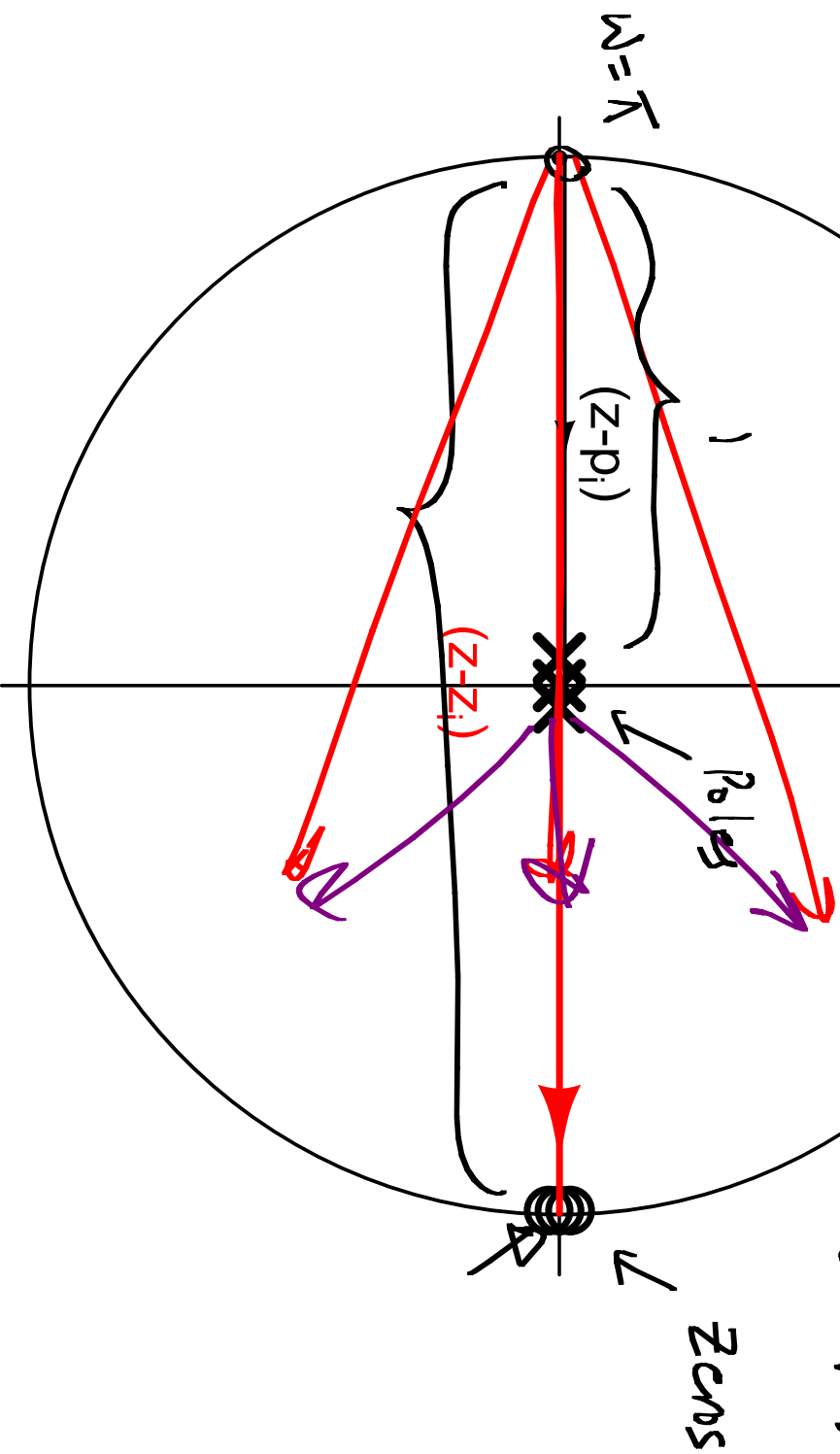


Pole-zero Plots

$$(1 - z^{-1})^3 = \frac{(z - 1)^3}{z^3}$$

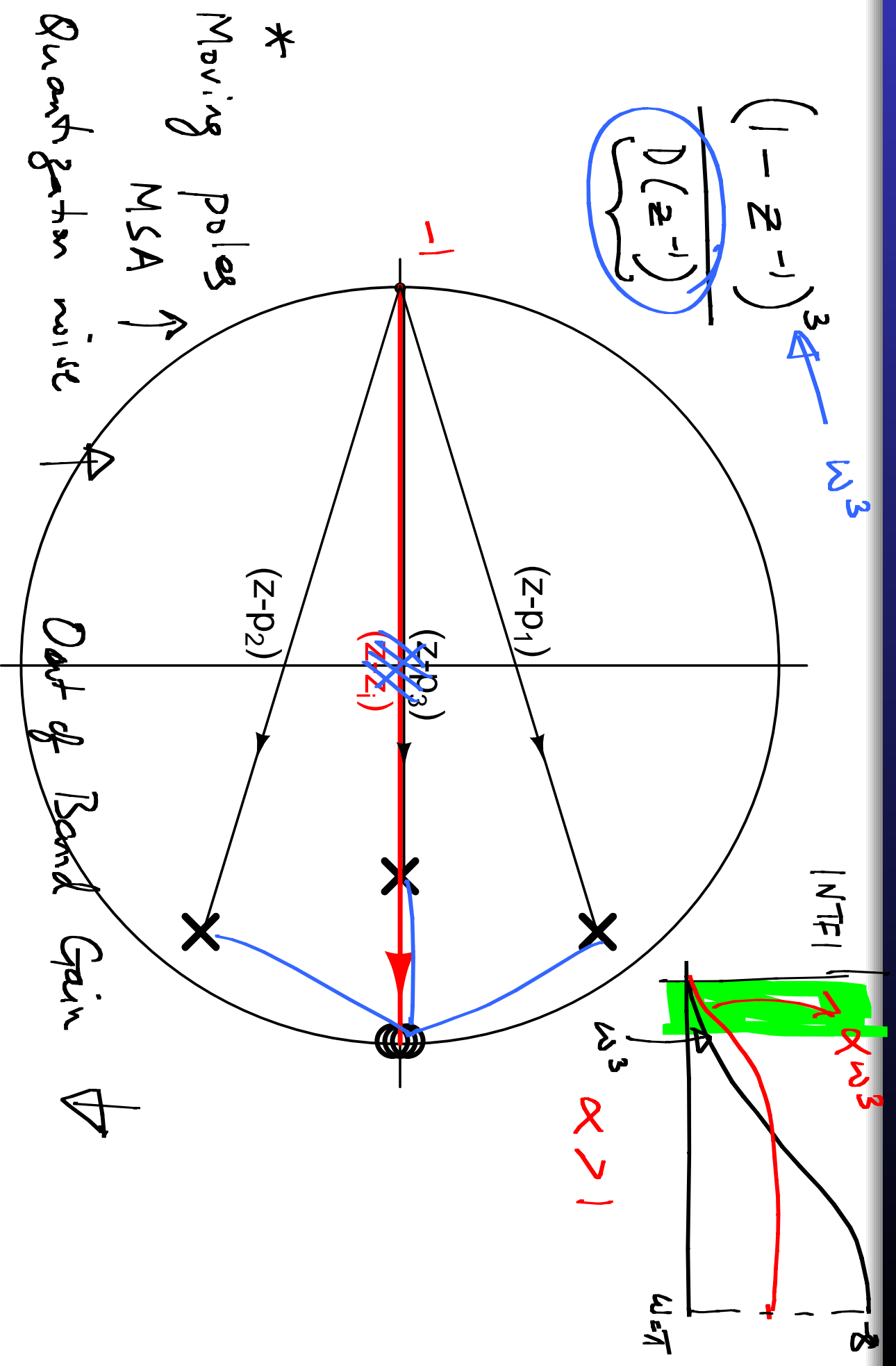
$$|NTF(\pi)|$$

$$\frac{8}{(1 - p_1) \cdots (1 - p_3)}$$

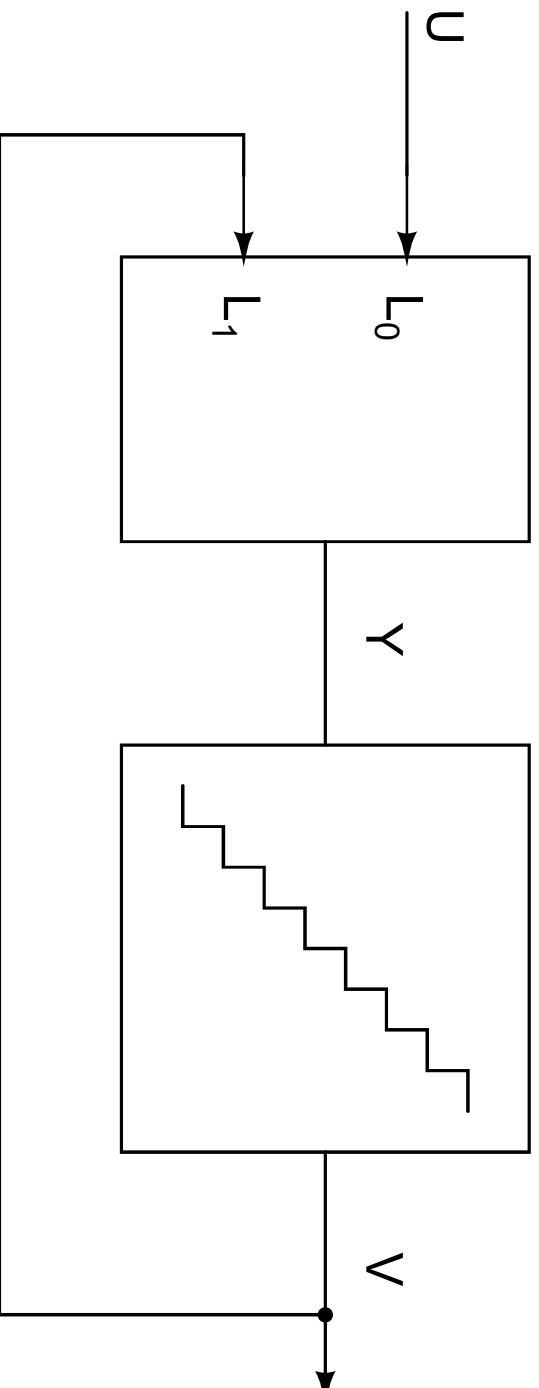




Pole-zero Plots

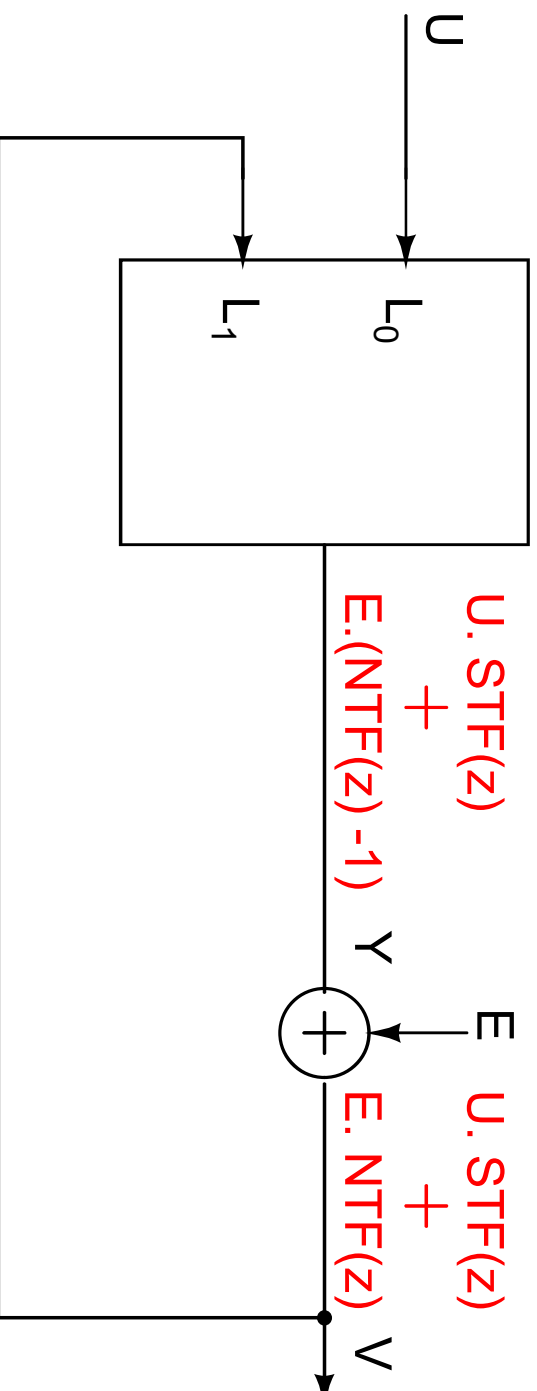


Stability of $\Delta\Sigma$ Modulators



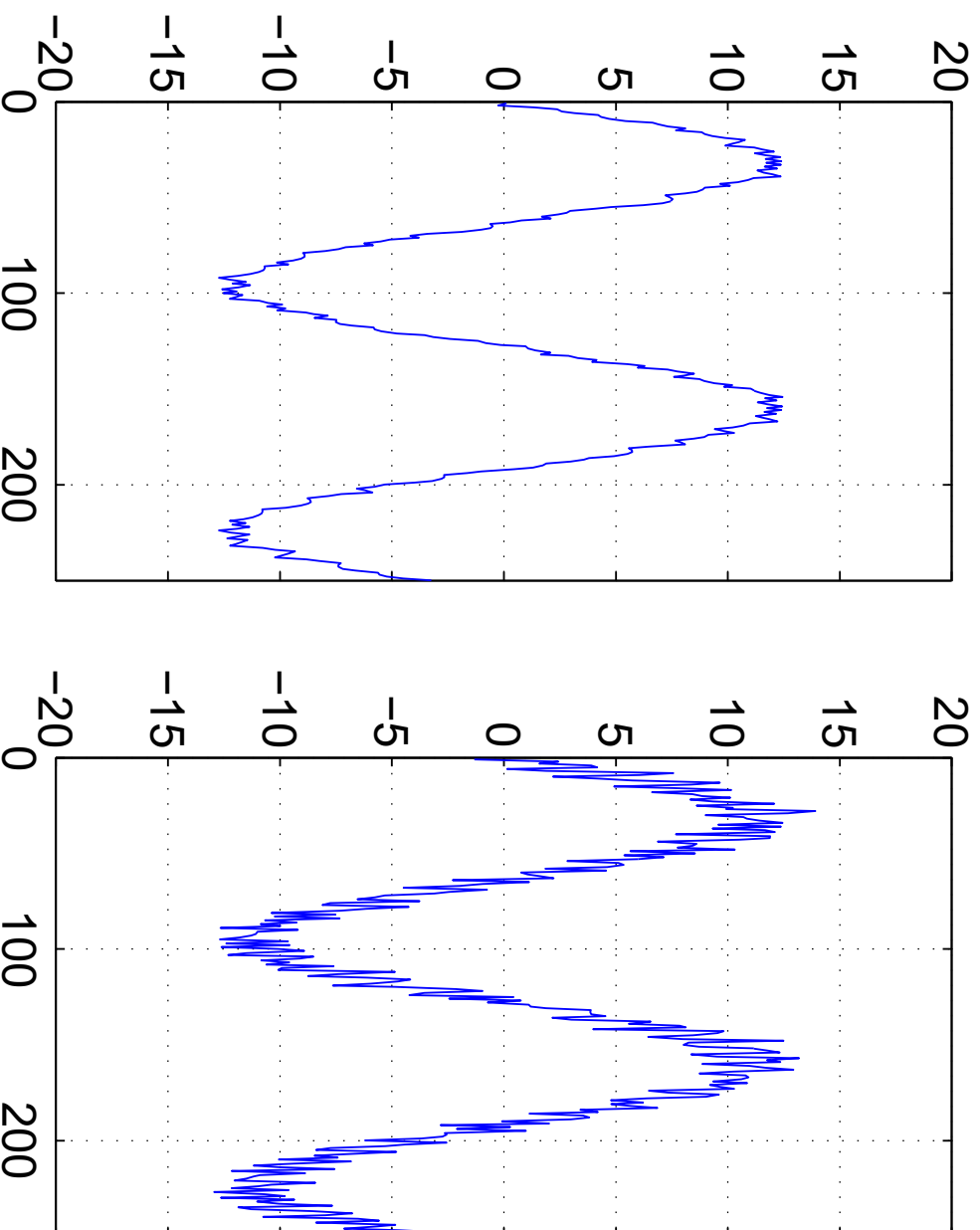
- $Y(z) = L_0(z)U(z) + L_1(z)V(z)$
- v is the quantized version of y .

Stability of $\Delta\Sigma$ Modulators



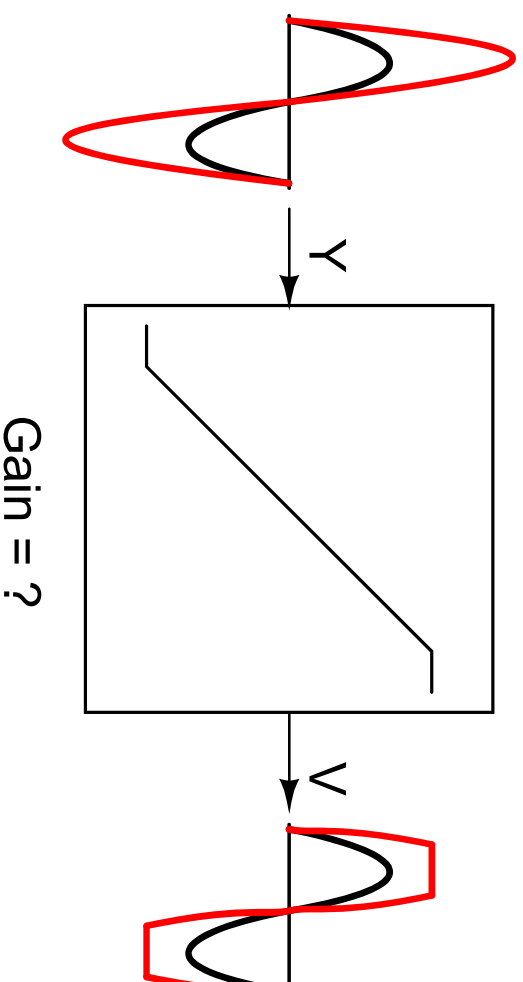
- Quantizer is modeled as an additive noise source.
- $V(z) = U(z)STF(z) + E(z)NTF(z)$
- $Y(z) = U(z)STF(z) + E(z)(NTF(z) - 1)$
- In the signal band, $STF(z) \approx 1$
- Quantizer Input $\approx$ (ADC input) + (Shaped Noise)

Stability of $\Delta\Sigma$ Modulators



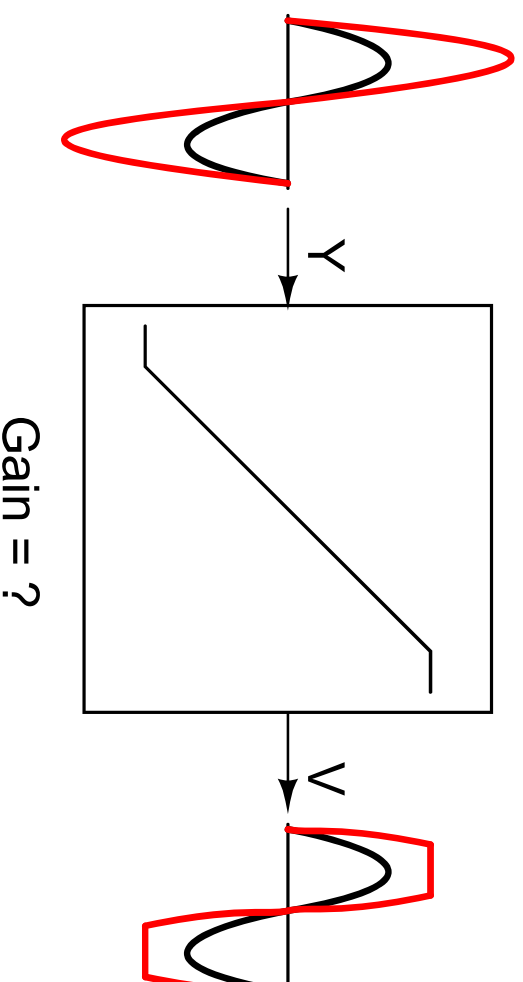
- Quantizer input for OBG=1.5 and OBG=3.5

Gain of a Nonlinear Characteristic



- Assume an infinite precision quantizer with saturation.
- What is its gain ?
- Gain depends on signal.
- Black sinewave : Gain = 1
- Red sinewave : Gain < 1

Gain of a Nonlinear Characteristic



- $Gain = \frac{E(v.y)}{E(y.y)}$.
- Makes intuitive sense.
- $E(v.y)$ is the average value of $v.y$.
- $E(v.y)$ is a measure of how much the output “resembles” the input.

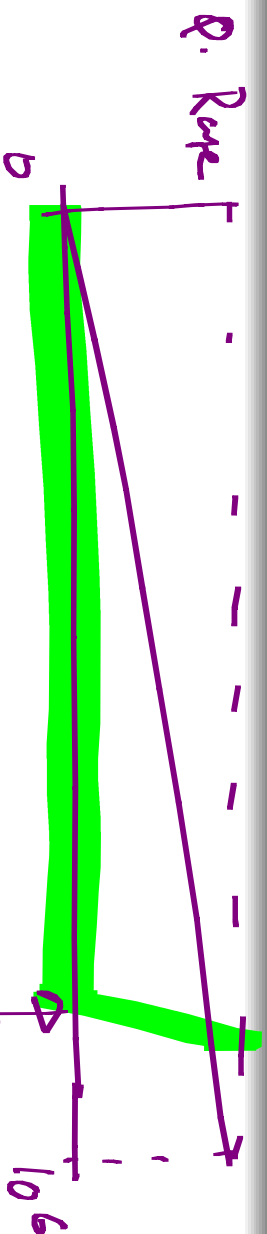
Intuition about Loop Stability

- Loop becomes unstable if the quantizer saturates.
- Saturation occurs if the quantizer input exceeds the quantizer range.
- Quantizer Input = ADC Input + Shaped Noise.
- Conclusions -
 - The maximum ADC input **must be smaller** than the quantizer range. (called the Maximum Stable Amplitude (MSA)).
 - More “shaped” noise → More likelihood of instability.
- More shaped noise → Lesser in-band noise.
- An aggressive NTF will have a reduced MSA.

Estimating Maximum Stable Amplitude (MSA)

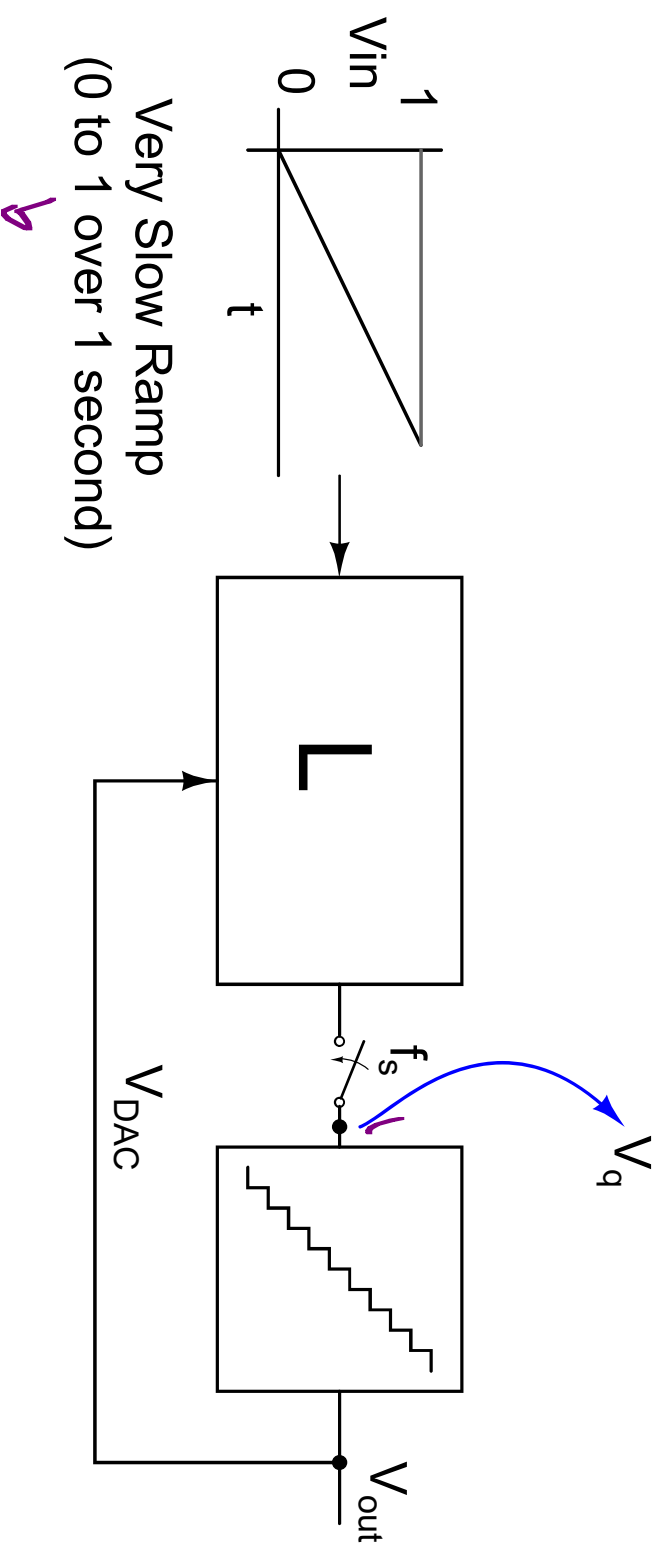
- Simulation is the best way.
- Keep stepping up the input sinewave amplitude.
 - For every amplitude, compute in-band SNR.
 - Beyond the MSA, the closed loop poles move out of the unit-circle.
 - Noise shaping is lost $\Rightarrow$ In-band SNR falls.
 - Quantizer input tends to infinity.
- Time consuming.

Estimating MSA Without Sinewave Inputs

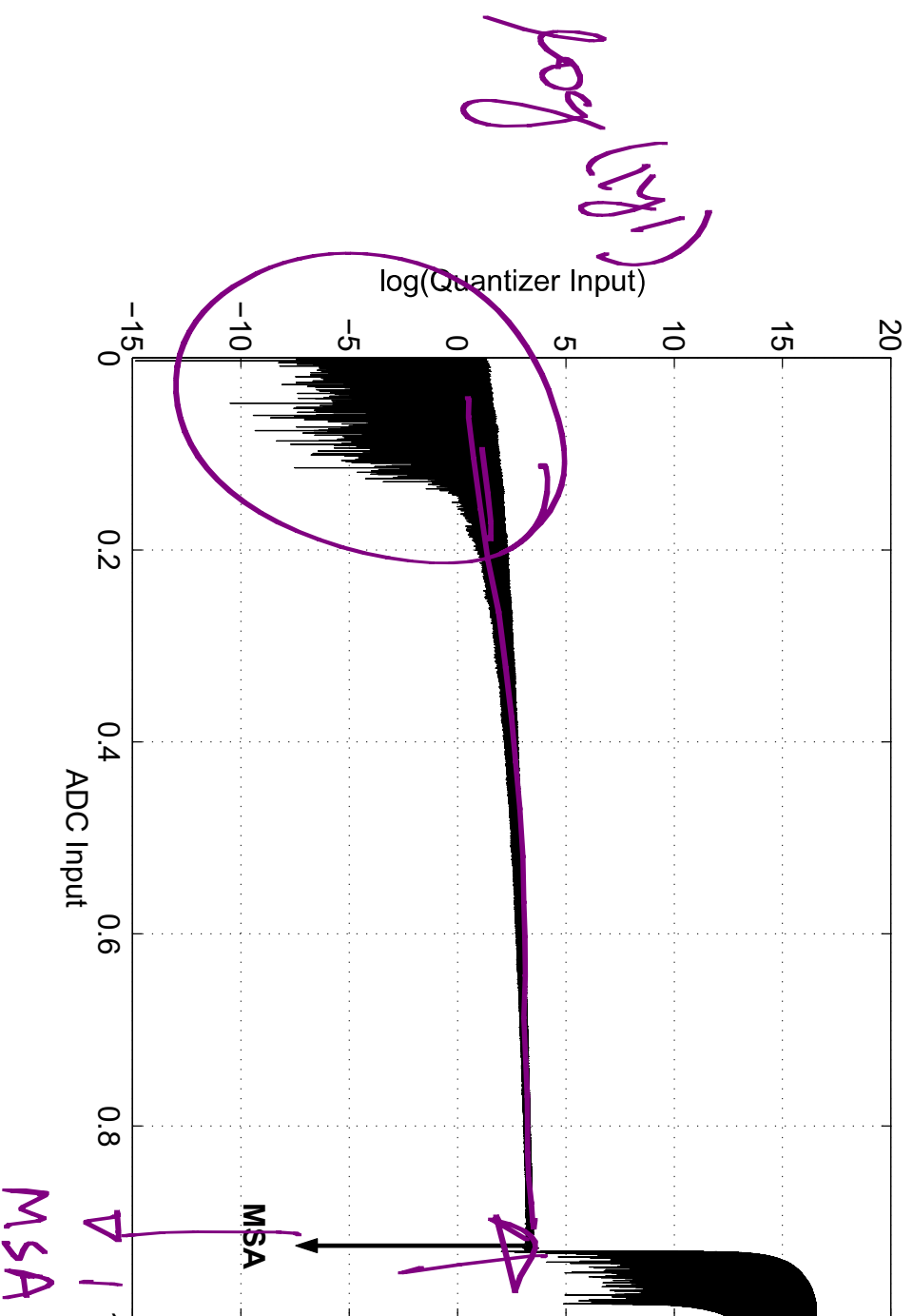


- Originally proposed by Lars Risbo.
- Put a slowly increasing ramp into the ADC.
 - Beyond the MSA, the closed loop poles move out of the unit-circle.
 - Quantizer input tends to infinity very rapidly.
 - The value of the ADC input when the quantizer input *blows up* is the MSA.
- Found (empirically) to result in an MSA close to that predicted by the sinewave method.
- Much quicker than the sinewave technique.

Estimating MSA Without Sinewave Inputs

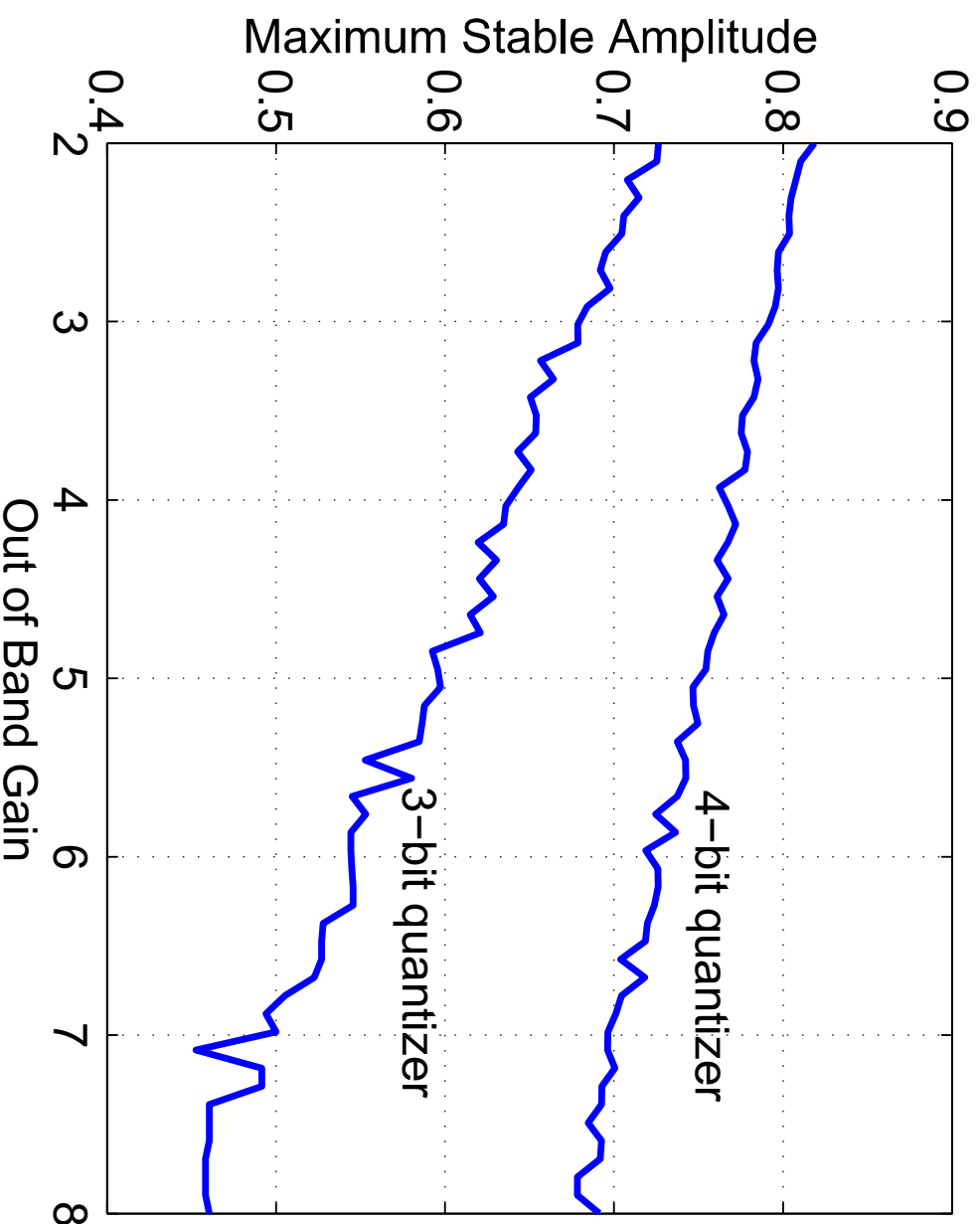


Estimating MSA Without Sinewave Inputs

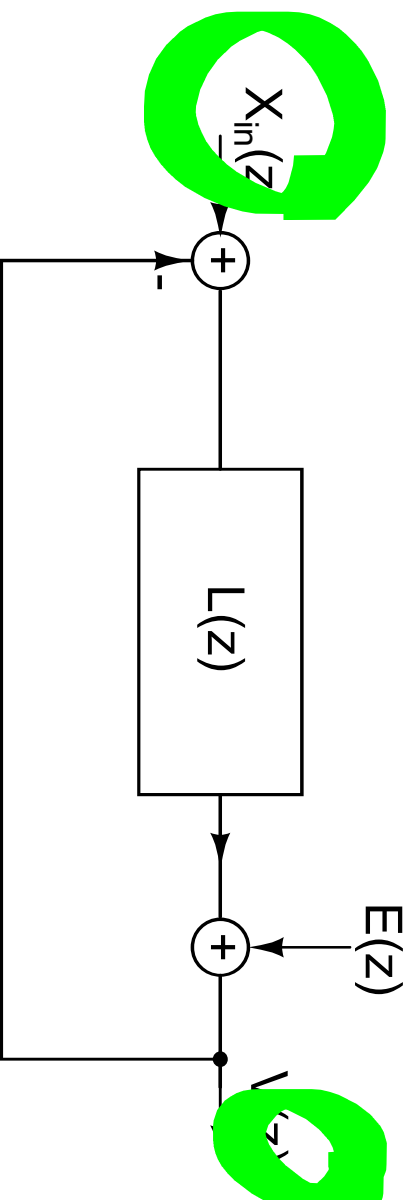


log(Quantizer Input) versus ADC Input
MSA is about 90% of the quantizer range

MSA vs OBG for a Third Order NTF

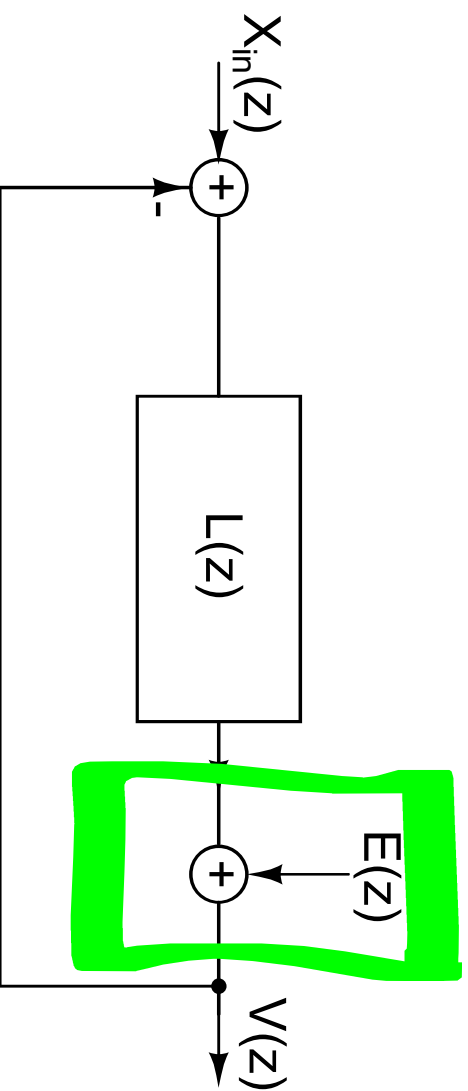


The Sensitivity of a Feedback Loop



- E is a disturbance injected into the feedback loop.
- $V(z) = X(z) \frac{L(z)}{1+L(z)} + E(z) \frac{1}{1+L(z)}$.
- If $L(z) \rightarrow \infty$, then $V(z) \rightarrow X(z)$.
- The loop rejects $E(z)$, or the loop is *insensitive* to $E(z)$.

The Sensitivity of a Feedback Loop



- $L(z)$ cannot be ∞ at all frequencies.
- $V(z) = X(z) \frac{L(z)}{1+L(z)} + E(z) \frac{1}{1+L(z)}$.
- The loop rejects E at frequencies where the loop gain is high.

- How effectively this is done is called the sensitivity function.
- Sensitivity is $\frac{1}{1+L(e^{j\omega})}$

The Sensitivity of a Feedback Loop

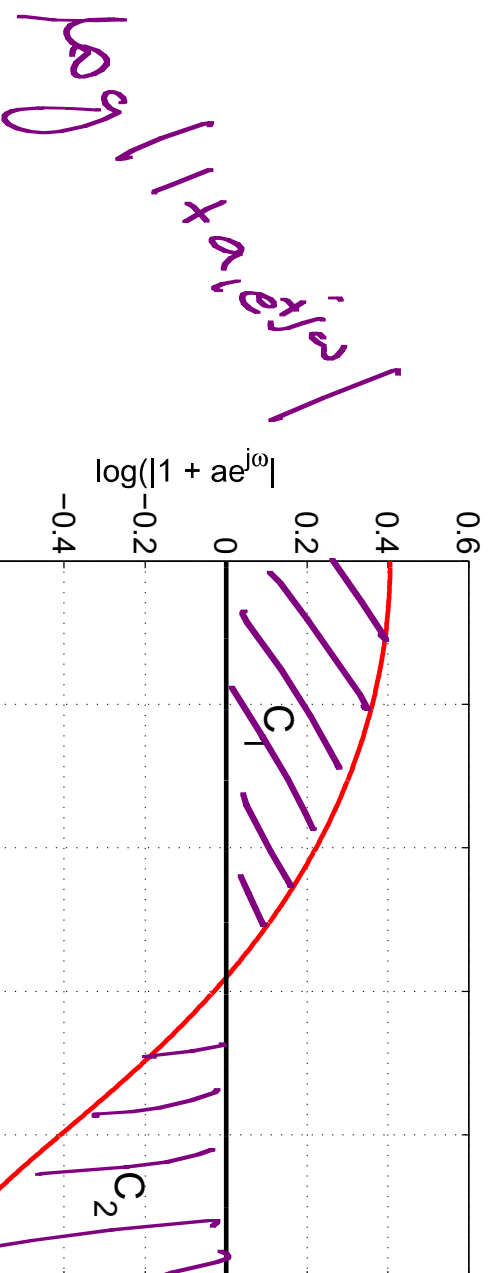
- In a $\Delta\Sigma$ loop, sensitivity is the same as the NTF.
- Recall: The first sample of the NTF impulse response is 1.
- Equivalent to $NTF(\infty) = 1$
- The NTF can be written as

$$\frac{(1+a_1z^{-1})(1+a_2z^{-1}+a_3z^{-2})\dots}{(1+b_1z^{-1})(1+b_2z^{-1}+b_3z^{-2})\dots}$$
- Poles must be within the unit circle (for a stable loop).
- The zeroes are on the unit circle (or inside).

The Sensitivity of a Feedback Loop

- It can be shown that $\int_0^\pi \log(|1 + a_1 e^{-j\omega}|) d\omega = 0$, if $|a_1| \leq 1$.

$$1 + a_1 z^{-1}$$



The area above the 0dB in the log magnitude plot is equal to the area below the 0dB line.

The Sensitivity of a Feedback Loop

- $\int_0^\pi \log(|1 + a_2 e^{-j\omega} + a_3 e^{-j2\omega}|) d\omega = 0$
if the roots of $1 + a_2 z^{-1} + a_3 z^{-2}$ lie within (or on) the unit circle.
- Straightforward to derive, if one accepts the previous result.

The Sensitivity of a Feedback Loop

$$\int_0^\pi \log |NTF(e^{j\omega})| d\omega \neq \int_0^\pi \log \left| \frac{(1 + a_1 e^{-j\omega})(1 + a_2 e^{-j\omega} + a_3 e^{-2j\omega}) \dots}{(1 + b_1 e^{-j\omega})(1 + b_2 e^{-j\omega} + b_3 e^{-2j\omega}) \dots} \right| d\omega$$

$$\int_0^\pi \log(|1 + a_1 e^{-j\omega}|) d\omega + \int_0^\pi \log(|1 + a_2 e^{-j\omega} + a_3 e^{-j2\omega}|) d\omega - \int_0^\pi \log(|1 + b_1 e^{-j\omega}|) d\omega - \int_0^\pi \log(|1 + b_2 e^{-j\omega} + b_3 e^{-j2\omega}|) d\omega + \dots$$

The Sensitivity of a Feedback Loop

$$\int_0^\pi \log |NTF(e^{j\omega})| d\omega = \int_0^\pi \log \left| \frac{(1 + a_1 e^{-j\omega})(1 + a_2 e^{-j\omega} + a_3 e^{-2j\omega}) \dots}{(1 + b_1 e^{-j\omega})(1 + b_2 e^{-j\omega} + b_3 e^{-3j\omega}) \dots} \right| d\omega =$$

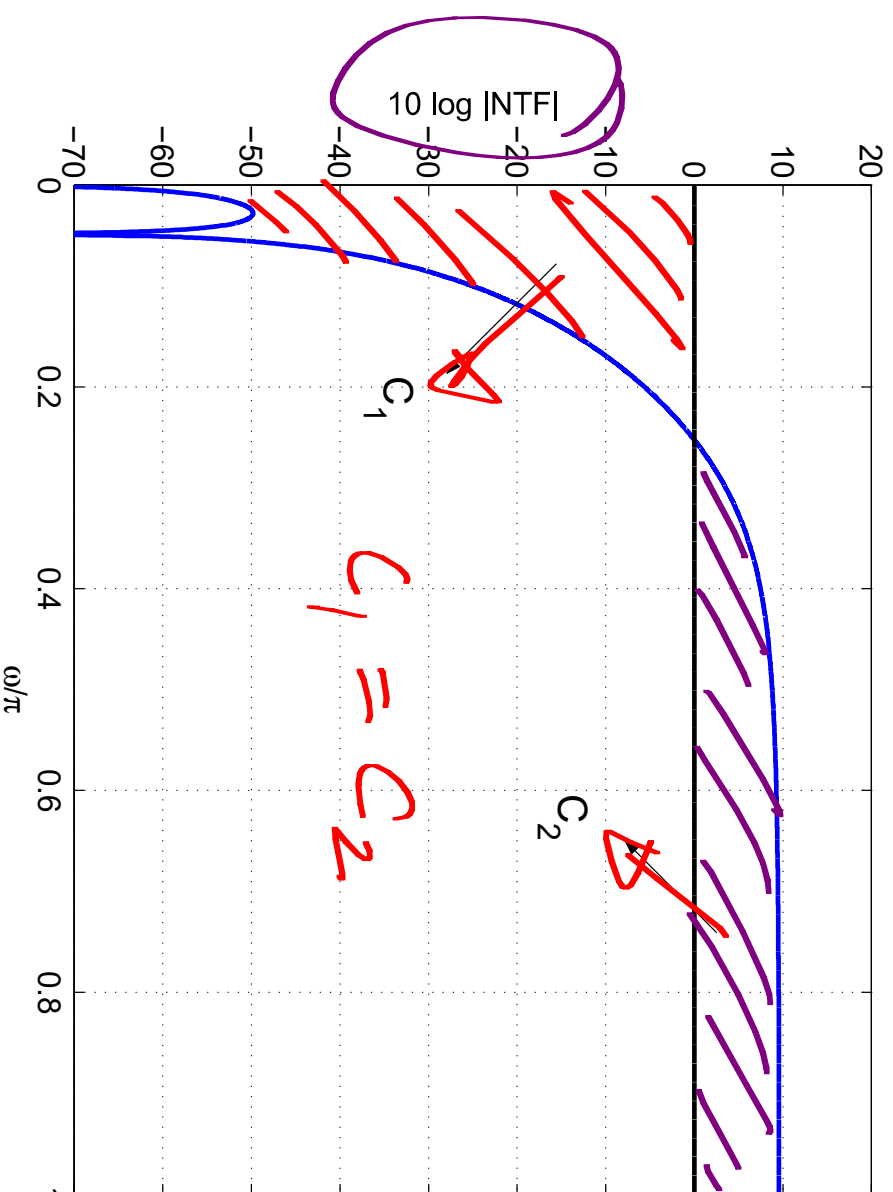
$$\int_0^\pi \log(|1 + a_1 e^{-j\omega}|) d\omega + \int_0^\pi \log(|1 + a_2 e^{-j\omega} + a_3 e^{-j2\omega}|) d\omega - \int_0^\pi \log(|1 + b_1 e^{-j\omega}|) d\omega - \int_0^\pi \log(|1 + b_2 e^{-j\omega} + b_3 e^{-j2\omega}|) d\omega + \dots$$

= Zero

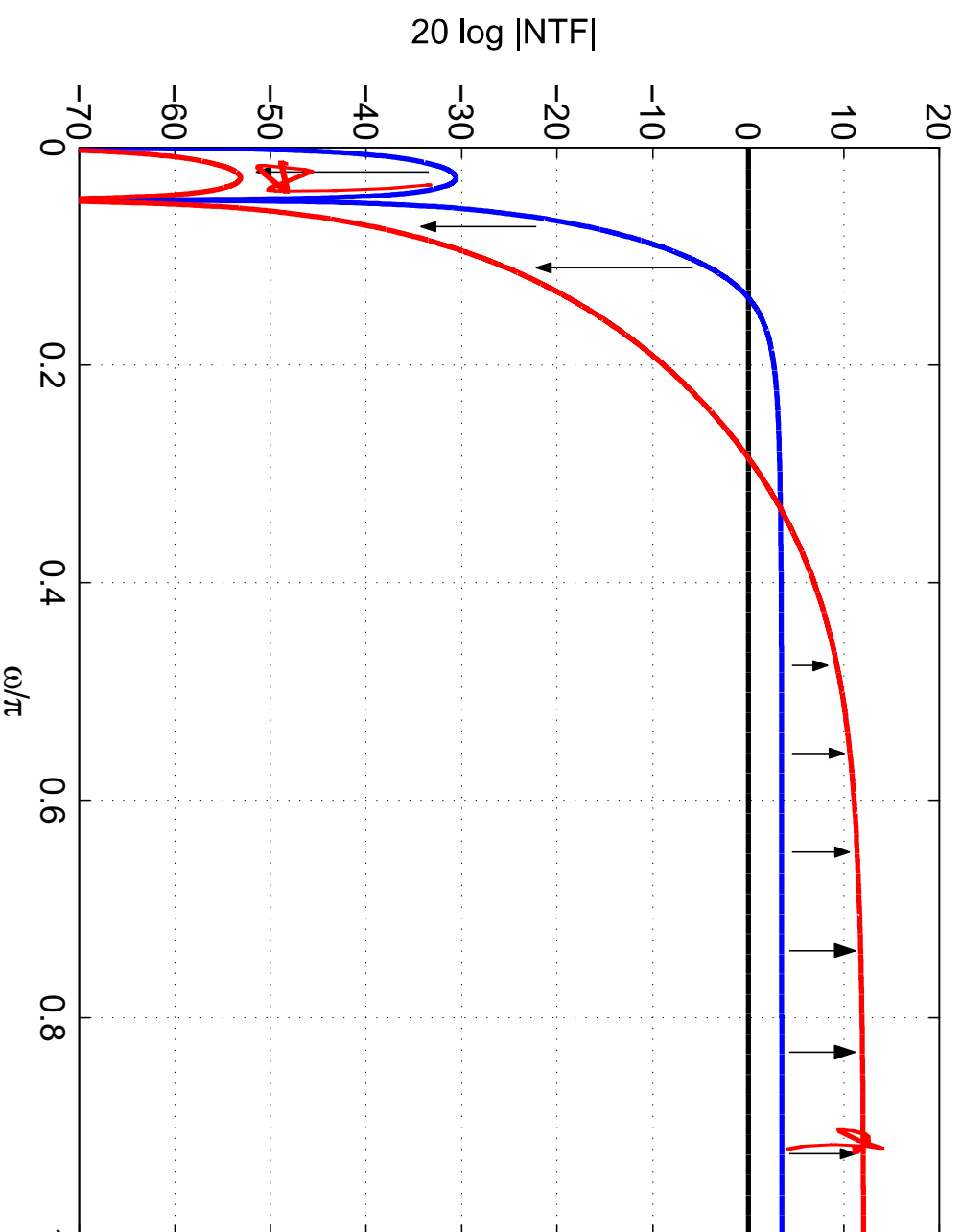
The Bode Sensitivity Integral

$$\int_0^{\pi} \log |NTF(e^{j\omega})| d\omega = 0$$

The Integral of the Log Magnitude of an NTF is 0

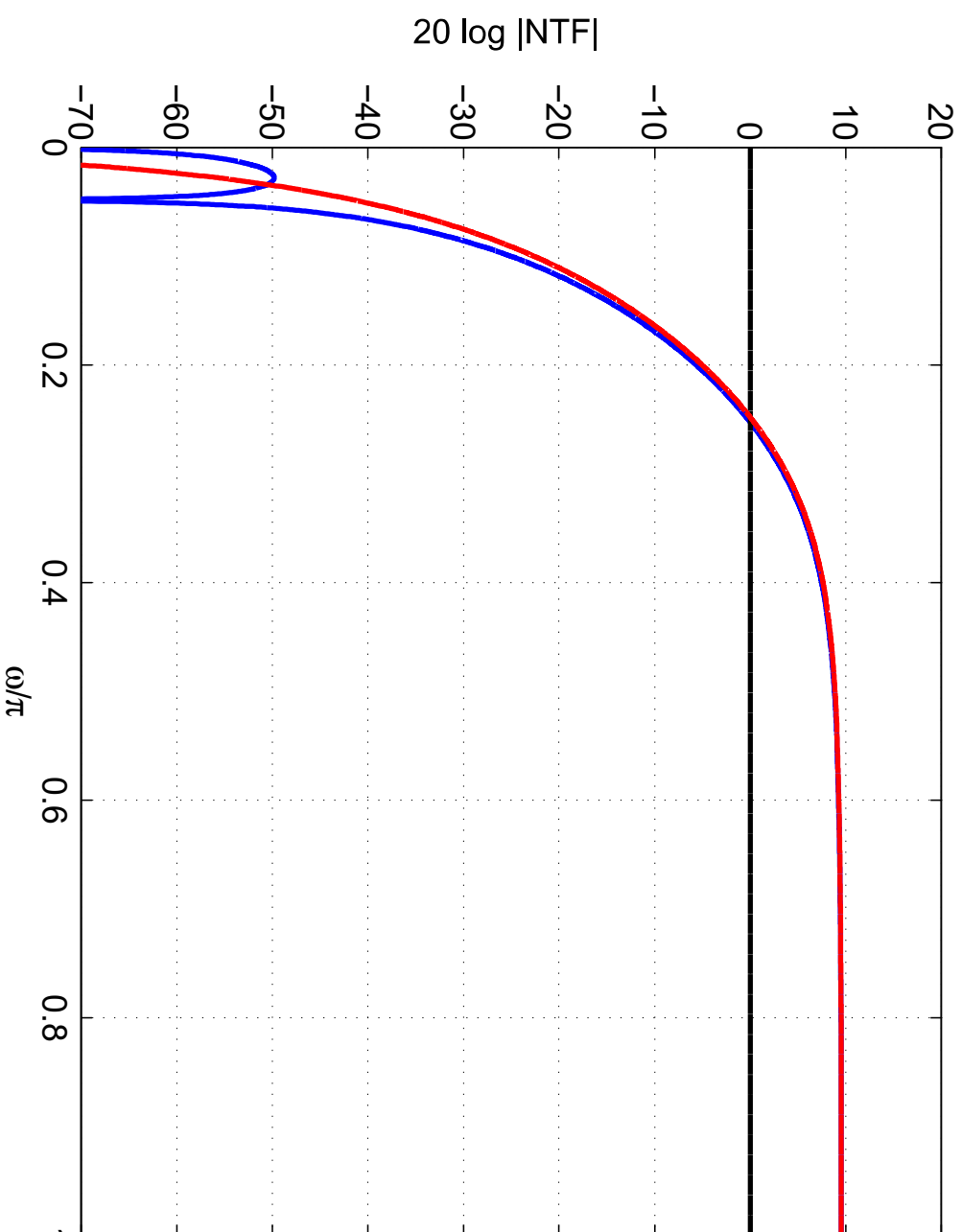


The Bode Sensitivity Integral



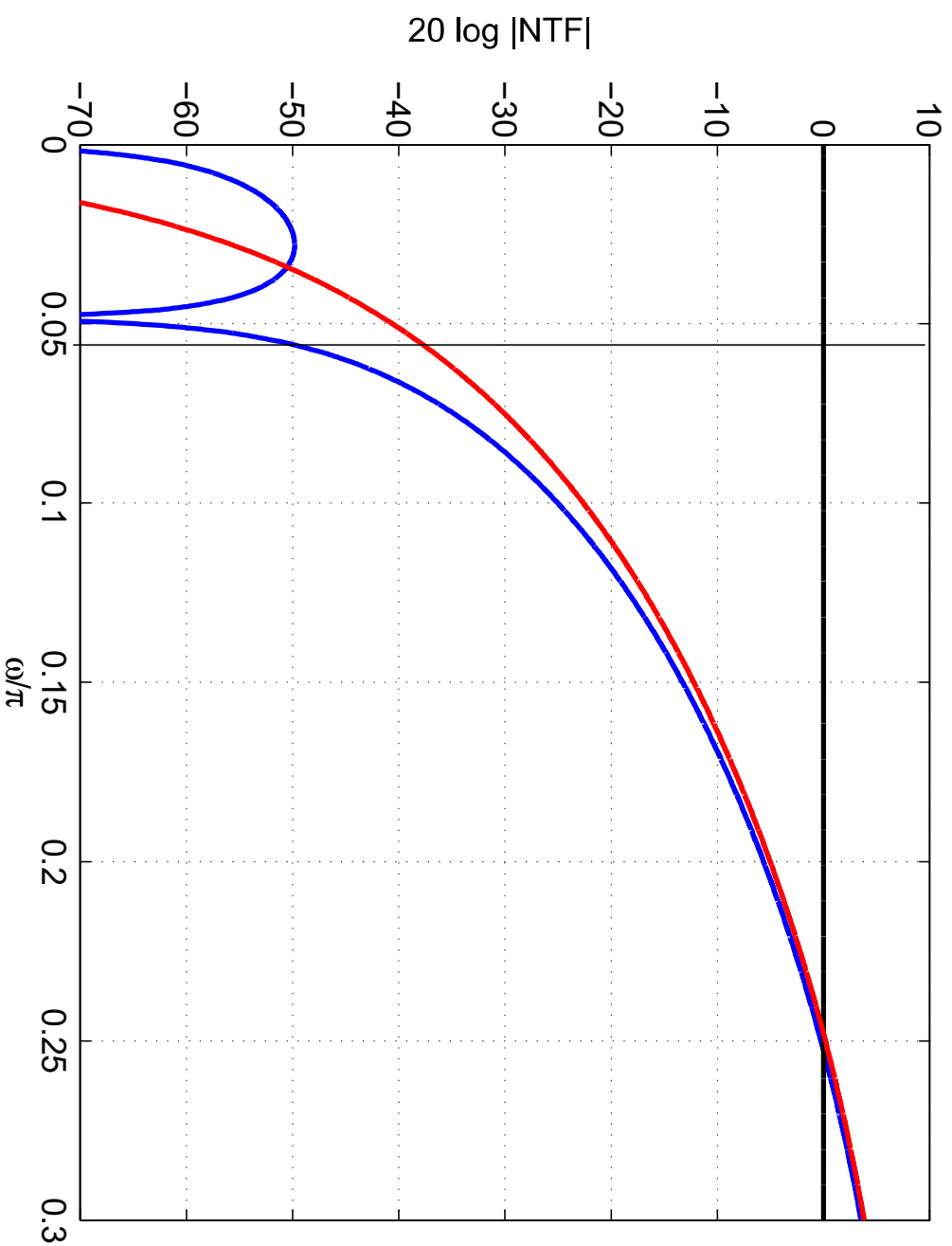
Good inband performance at the expense of poor out-of-band performance.

The Bode Sensitivity Integral



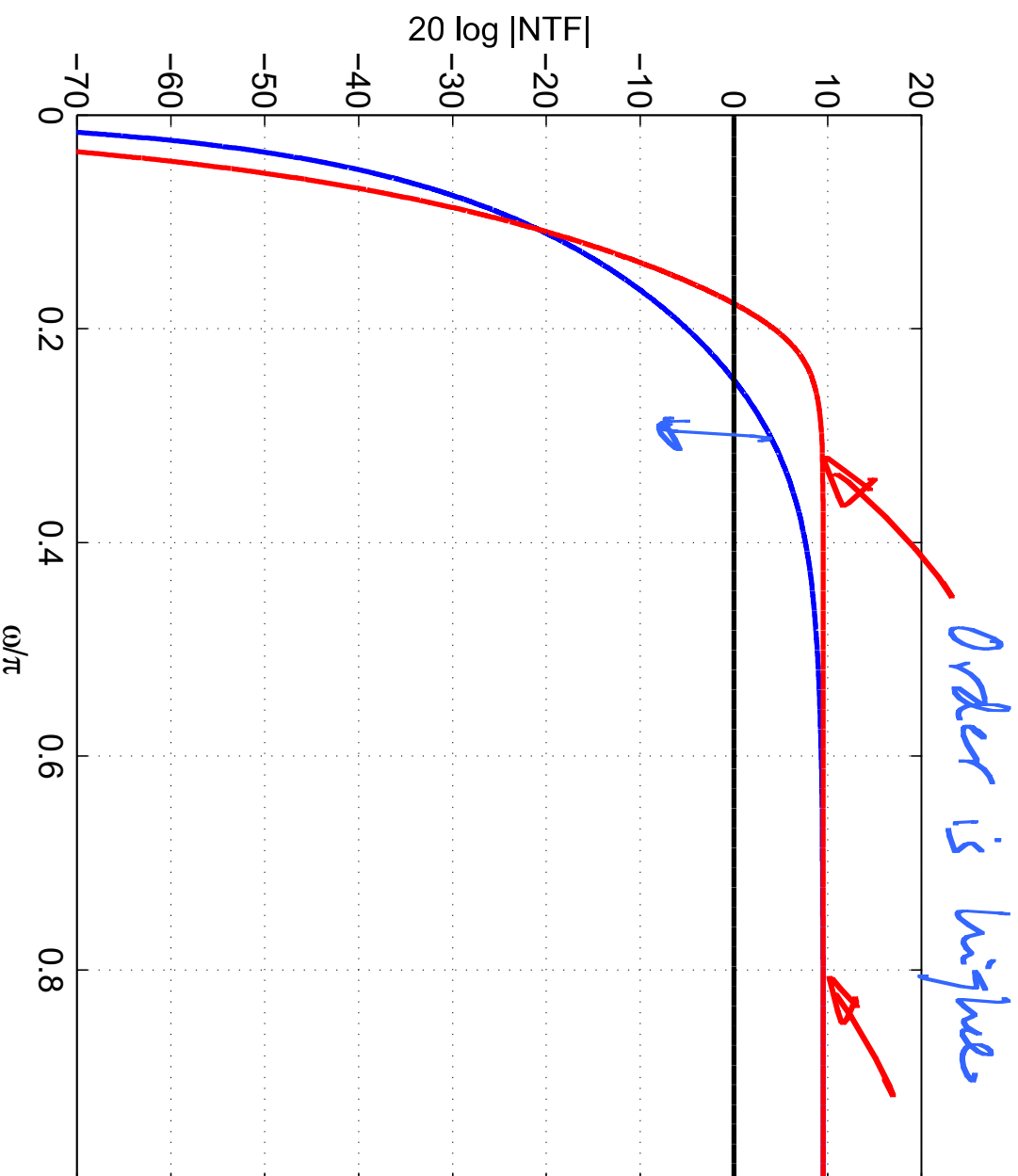
Complex zeros better than choosing all NTF zeros at the origin.

The Bode Sensitivity Integral



Complex zeros better than choosing all NTF zeros at the origin.

The Bode Sensitivity Integral



Higher order $\Rightarrow$ less in-band noise.

A Systematic NTF Design Procedure

$$\omega^2 \quad q\omega^3 \quad \omega^N \quad q\omega^N$$

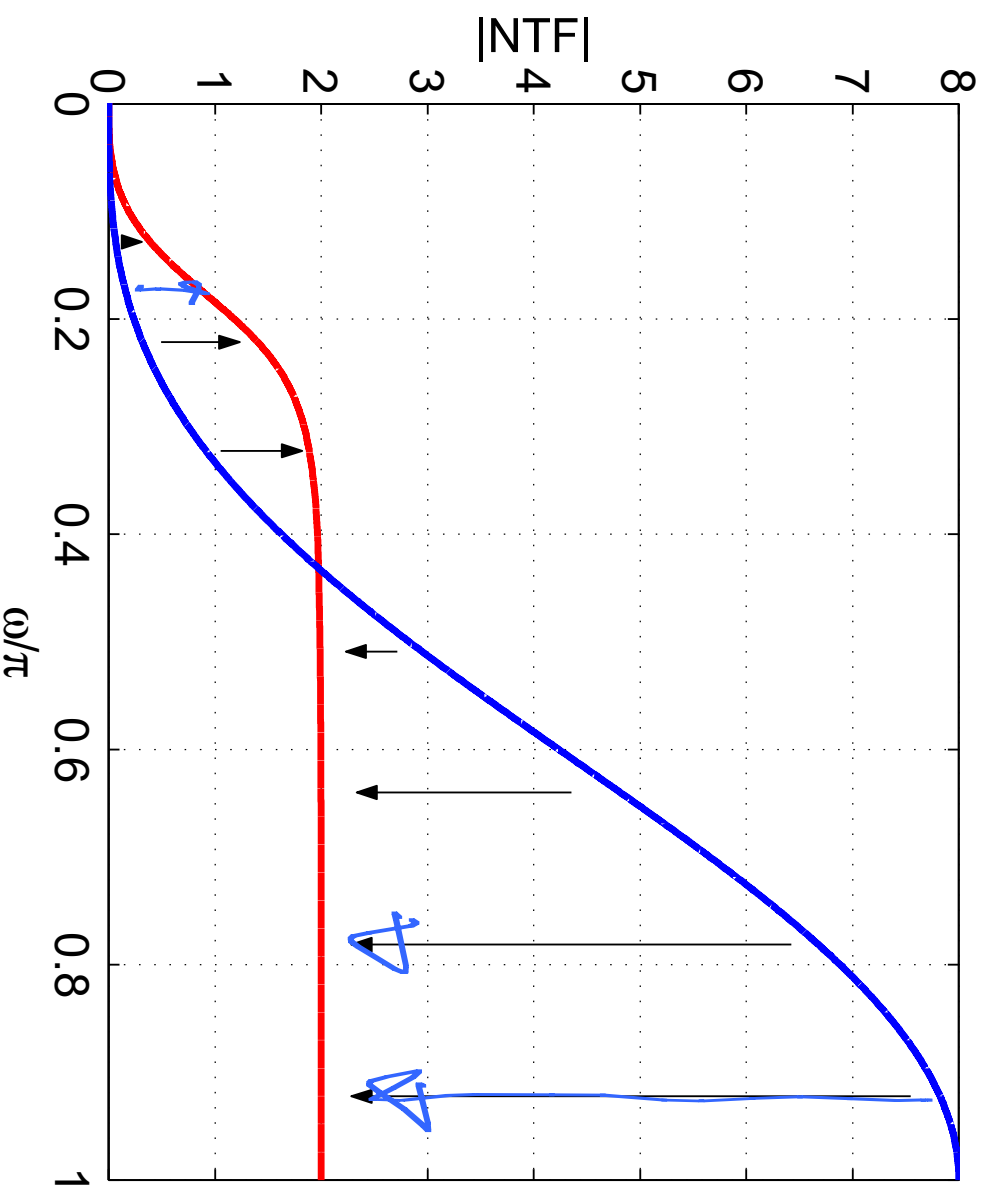
- NTFs of the form $(1 - z^{-1})^N$ have stability problems.
- Why ?
- The OBG is too high (2^N).
- This saturates the quantizer even for small inputs, causing instability.
- The MSA is small.
- Worse for low quantizer resolutions.

A Systematic NTF Design Procedure

Solution

- Introduce poles into the NTF.
- $NTF(z) = \frac{(1 - z^{-1})^N}{D(z^{-1})}$. 
- Recall that $NTF(\infty) = 1$.
- $\Rightarrow \underbrace{D(z = \infty)} = 1$.

Why do poles help ?

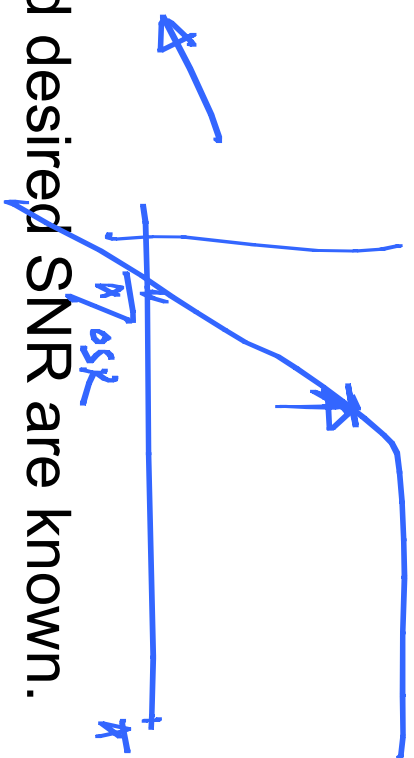


- Properly chosen poles reduce OBG of the NTF, enhancing stability.
- However, stability comes at the expense of increased in-band noise.

A Systematic NTF Design Procedure

- Commonly used pole positions : Butterworth, Chebyshev, Inv. Chebyshev etc.
- Coefficients for these approximations readily gotten from MATLAB.
- Schreier's Delta-Sigma Toolbox is an invaluable design aid.
- One should understand what the toolbox does.

A Systematic NTF Design Procedure



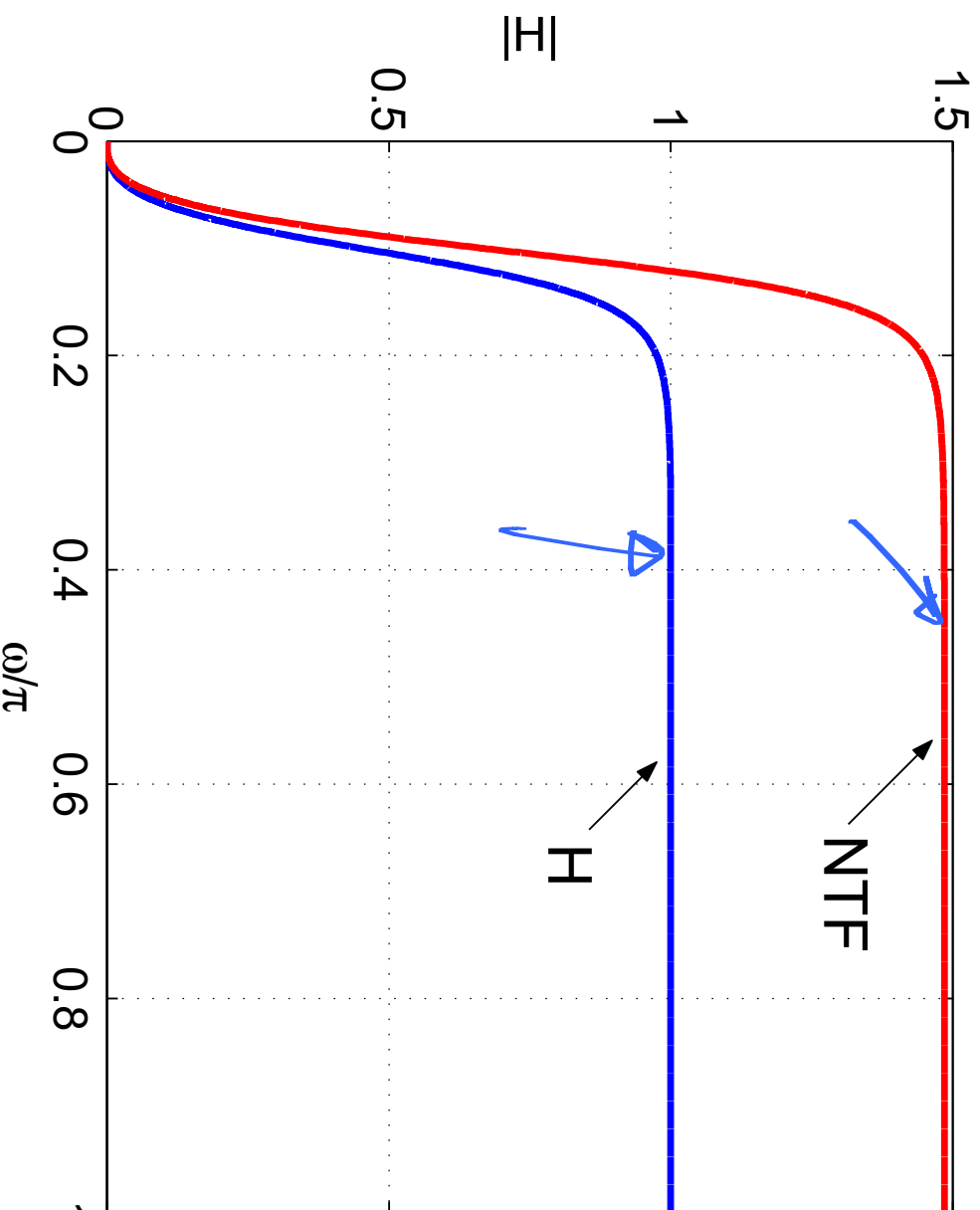
- Choose the order of the NTF.
- OSR, number of levels (n) and desired SNR are known.
- Example : Order = 3, OSR = 64, $n = 16$, SNR = 115 dB.
- Basically, the NTF is a high-pass filter transfer function.
- Example : Choose a Butterworth Highpass.
- Choose the 3 dB corner of the high pass filter -
 - Example : $\omega_{3dB} = \frac{\pi}{8}$.
 - For a Butterworth NTF, specifying the cutoff specifies the complete transfer function.

A Systematic NTF Design Procedure

- Get the transfer function from MATLAB
 - `[b, a] = butter(3, 1/8, 'high')`
 - $$H(z) = \frac{0.6735 - 2.0204z^{-1} + 2.0204z^{-2} - 0.6735z^{-3}}{1 - 2.2192z^{-1} + 1.7151z^{-2} - 0.4535z^{-3}}$$
 - MATLAB sets $|H(e^{j\pi})| = 1$.
- Recall that for $H(z)$ to be a valid NTF, $H(\infty) = 1$.

A Systematic NTF Design Procedure

- Scale $H(z)$ by $\frac{1}{0.6735}$ to obtain $NTF(z)$.
- $NTF(z) = \frac{(1 - 3z^{-1} + 3z^{-2} - z^{-3})}{1 - 2.2192z^{-1} + 1.7151z^{-2} - 0.4535z^{-3}}$ ← $(1 - z^{-1})^3$



A Systematic NTF Design Procedure

- Find loop filter using $\frac{1}{1+L(z)} = NTF(z)$.
- Simulate the equations describing the modulator.
- Compute the peak SNR.
 - In our example, we obtain SNR=102 dB after simulation.
 - MSA = 0.85.

A Systematic NTF Design Procedure

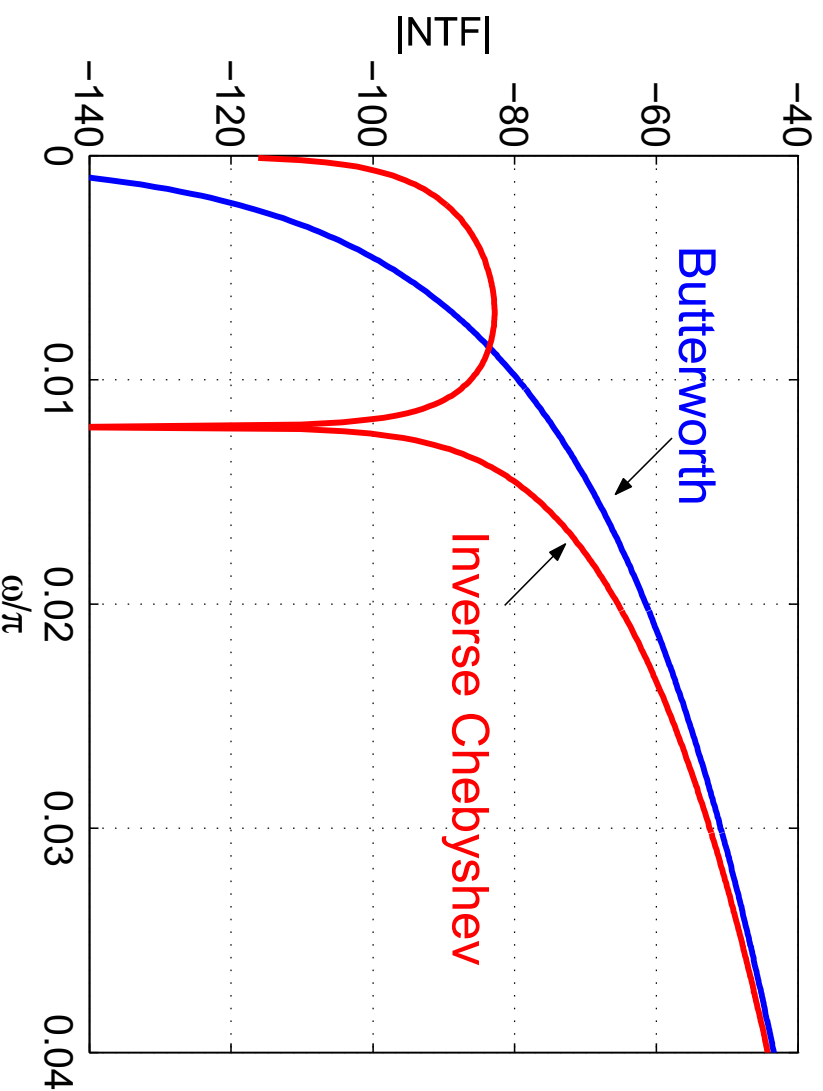
- If SNR is not enough, repeat the entire procedure above with a higher cutoff frequency for the Butterworth high pass filter.
 - This will increase the OBG (intuition on this later).
 - The MSA will reduce.
- If SNR is too high, repeat the entire procedure above with a lower cutoff frequency for the Butterworth high pass filter.
 - This will decrease the OBG (intuition on this later).
 - The MSA will increase.

A Systematic NTF Design Procedure

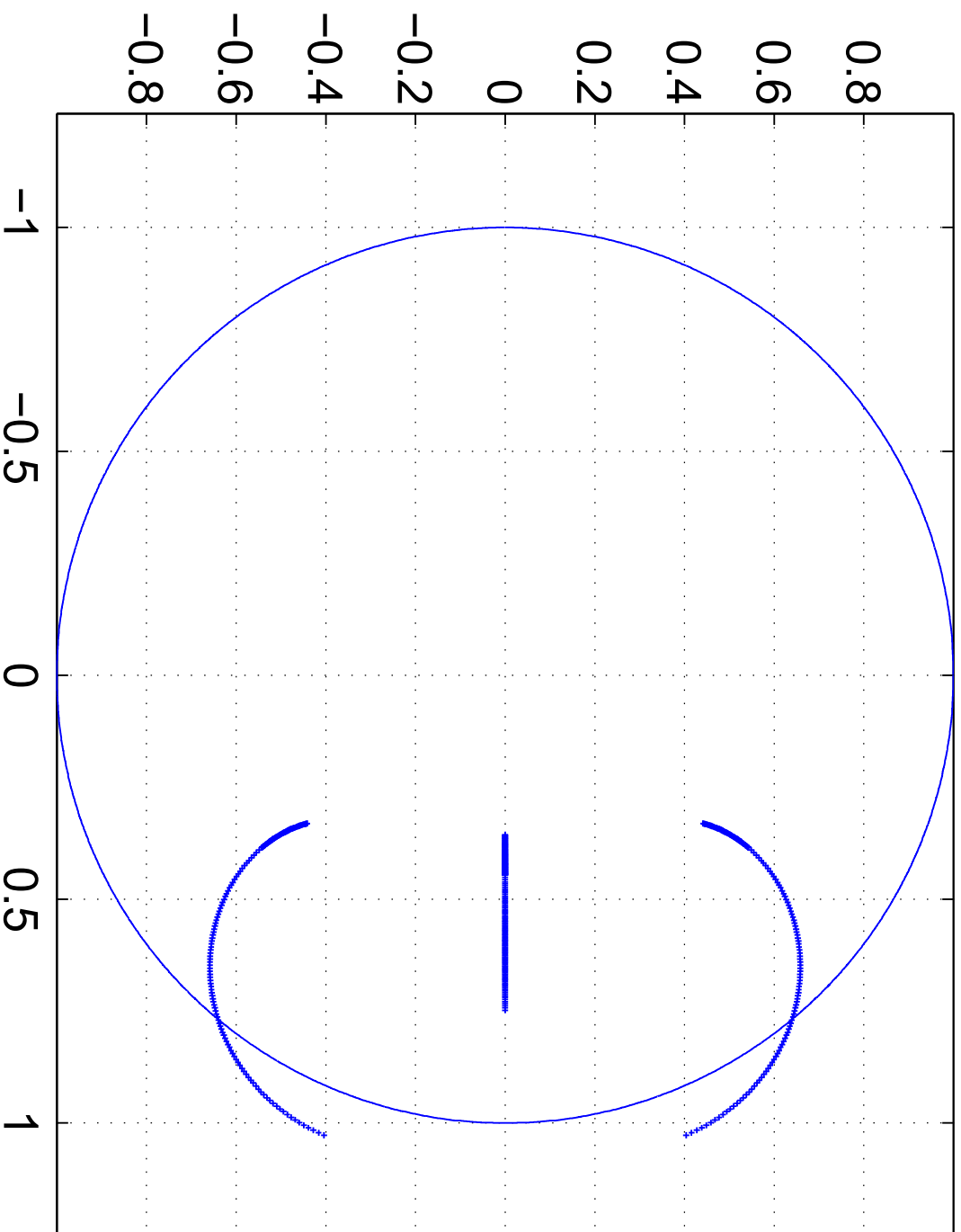
- SNR obtained with 3 dB cutoff of $\frac{\pi}{8}$ is inadequate.
- So, we increase the cutoff frequency to $\frac{\pi}{4}$.
- The peak SNR is around 116 dB.
- OBG = 2.25, MSA = 0.8.
- We are done.
- This iterative process is coded into `synthesizeNTF` in Schreier's toolbox.

A Systematic NTF Design Procedure : Remarks

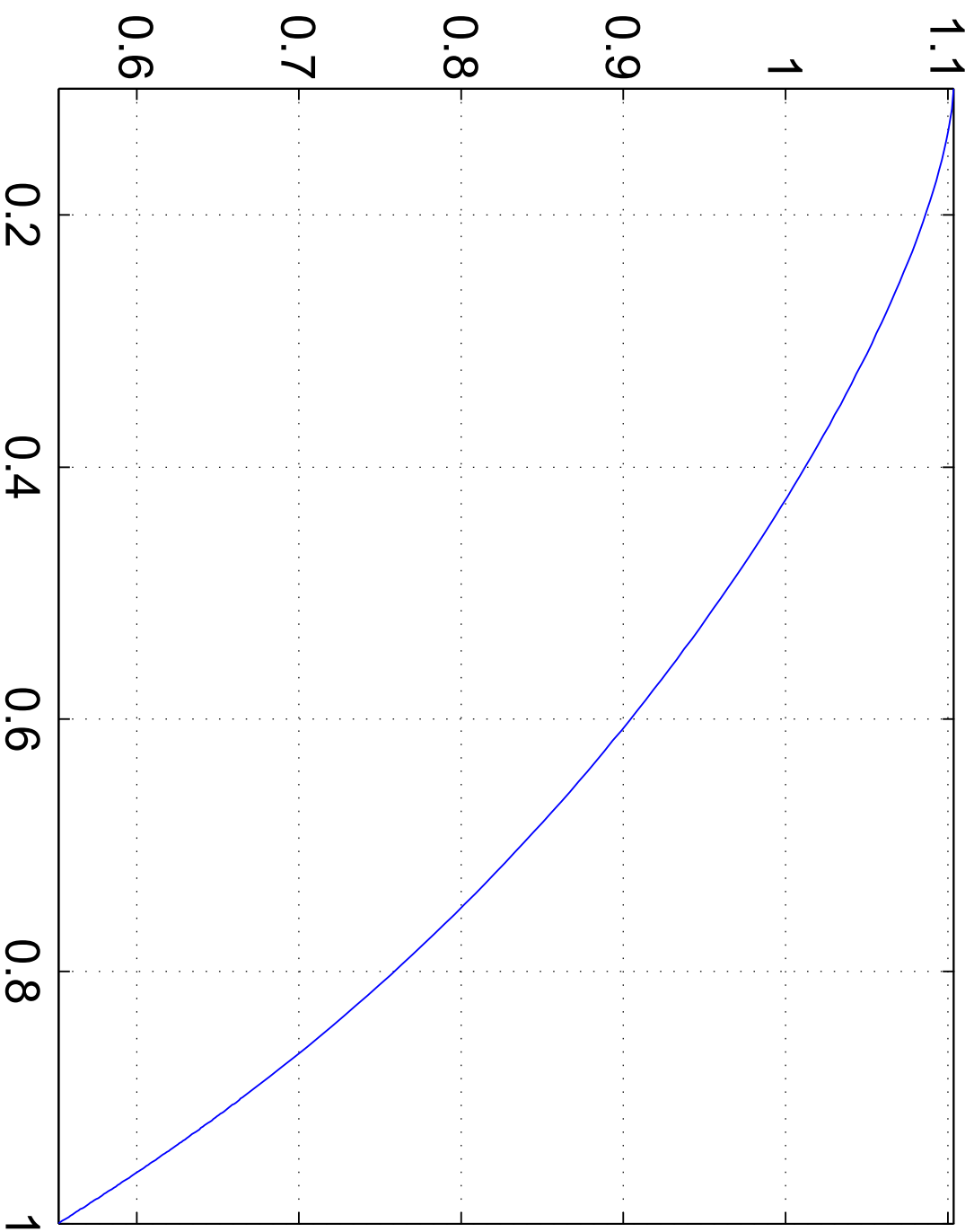
- Butterworth is one of several candidate high pass filters.
 - All the zeros of transmission are at the origin.
- Another useful family is the inverse Chebyshev approximation.
 - Has complex zeros (on the unit circle).



Root Locus of a Third Order $\Delta\Sigma$, OBG=3



Third Order DSM : $|p|$ versus Quantizer Gain, OBG=3



VLSI Data Conversion Circuits: Lecture 24

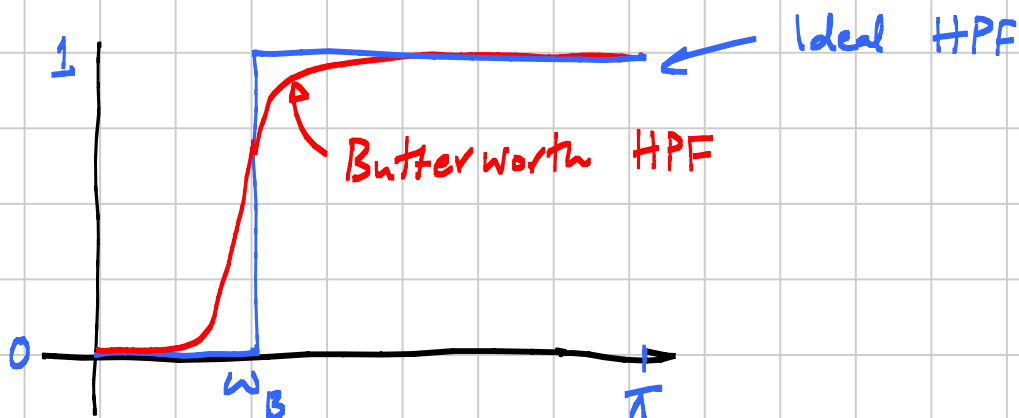
Note Title

09-02-2011

- * $NTF(z = \infty) = 1$
- * Area of the $\log |NTF|$ below zero
= Area of the $\log |NTF|$ above zero
- * Good performance in-band $\Rightarrow$
Poor performance outside the band
- * Order ✓
- * n (quantizer levels) ✓
- * f_s, f_b } OSR ✓
- * In band SQNR ✓

NTF Design $\Rightarrow$ High pass filter design

$\Rightarrow$ Butterworth, Chebyshev, Inv. Chebyshev, Elliptic



A Systematic NTF Design Procedure

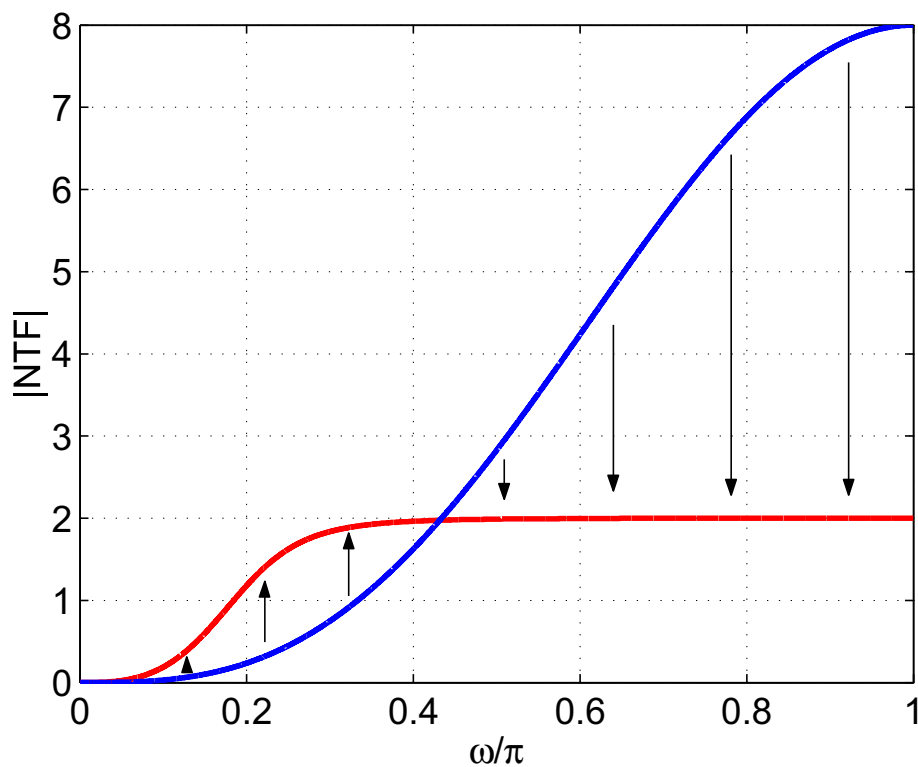
- NTFs of the form $(1 - z^{-1})^N$ have stability problems.
- Why ?
- The OBG is too high (2^N).
- This saturates the quantizer even for small inputs, causing instability.
- The MSA is small.
- Worse for low quantizer resolutions.

A Systematic NTF Design Procedure

Solution

- Introduce poles into the NTF.
- $NTF(z) = \frac{(1 - z^{-1})^N}{D(z^{-1})}$.
- Recall that $NTF(\infty) = 1$.
- $\Rightarrow D(z = \infty) = 1$.

Why do poles help ?

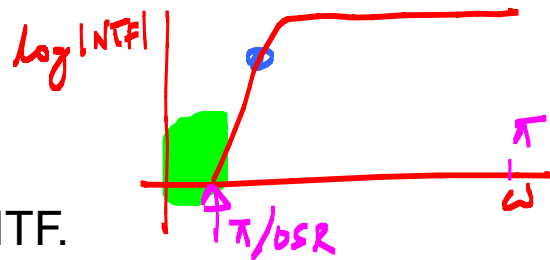


- Properly chosen poles reduce OBG of the NTF, enhancing stability.
- However, stability comes at the expense of increased in-band noise.

A Systematic NTF Design Procedure

- Commonly used pole positions : Butterworth, Chebyshev, Inv. Chebyshev etc. ✓
- Coefficients for these approximations readily gotten from MATLAB. ✓
- Schreier's Delta-Sigma Toolbox is an invaluable design aid.
- One should understand what the toolbox does.

A Systematic NTF Design Procedure



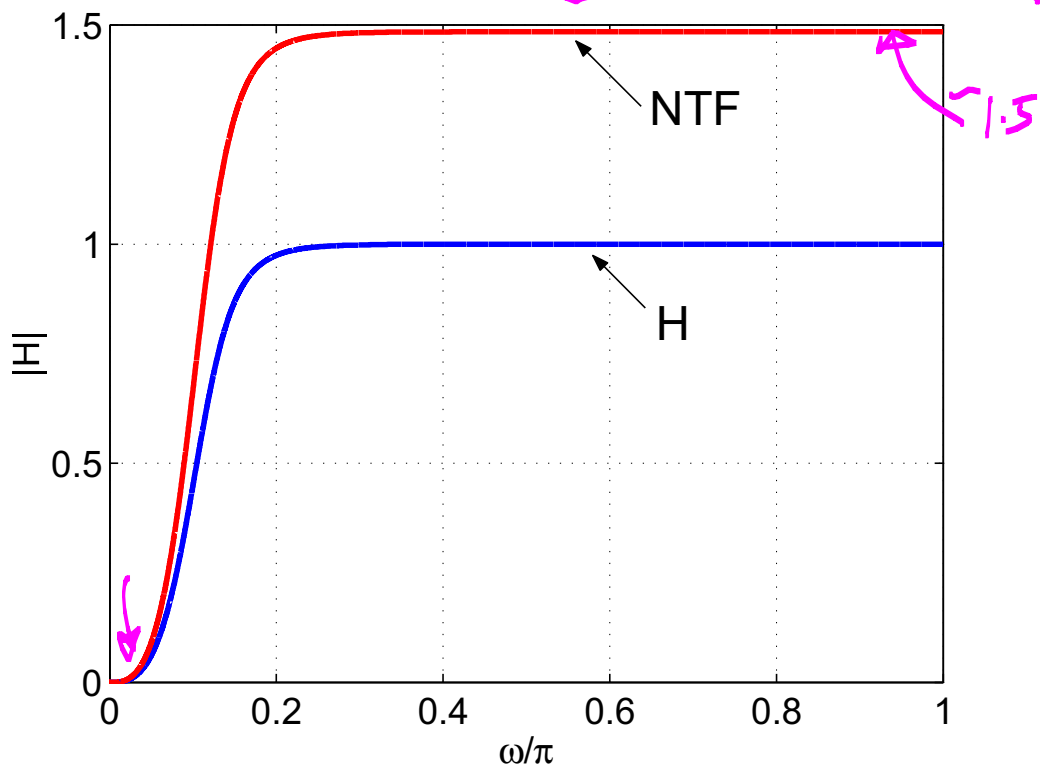
- Choose the order of the NTF.
- OSR, number of levels (n) and desired SNR are known.
 - Example : Order = 3, OSR = 64, $n = 16$, SNR = 115 dB.
- Basically, the NTF is a high-pass filter transfer function.
 - Example : Choose a Butterworth Highpass.
- Choose the 3 dB corner of the high pass filter -
 - Example : $\omega_{3dB} = \frac{\pi}{8}$.
 - For a Butterworth NTF, specifying the cutoff specifies the complete transfer function.

A Systematic NTF Design Procedure

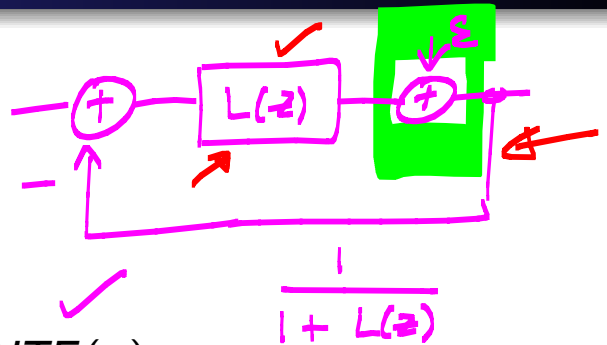
- Get the transfer function from MATLAB
 - `[b,a]=butter(3,1/8,'high')`
 - $H(z) = \frac{0.6735 - 2.0204z^{-1} + 2.0204z^{-2} - 0.6735z^{-3}}{1 - 2.2192z^{-1} + 1.7151z^{-2} - 0.4535z^{-3}}$
 - MATLAB sets $|H(e^{j\pi})| = 1$.
- Recall that for $H(z)$ to be a valid NTF, $H(\infty) = 1$.

A Systematic NTF Design Procedure

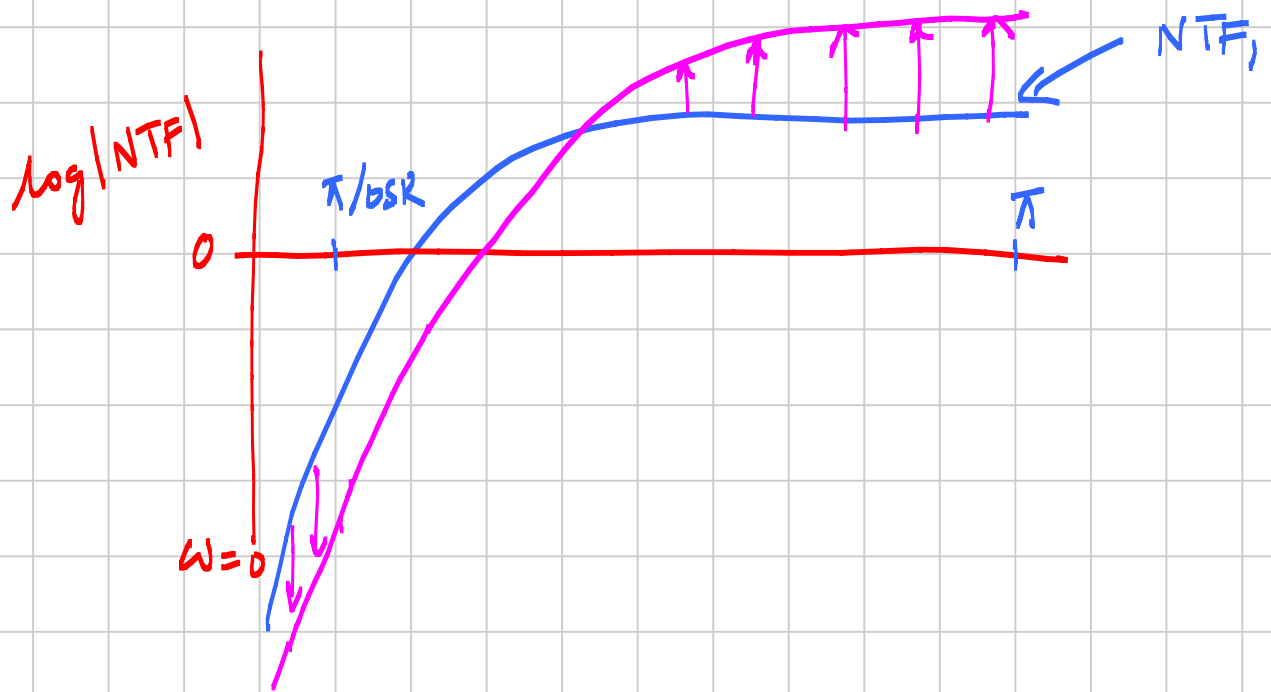
- Scale $H(z)$ by $\frac{1}{0.6735}$ to obtain $NTF(z)$.
- $NTF(z) = \frac{(1 - 3z^{-1} + 3z^{-2} - z^{-3})}{1 - 2.2192z^{-1} + 1.7151z^{-2} - 0.4535z^{-3}}$



A Systematic NTF Design Procedure



- Find loop filter using $\frac{1}{1+L(z)} = NTF(z)$.
- Simulate the equations describing the modulator.
- Compute the peak SNR.
 - In our example, we obtain SNR=102 dB after simulation.
 - MSA = 0.85.



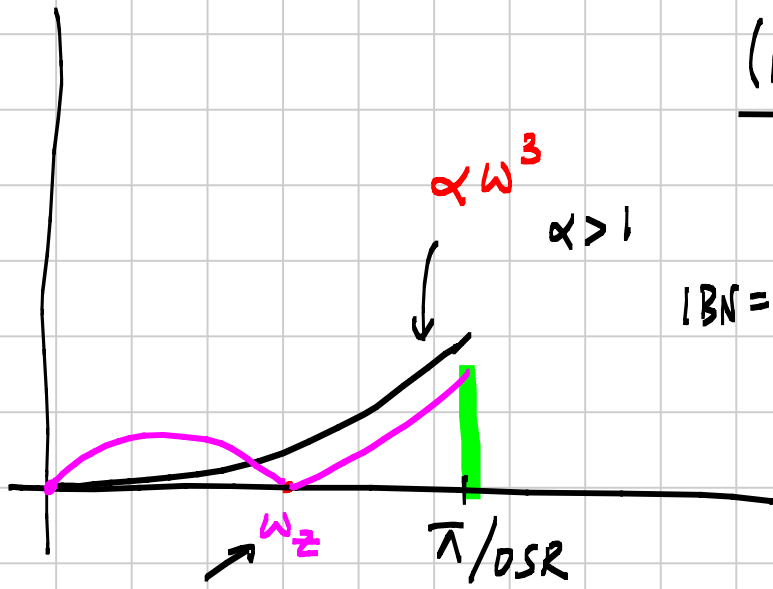
A Systematic NTF Design Procedure

- If SNR is not enough, repeat the entire procedure above with a higher cutoff frequency for the Butterworth high pass filter.
 - This will increase the OBG (intuition on this later).
 - The MSA will reduce.
- If SNR is too high, repeat the entire procedure above with a lower cutoff frequency for the Butterworth high pass filter.
 - This will decrease the OBG (intuition on this later).
 - The MSA will increase.

A Systematic NTF Design Procedure

- SNR obtained with 3 dB cutoff of $\frac{\pi}{8}$ is inadequate.
- So, we increase the cutoff frequency to $\frac{\pi}{4}$.
- The peak SNR is around 116 dB.
- OBG = 2.25, MSA = 0.8.
- We are done.
- This iterative process is coded into synthesizeNTF in Schreier's toolbox.

$|NTF|$

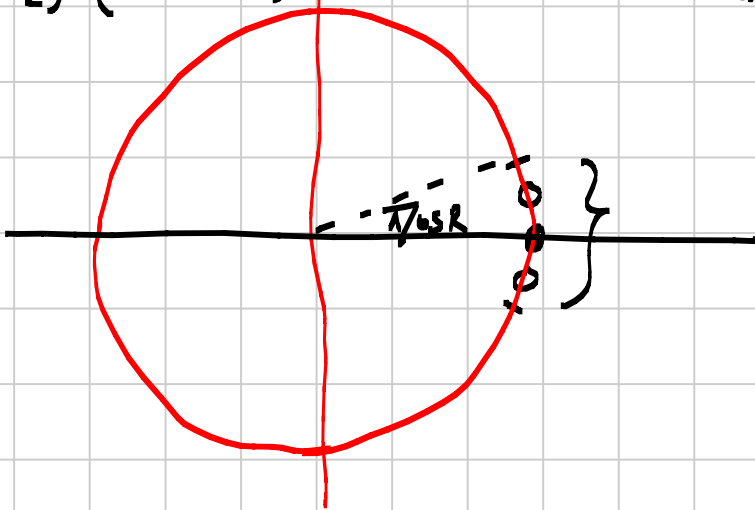


$$\frac{(1-z^{-1})^N}{D(z^{-1})}$$

$$|BN| = \frac{\Delta^2}{12\pi} \int_0^{\pi/OSR} \alpha^2 \omega^{2N} d\omega$$

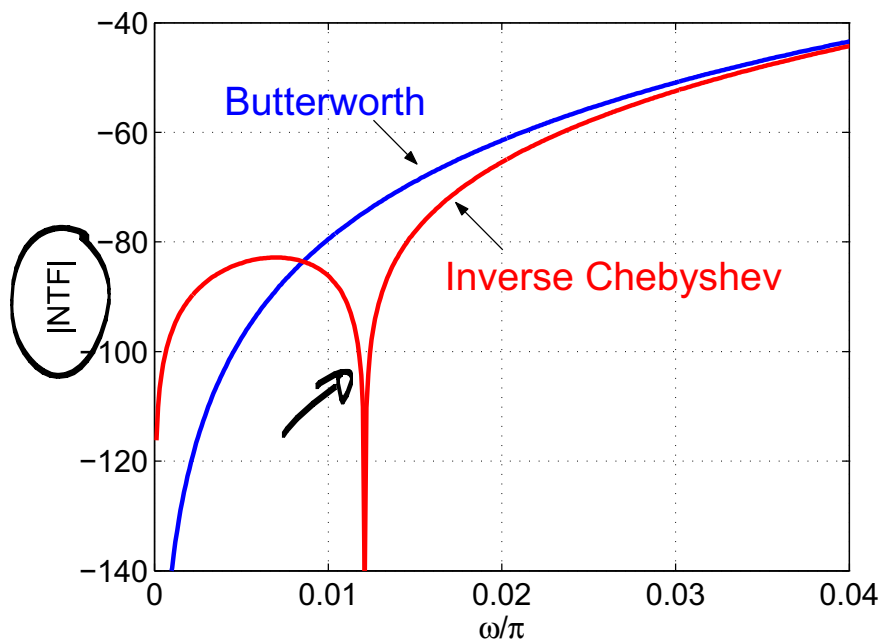
$$\frac{\Delta^2}{12\pi} \int_0^{\pi/OSR} \omega^2 (\omega^2 - \omega_z^2)^2 d\omega$$

$$\omega^2 (\omega - \omega_z)^2 (\omega + \omega_z)^2$$

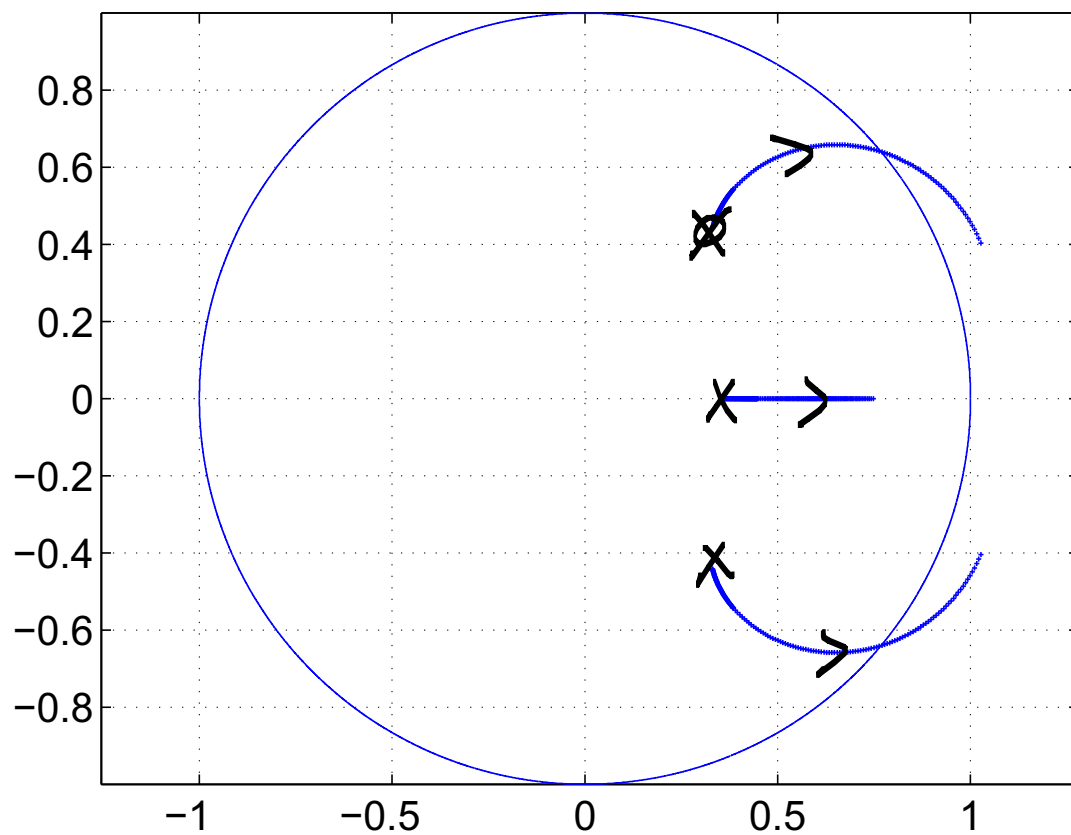


A Systematic NTF Design Procedure : Remarks

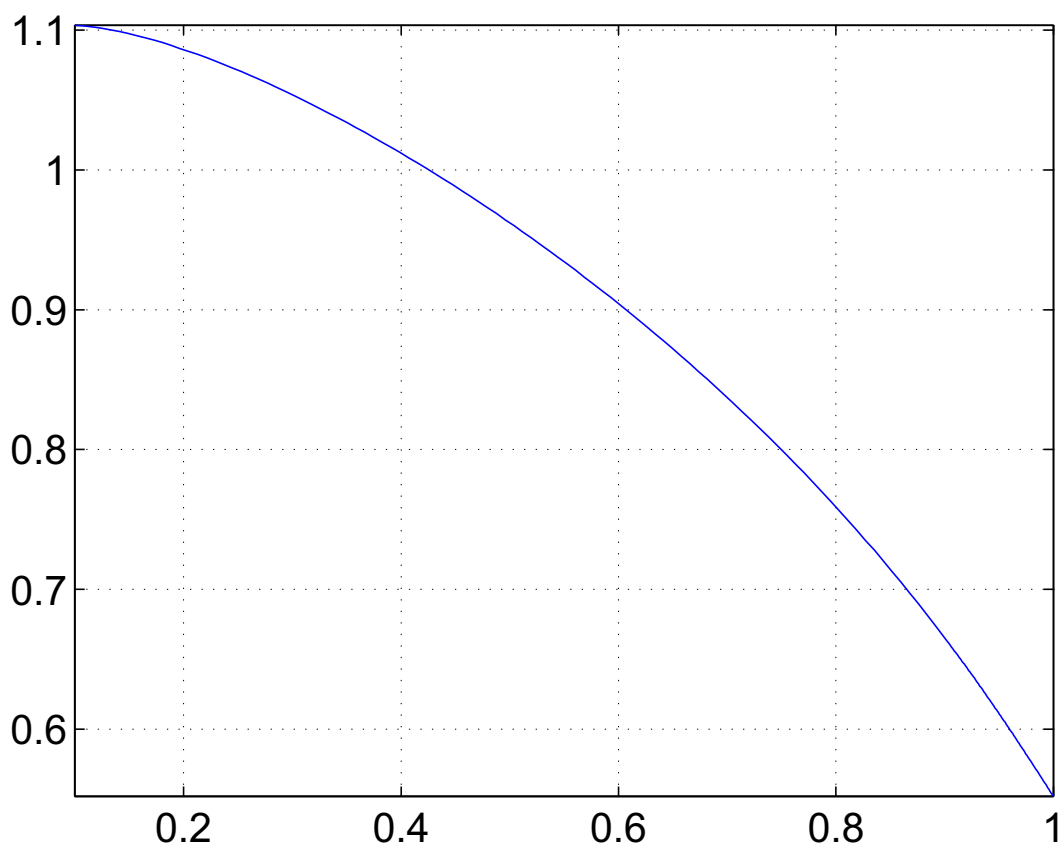
- Butterworth is one of several candidate high pass filters.
 - All the zeros of transmission are at the origin.
- Another useful family is the inverse Chebyshev approximation.
 - Has complex zeros (on the unit circle).



Root Locus of a Third Order $\Delta\Sigma$, OBG=3



Third Order DSM : $|p|$ versus Quantizer Gain, OBG=3



VLSI Data Conversion Circuits: Lecture 25

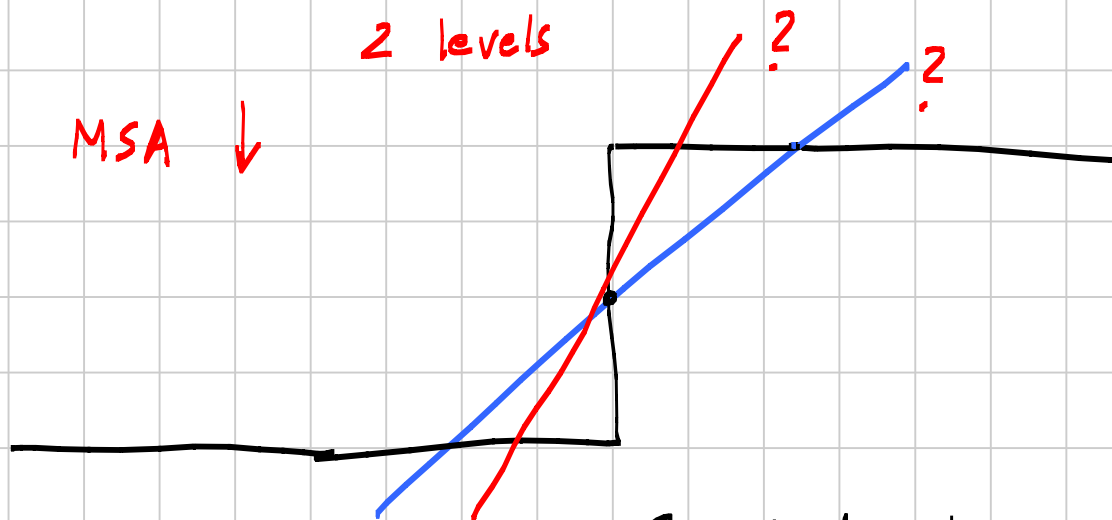
* Systematic Design an NTF

→ Order, Out of Band Gain (OBG), (Iterate)

→ OSR, n (Fixed)

can be made as low as 2 levels

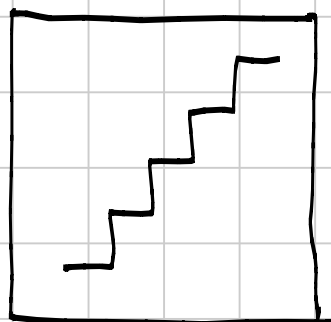
$n \downarrow$ MSA $\downarrow$



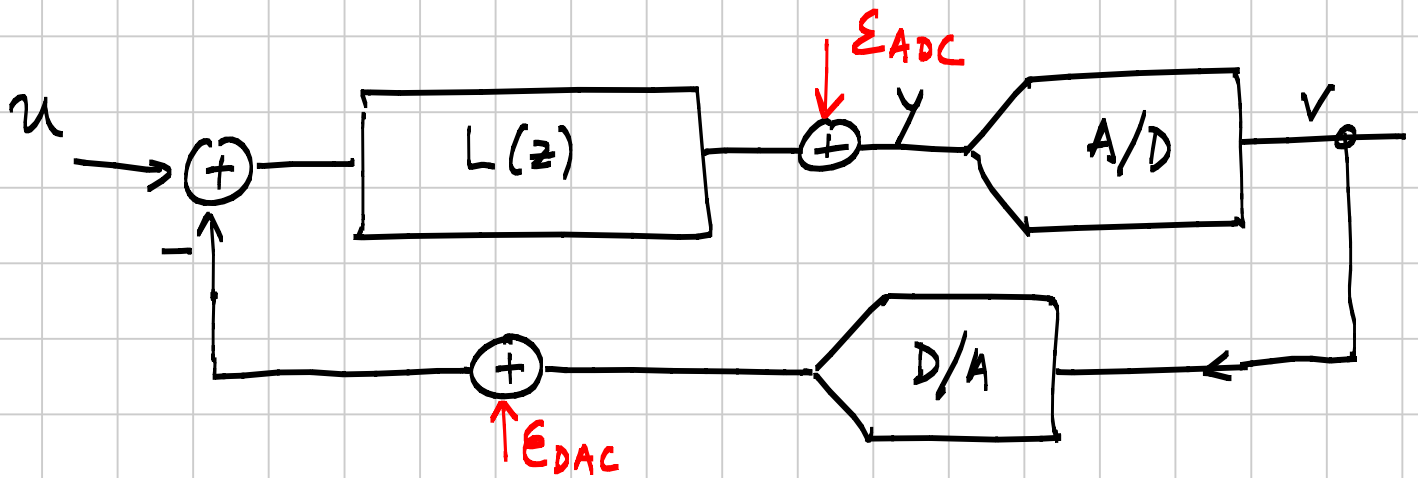
* NTF's OBG ≤ 1.5 } Empirical rule
Lee's Rule

→ Multibit $\Delta\Sigma$ Modulators

→ Single bit $\Delta\Sigma$ Modulators

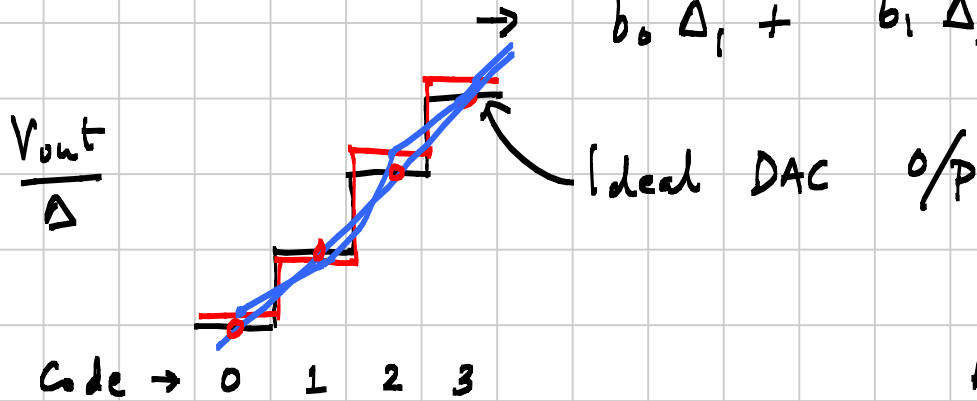


→ Offset
→ Gain Error
→ DNL, INL

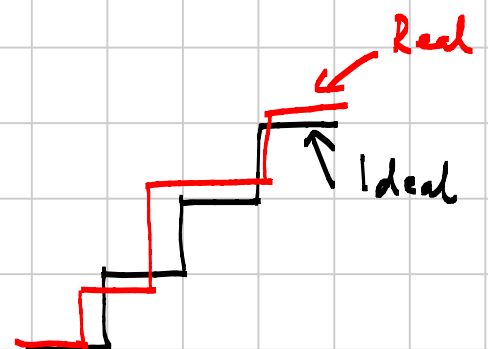
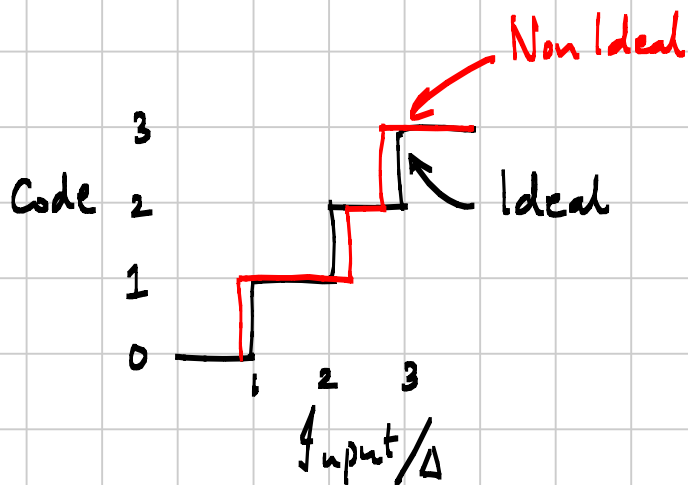


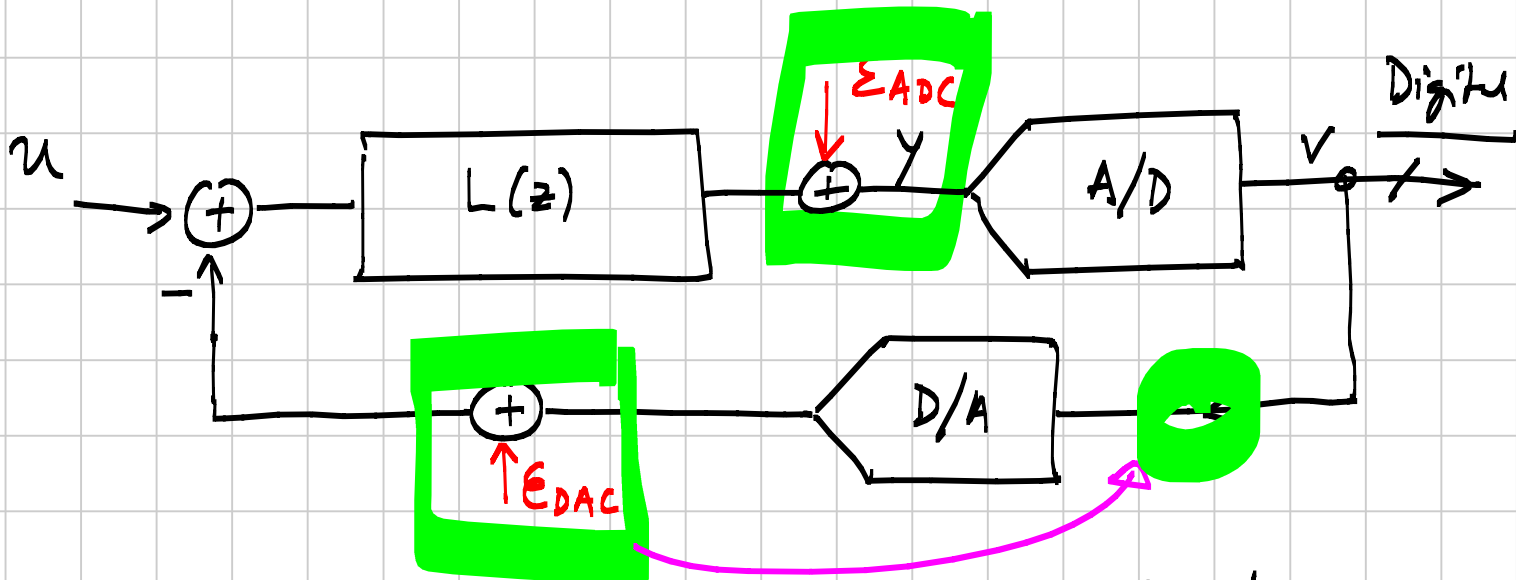
D/A Converter $\rightarrow b_1, b_0$

$$\rightarrow b_0 \Delta_1 + b_1 \Delta_2$$



ADC-DAC Cascade

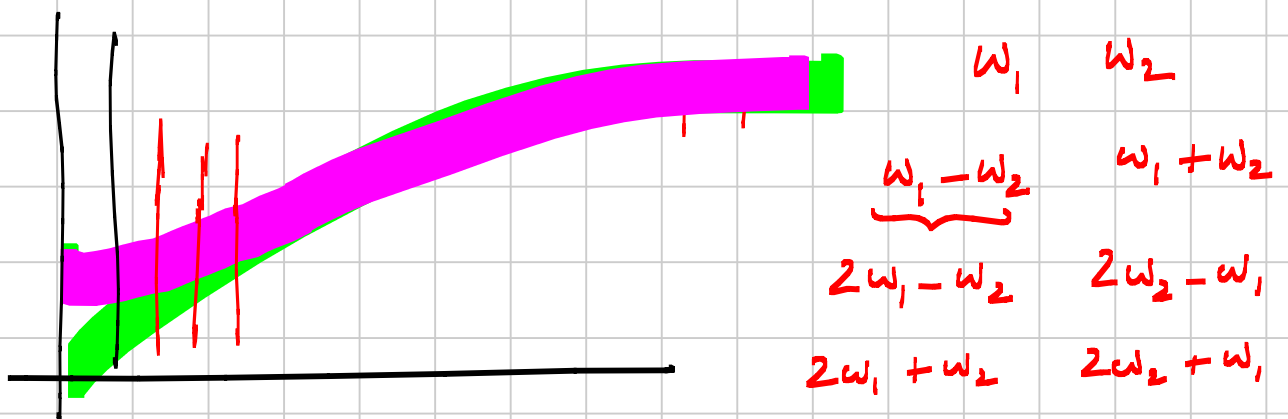




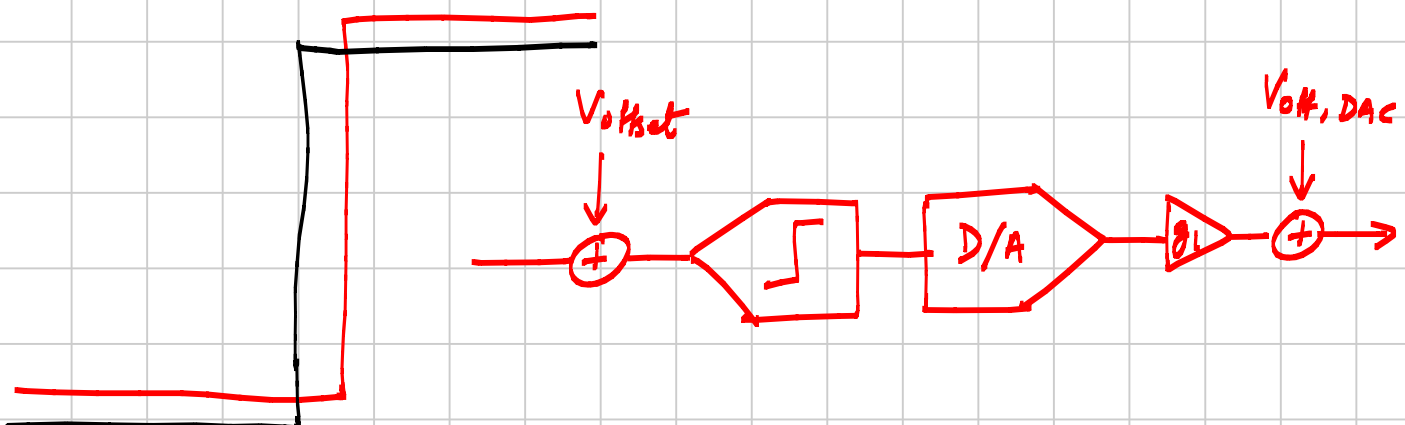
ϵ_{ADC} is benign as it gets noise shaped.

ϵ_{DAC} causes problems as the TF from

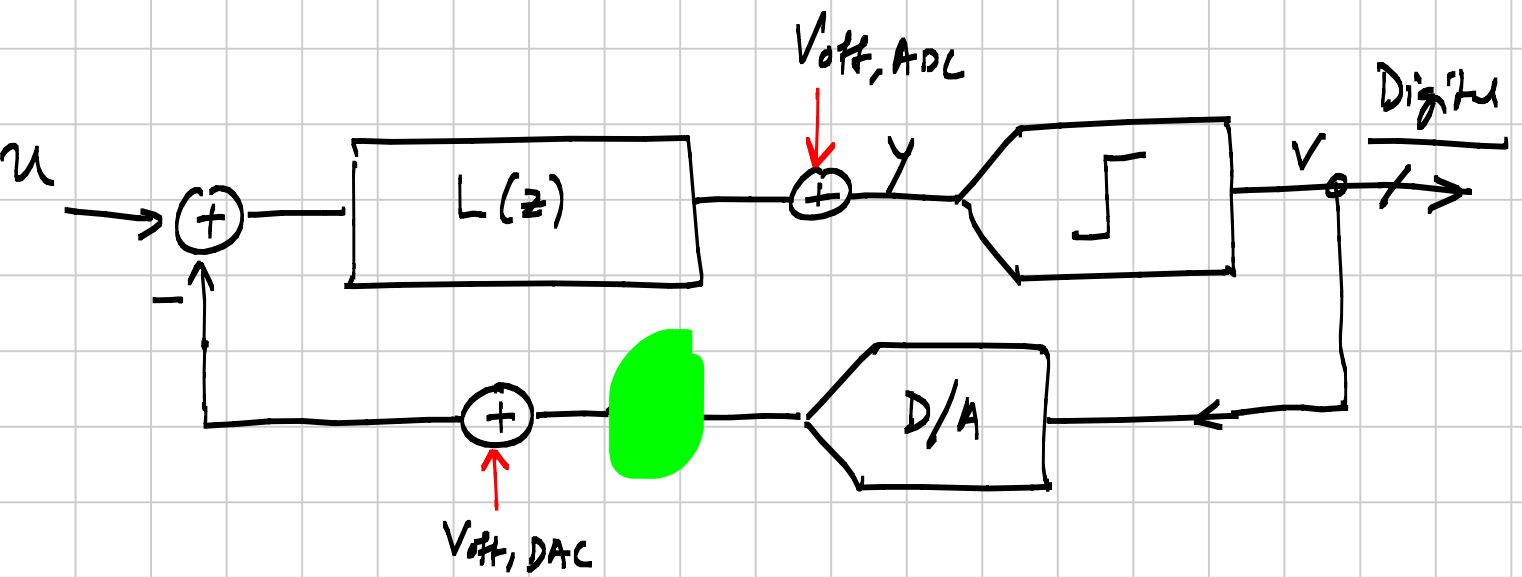
ϵ_{DAC} to V is the same as the STF ($=1$)



* Linearity of the feedback DAC is very very important



Nonideal Single bit $\Delta\Sigma M$



* Single bit $\rightarrow$ D/A & A/D errors do not matter

VLSI Data Conversion Circuits: Lecture 26

Note Title

14-02-2011

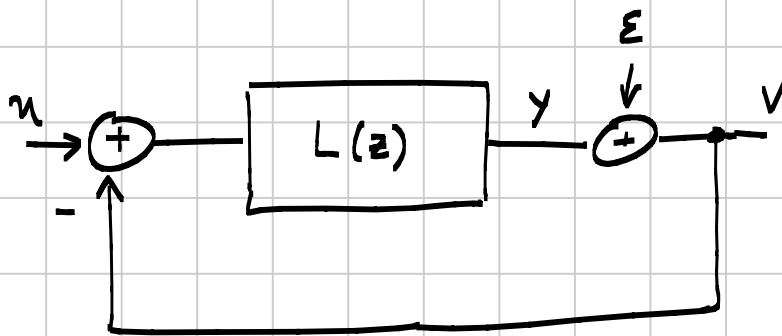
* Noise Shaping

* NTF $\frac{(1 - z^{-1})^N}{D(z^{-1})}$

* $\int_0^\pi \log |NTF| d\omega = 0$

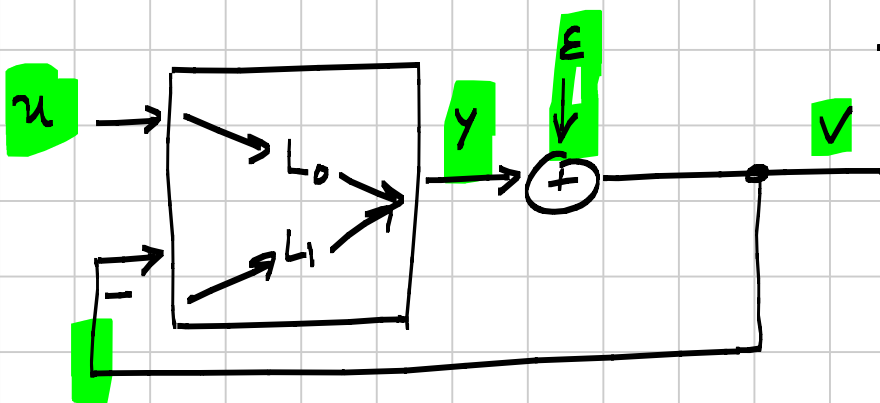
$NTF(z = \infty) = 1 \equiv h[0] = 1 \equiv 1(0) = 0$

$\rightarrow \frac{1}{1 + L(z)} = NTF(z)$



STF: $\frac{L(z)}{1 + L(z)}$

NTF: $\frac{1}{1 + L(z)}$



→ Single loop structure

Single bit Multibit

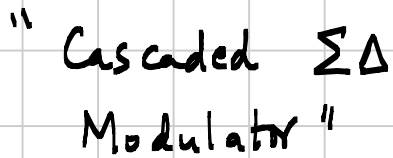
$y = L_0 u - L_1 v$
 $L_0 u - L_1 v + \epsilon = v$

$v = \frac{L_0(z) u}{1 + L_1(z)} + \frac{\epsilon}{1 + L_1(z)}$

STF = $\frac{\text{[redacted]}}{1 + \text{[redacted]}}$

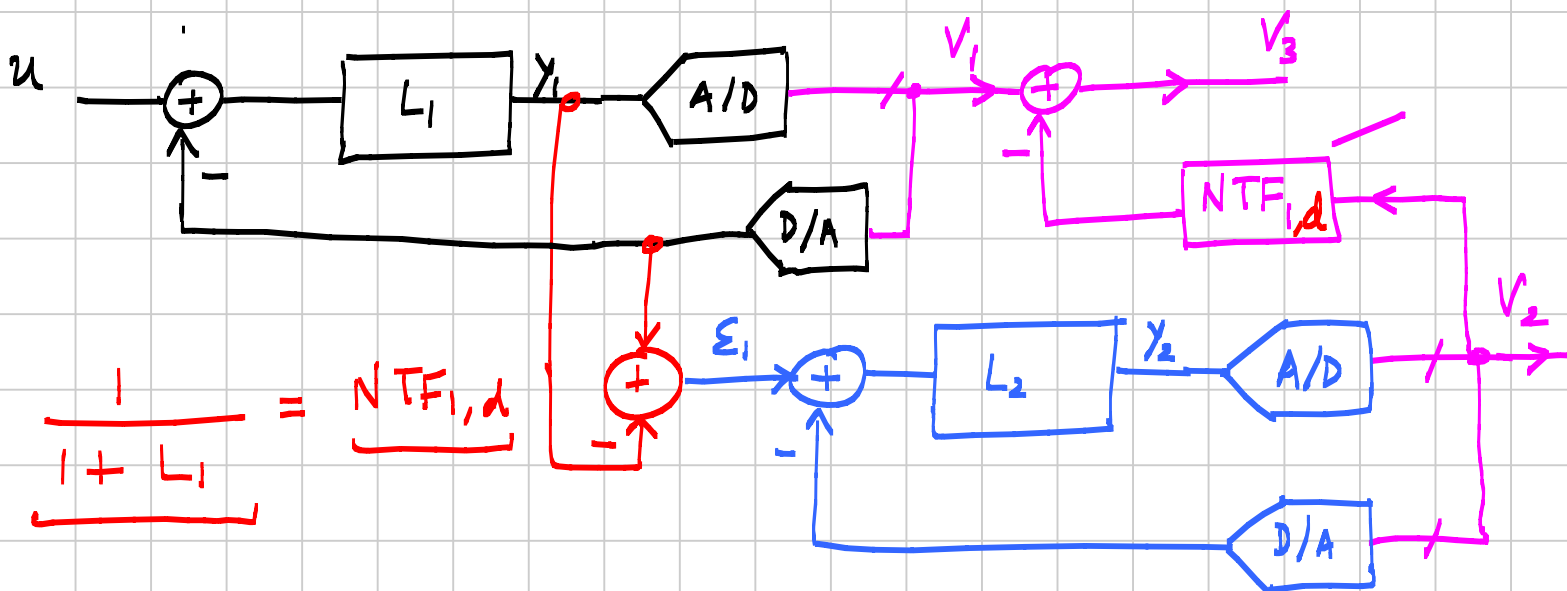
NTF: $\frac{1}{1 + \text{[redacted]}}$

$$\approx u + NTF, \varepsilon_1$$


$$[V_2 \approx \varepsilon_1 + NTF_2 \varepsilon_2] NTF_1$$

$$V_3 = V_1 - NTF_1 V_2 \quad (1 - z^{-1})^4$$

$$= u - \underbrace{NTF_1 \cdot NTF_2}_{=1} \varepsilon_2$$



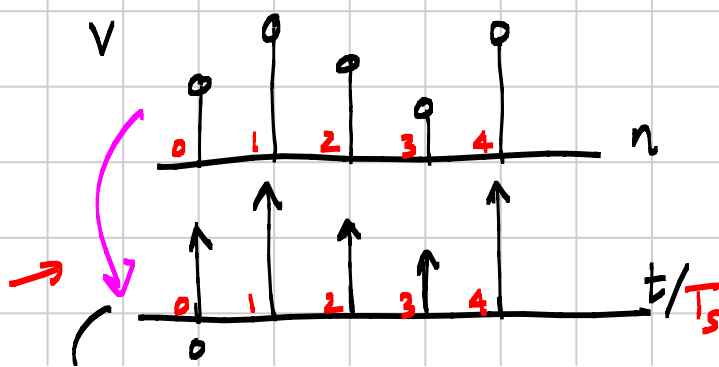
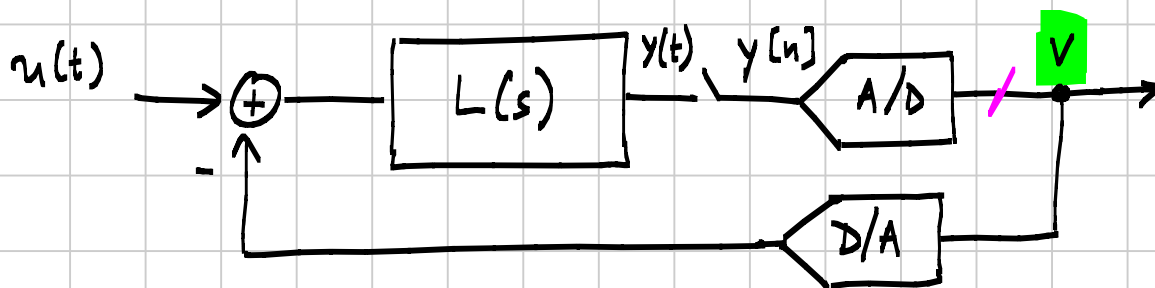
$$V_3 = u + N_1 \epsilon_1 - NTF_{1,d} \epsilon_1 - NTF_{1,d} NTF_{2,a} \epsilon_2$$

$\underbrace{\epsilon_1, NTF_{1,d}}_{\delta \rightarrow \text{Mismatch}}$

↳ Noise Leakage Problem of Cascaded $\Sigma\Delta M$

VLSI Data Conversion Circuits: Lecture 27

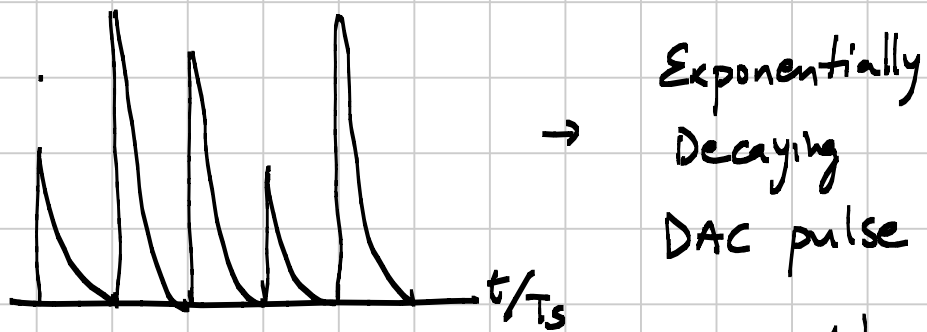
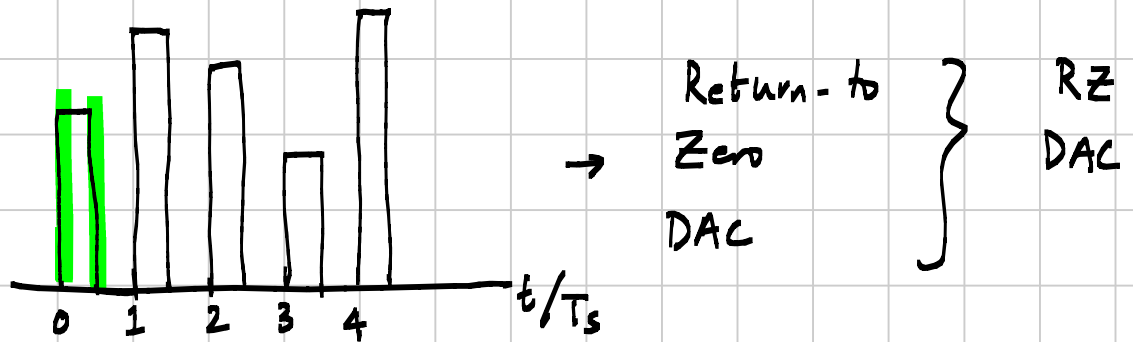
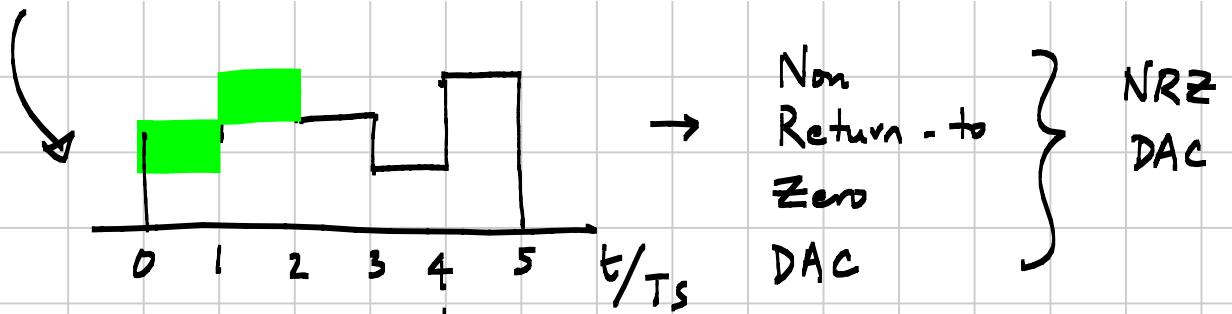
- * Single loop
 - * Cascade structure (MASH)
- Loop Filter
- Sampled Data Filter
 - Switched Capacitor Circuits
 - DT $\Sigma\Delta$ Modulators
 - Continuous-time Filter
 - CT $\Sigma\Delta$ Modulation



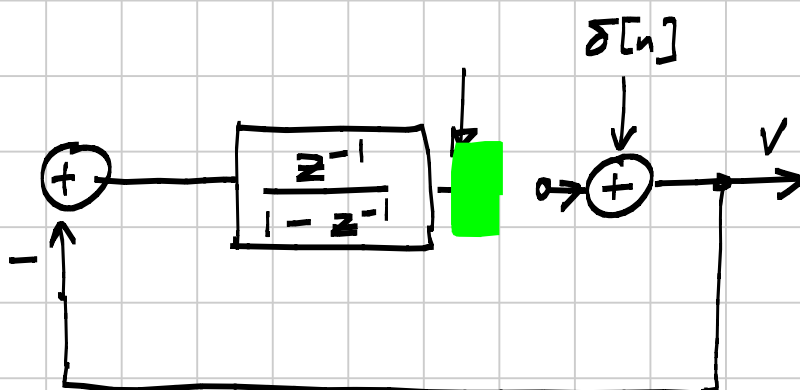
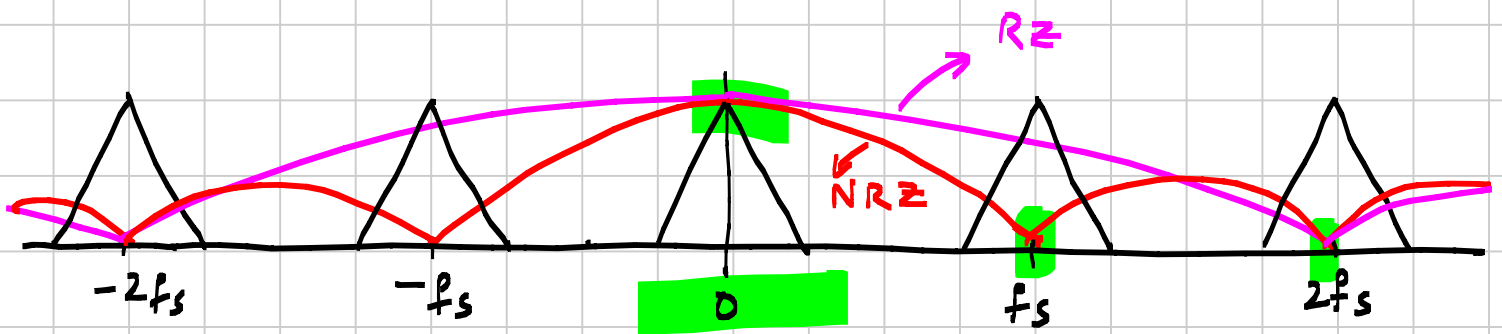
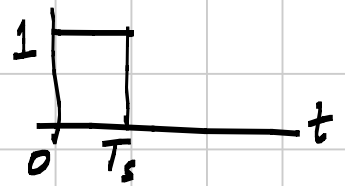
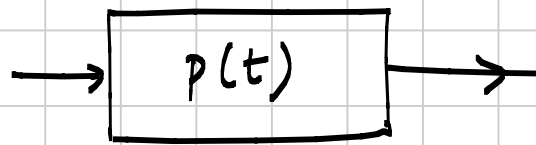
$$X(e^{j\omega}) = \sum x[n] e^{-j\omega n}$$

$$X(f) = \sum x[n] e^{-j2\pi f T_s n}$$

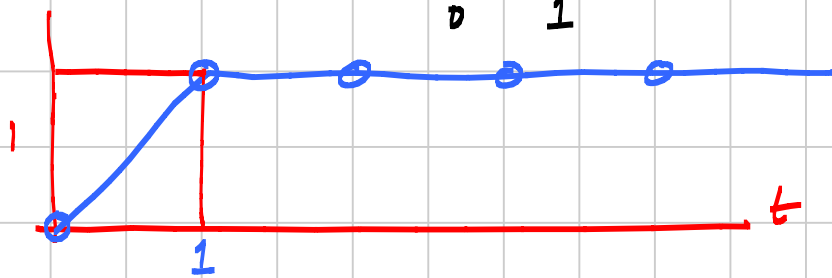
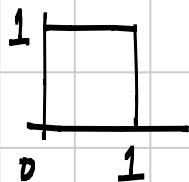
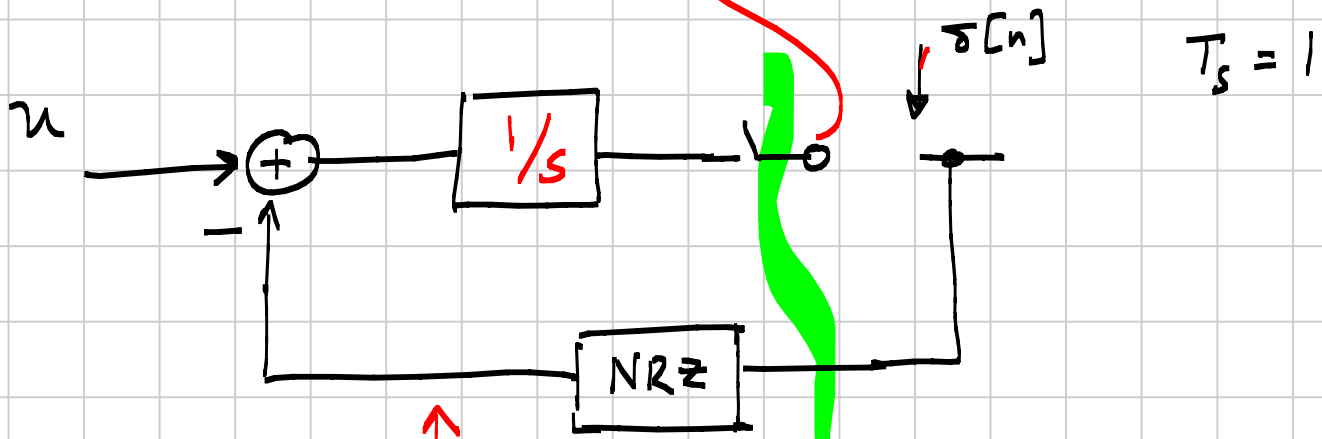
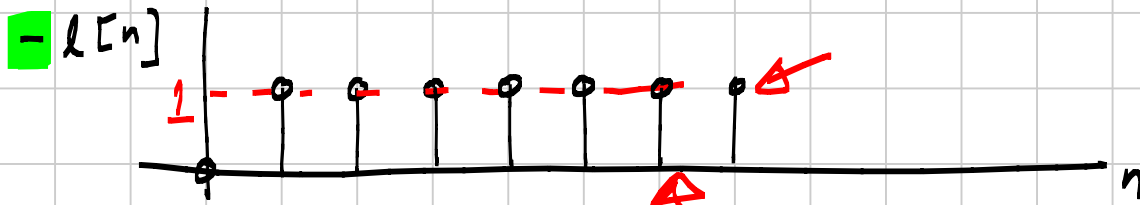
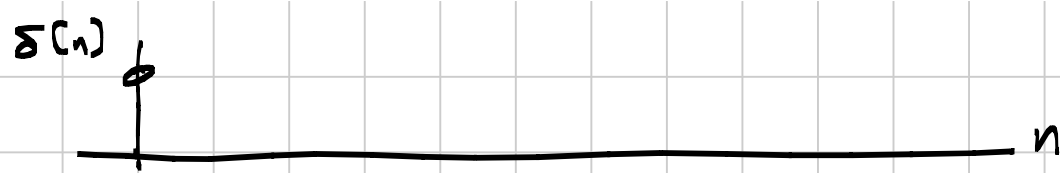
→ Impulsive DAC



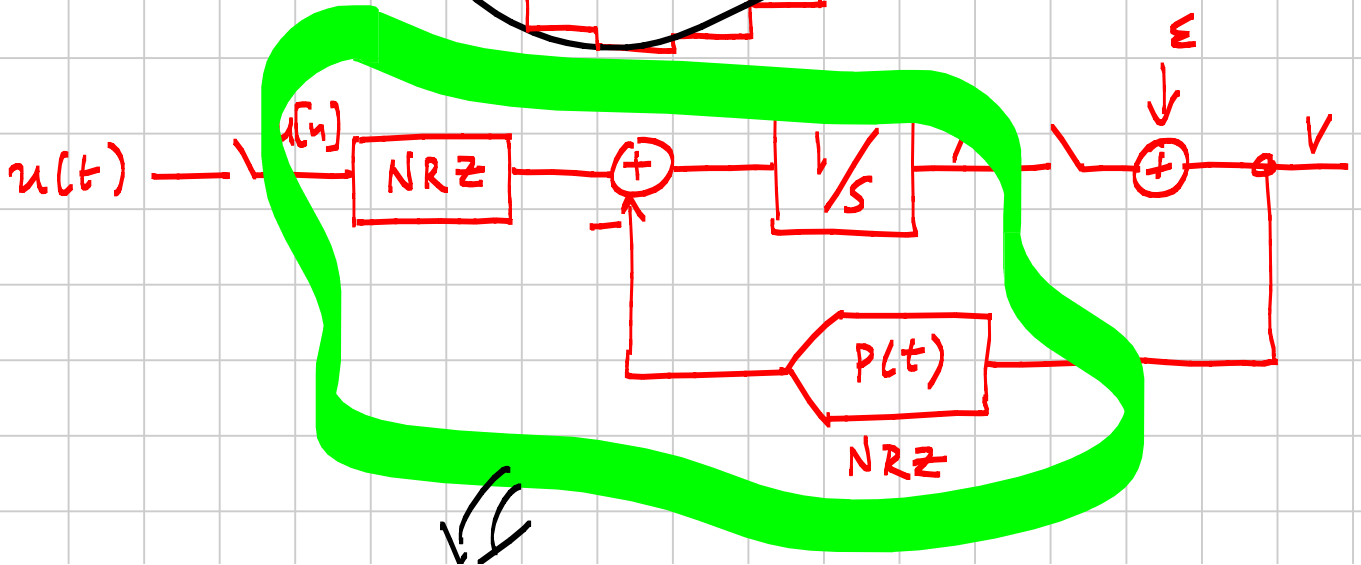
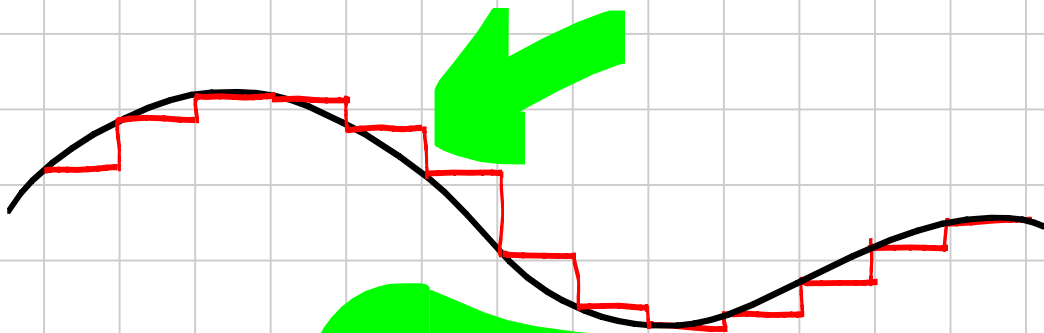
Impulsive DAC Output

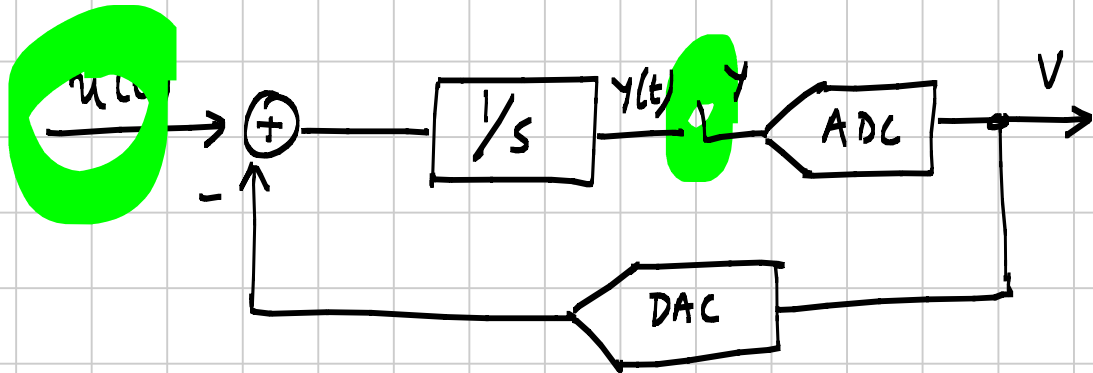
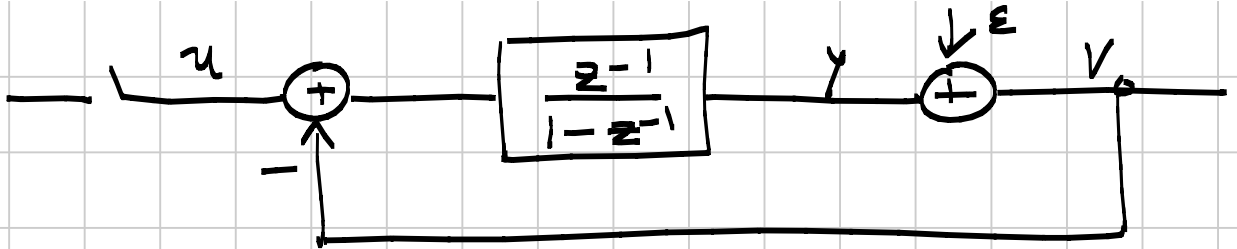


$$V = (1 - z^{-1}) \varepsilon$$



$\{0, 1, 1, 1, \dots\}$



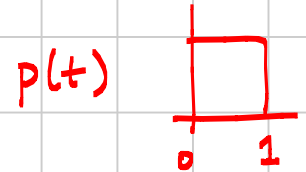
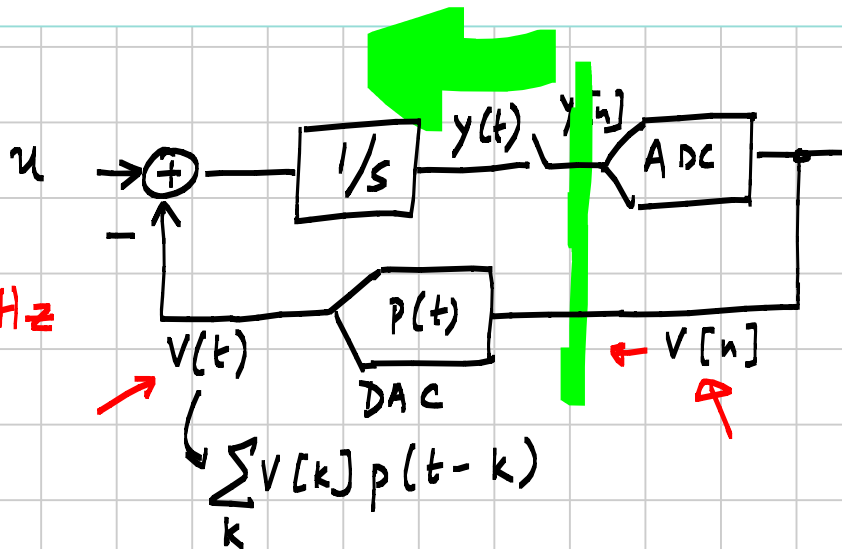


VLSI Data Conversion Circuits: Lecture 28

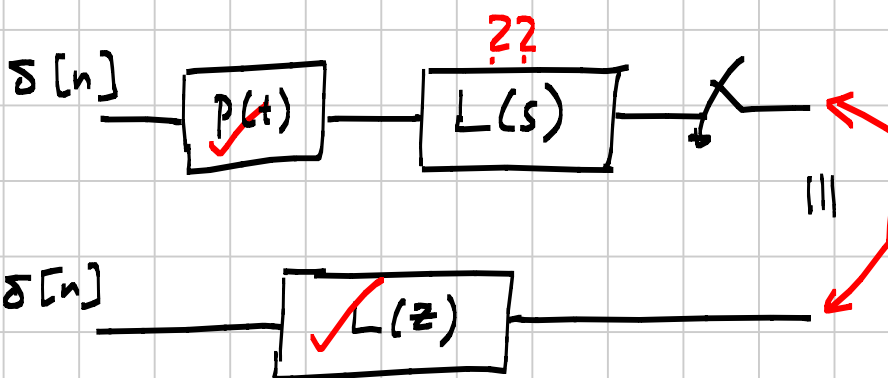
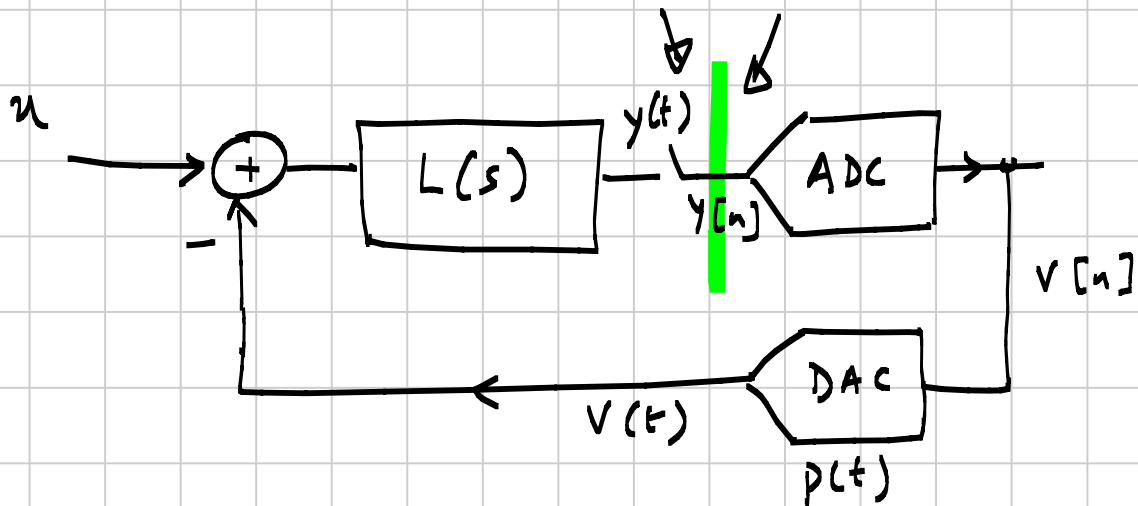
Note Title

17-02-2011

* $f_s = 1 \text{ Hz}$

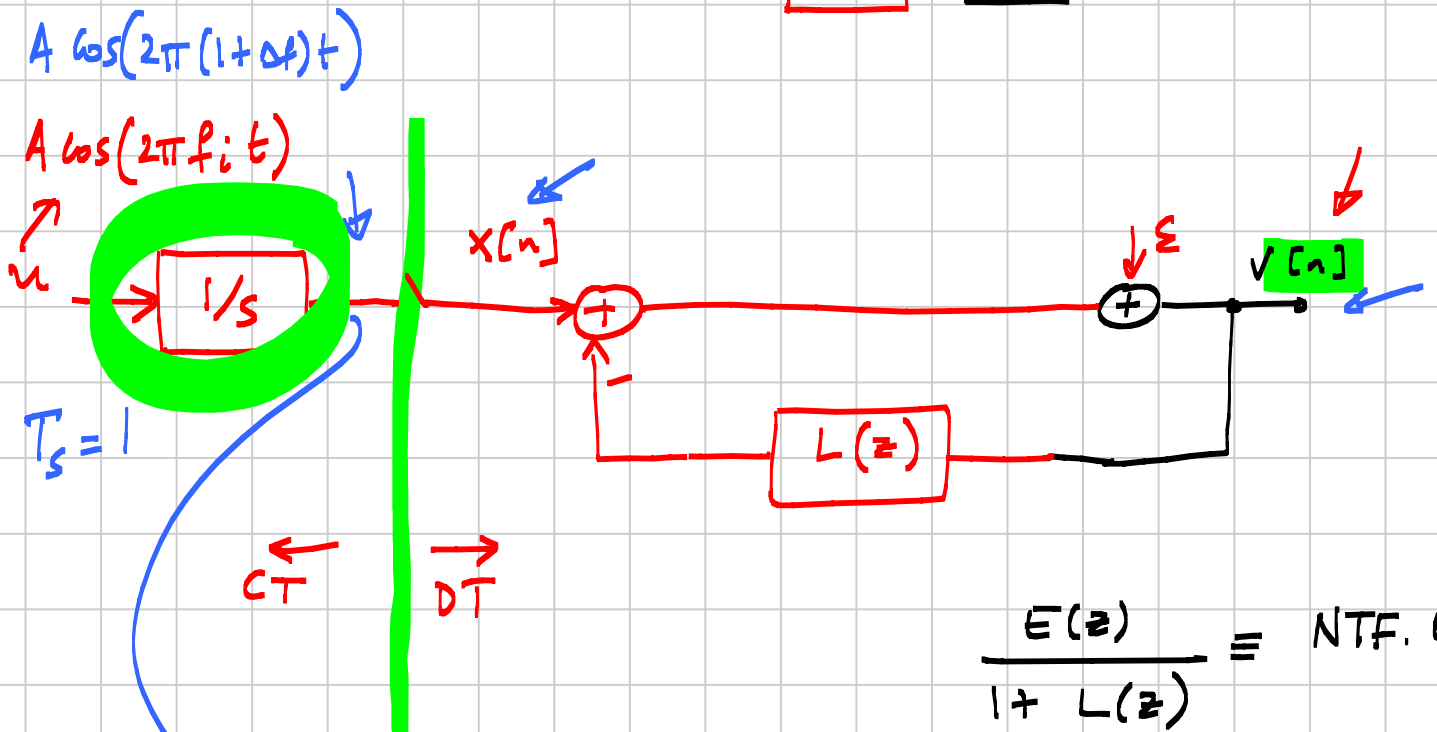
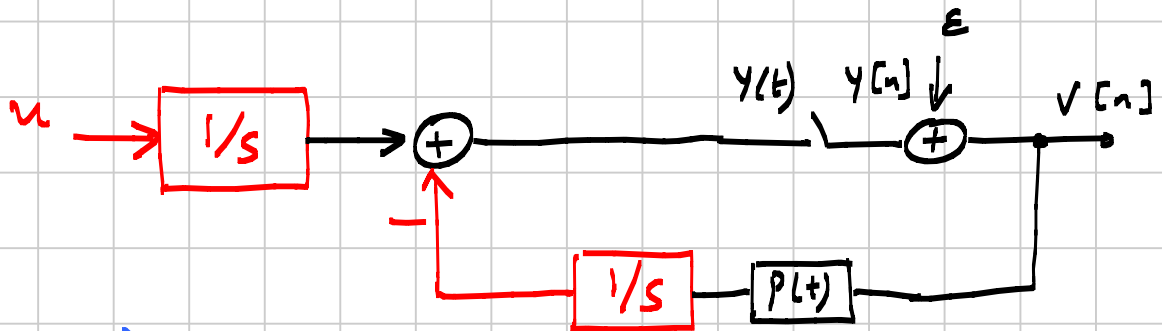
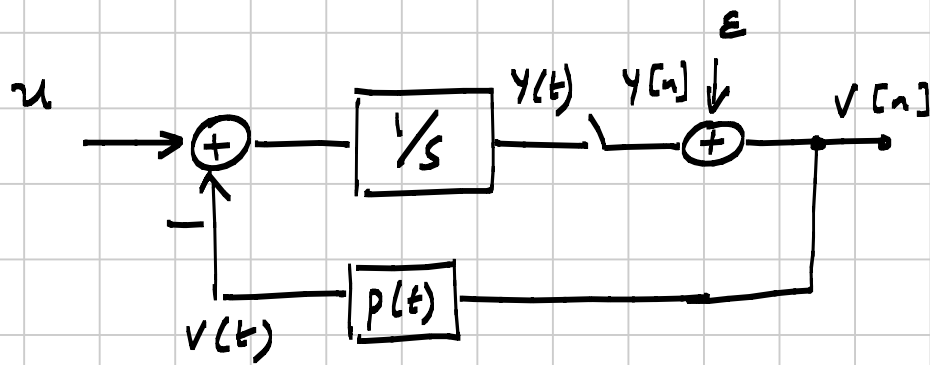


$$\boxed{p(t)} \rightarrow \boxed{1/s} \rightarrow L \equiv \frac{z^{-1}}{1-z^{-1}}$$

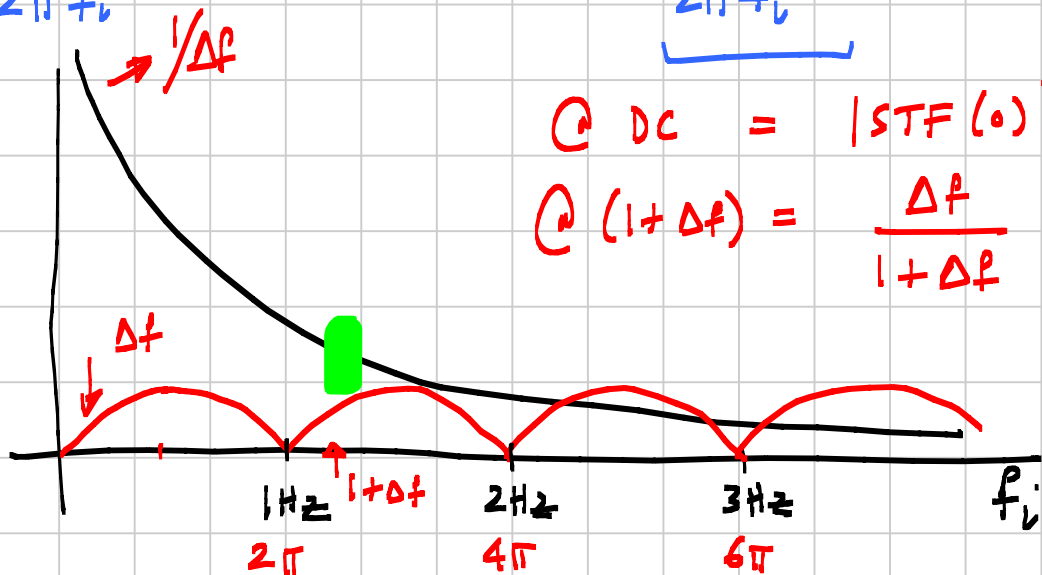


$$NTF(z) = \frac{1}{1+L(z)}$$

"Impulse Invariance"

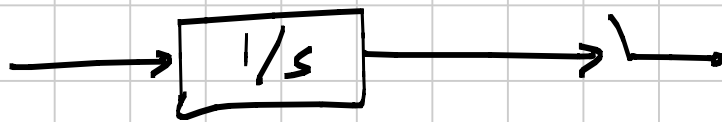


$$\frac{A}{2\pi f_i} \sin(2\pi f_i t) \quad \longleftrightarrow \quad \frac{A}{2\pi f_i} \sin(2\pi f_i n)$$



$$@ \text{DC} = |STF(0)| = 1$$

$$@ (1+\Delta f) = \frac{\Delta f}{1+\Delta f}$$



$$A \cos(2\pi \Delta f t)$$

$$\frac{A}{2\pi \Delta f} \sin(2\pi \Delta f n)$$

$$A \cos(2\pi (1 + \Delta f) t)$$

$$\frac{A}{2\pi (1 + \Delta f)} \sin(2\pi \Delta f n)$$

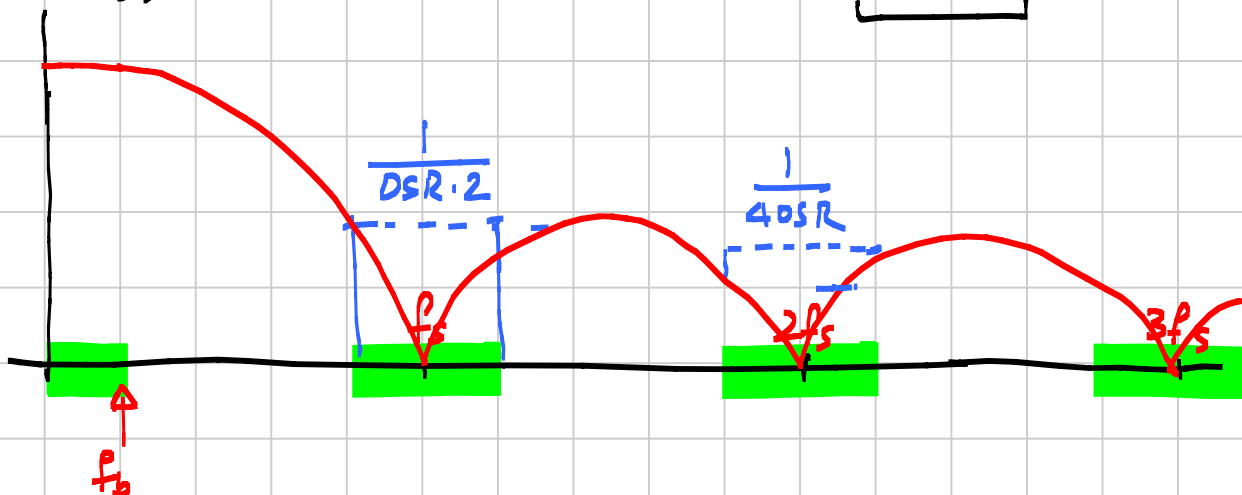
$$\frac{\text{STF}(\Delta f)}{\text{STF}(1 + \Delta f)} = \frac{1 + \Delta f}{\Delta f}$$

$$|\text{STF}(1 + \Delta f)| = |\text{STF}(\Delta f)| \cdot \frac{1}{2\text{OSR}}$$

$\frac{1}{2\text{OSR}}$

For $\Delta f = 0$, $\text{STF}(1) = 1 \cdot 0 = 0$!

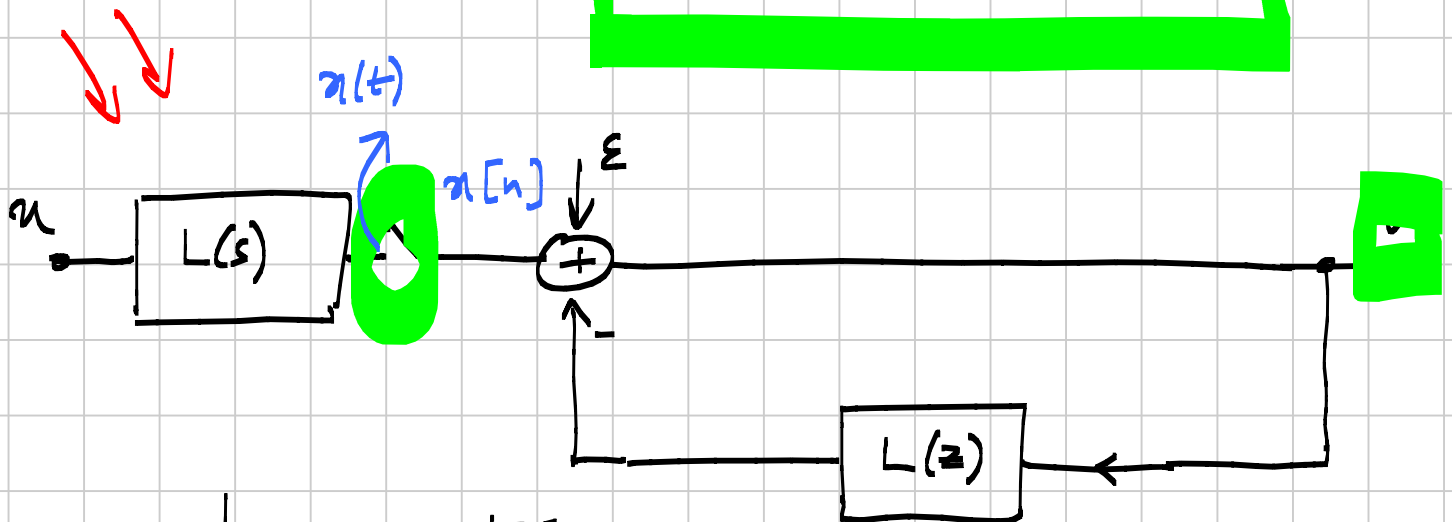
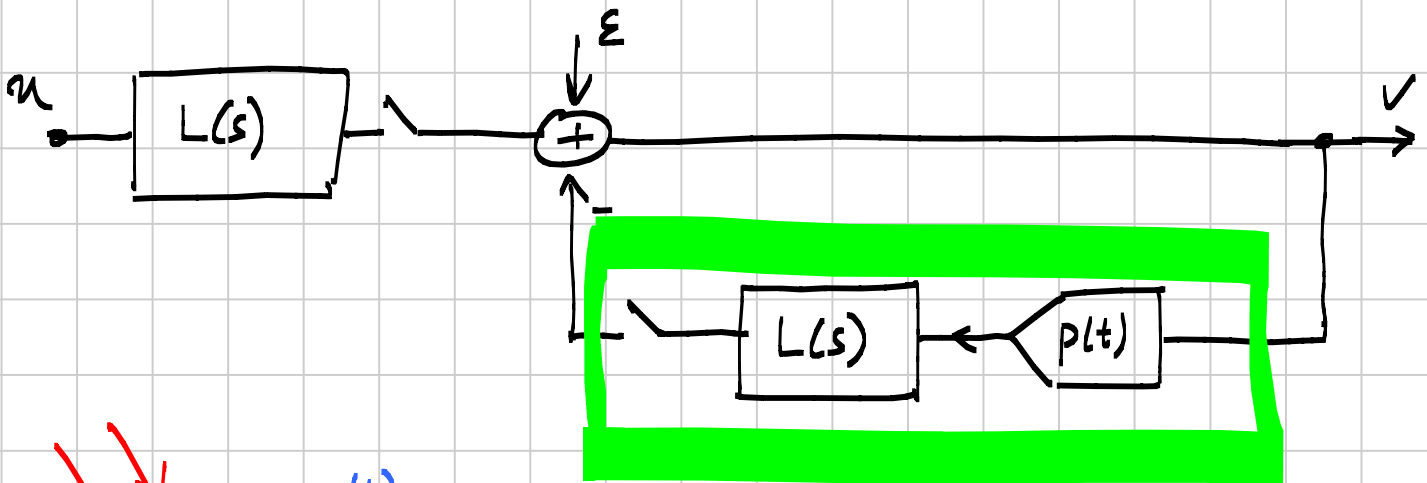
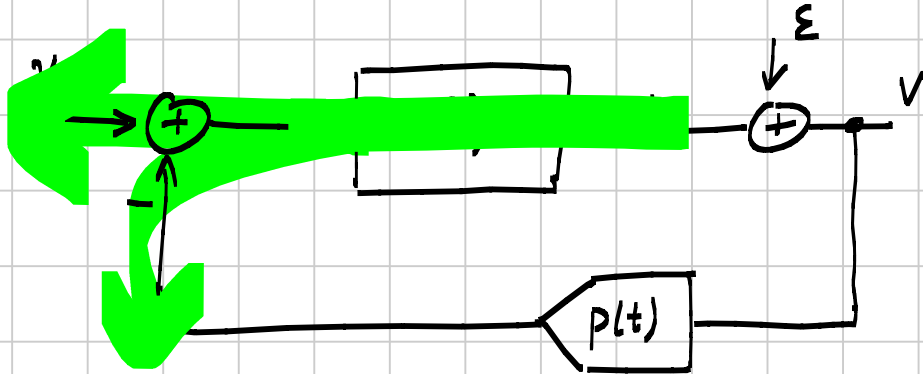
$$\frac{P_{in}}{f_s/2} = \frac{1}{\text{OSR}} \rightarrow \frac{P_{in}}{f_s} = \frac{1}{2\text{OSR}}$$



"Implicit Anti-Alias Property"

VLSI Data Conversion Circuits : Lecture 29

Implicit anti-aliasing property of a CT $\Sigma\Delta M$



$$\frac{1}{1 + L(z)} = \text{NTF}$$

$$x(t) = A |L(2\pi(n + \Delta f))| \cos(2\pi(n + \Delta f)t + \phi)$$

$$x[n] = A |L(2\pi(n + \Delta f))| \cos(2\pi \Delta f n + \phi)$$

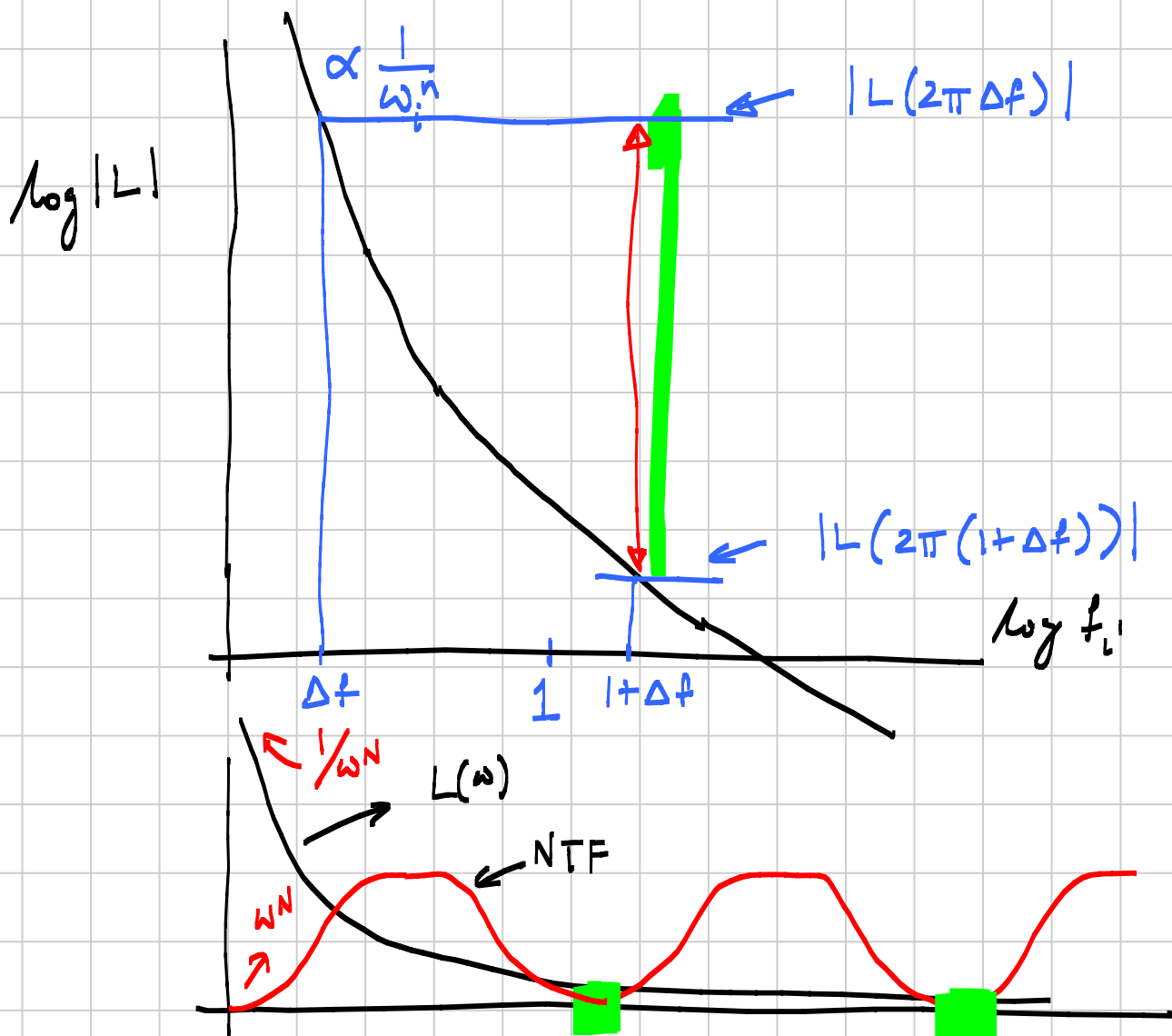
$$STF(n+\Delta f) = |L(2\pi(n+\Delta f))| \cdot NTF(2\pi\Delta f)$$

$$STF(0) \approx STF(\Delta f) = 1$$

$$|STF(n+\Delta f)| = \left| \frac{L(2\pi(n+\Delta f))}{L(2\pi\Delta f)} \right|$$

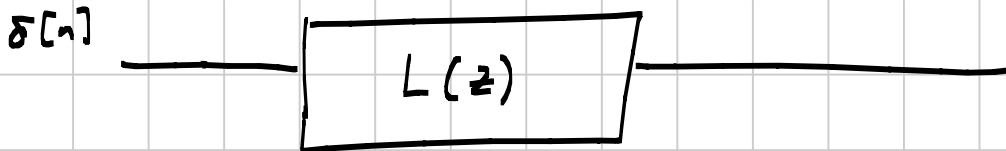
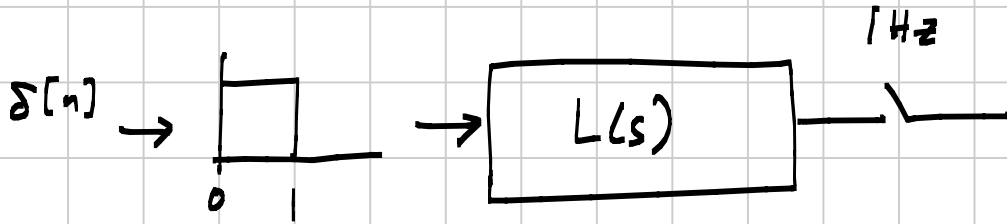
$$STF(n+\Delta f) = |L(2\pi(n+\Delta f))| \cdot NTF(2\pi\Delta f)$$

$$1 \approx STF(\Delta f) = |L(2\pi\Delta f)| \cdot NTF(2\pi\Delta f)$$



$$(1 - z^{-1})^2$$

$$p(t) \rightarrow \text{NRZ}$$



$$\frac{1}{1 + L(z)} = (1 - z^{-1})^2 \Rightarrow$$

$$L(z) = \frac{1}{(1 - z^{-1})^2} - 1 = \frac{1 - (1 - z^{-1})^2}{(1 - z^{-1})^2}$$

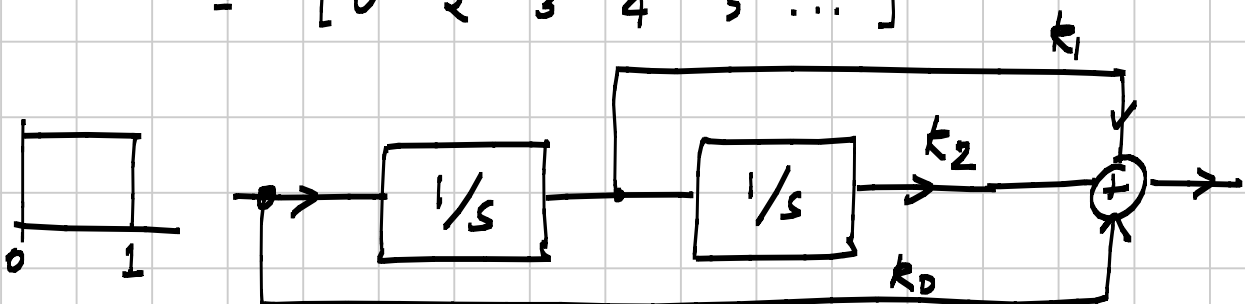
$$= \frac{z^{-1}(1 + 1 - z^{-1})}{(1 - z^{-1})^2}$$

$$= \frac{z^{-1}}{1 - z^{-1}} + \frac{z^{-1}}{(1 - z^{-1})^2}$$

$$l[n] = [0 \ 1 \ 1 \ 1 \ 1 \ \dots]$$

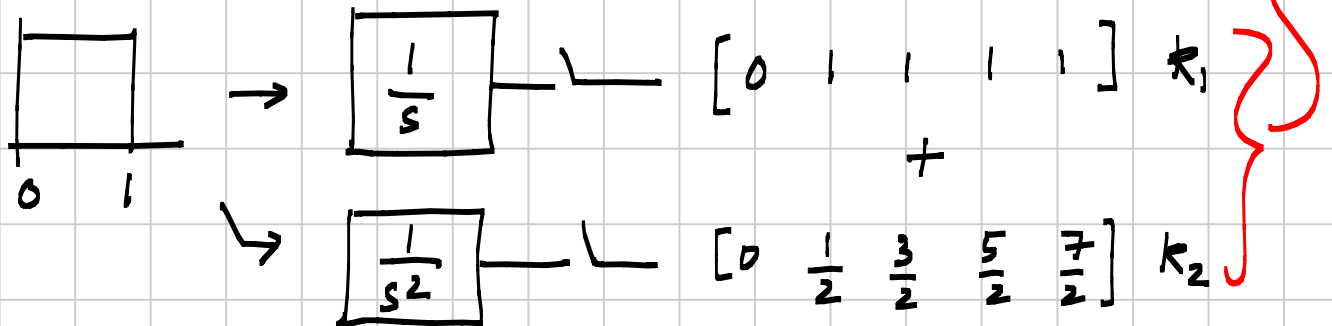
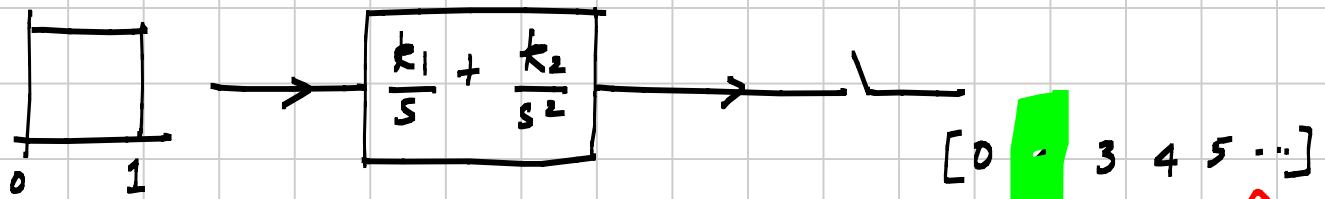
$$+ [0 \ 1 \ 2 \ 3 \ 4 \ \dots]$$

$$= [0 \ 2 \ 3 \ 4 \ 5 \ \dots]$$

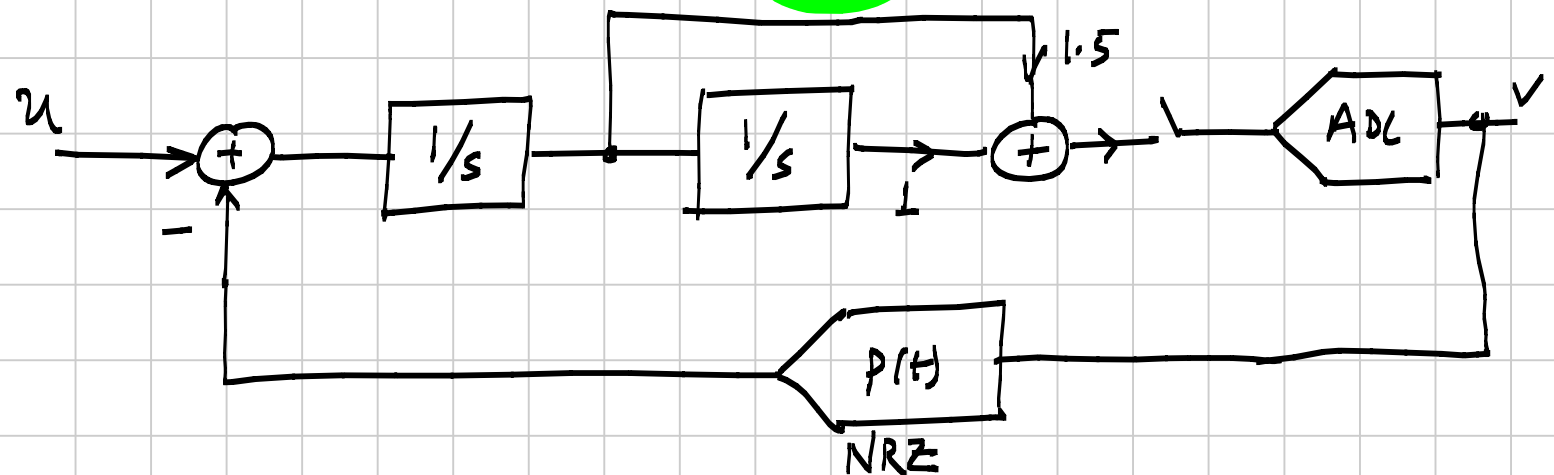


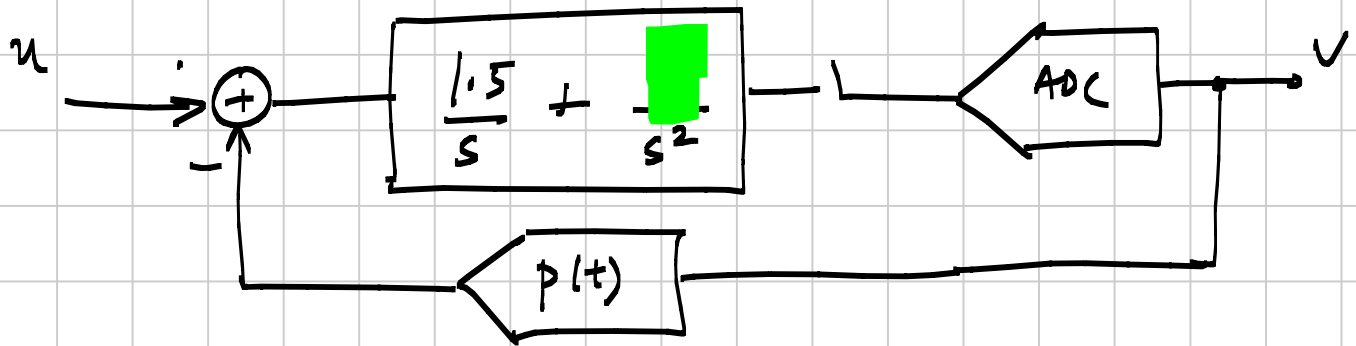
$$L(s) = k_0 + \frac{k_1}{s} + \frac{k_2}{s^2}$$

$\downarrow$
 0 (No delay free loops)



$$k_1 = 1.5 \quad k_2 = 1$$





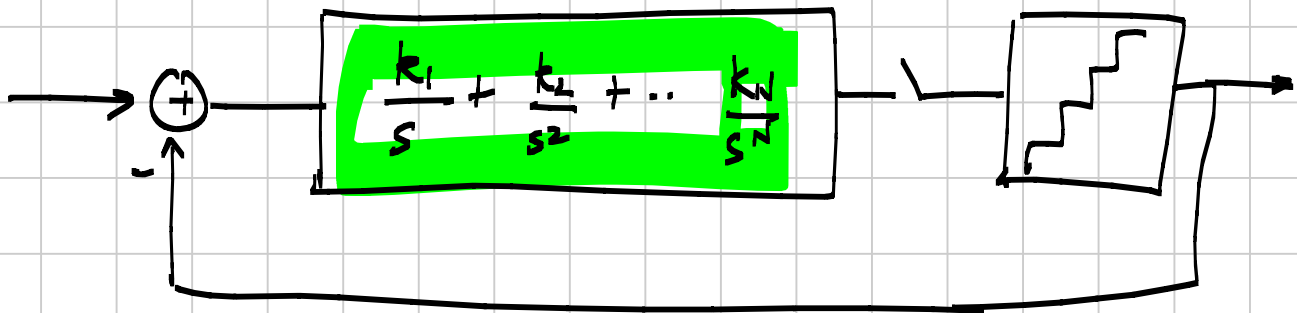
$$\omega \rightarrow 0 \quad NTF \rightarrow \omega^2 \quad \frac{1}{1+L(z)} \rightarrow \omega^2$$

$$\Rightarrow L(z) = 1/\omega^2$$

$$NTF \rightarrow \alpha \omega^N$$

$$L(z) = \frac{1}{\alpha \omega^N}$$

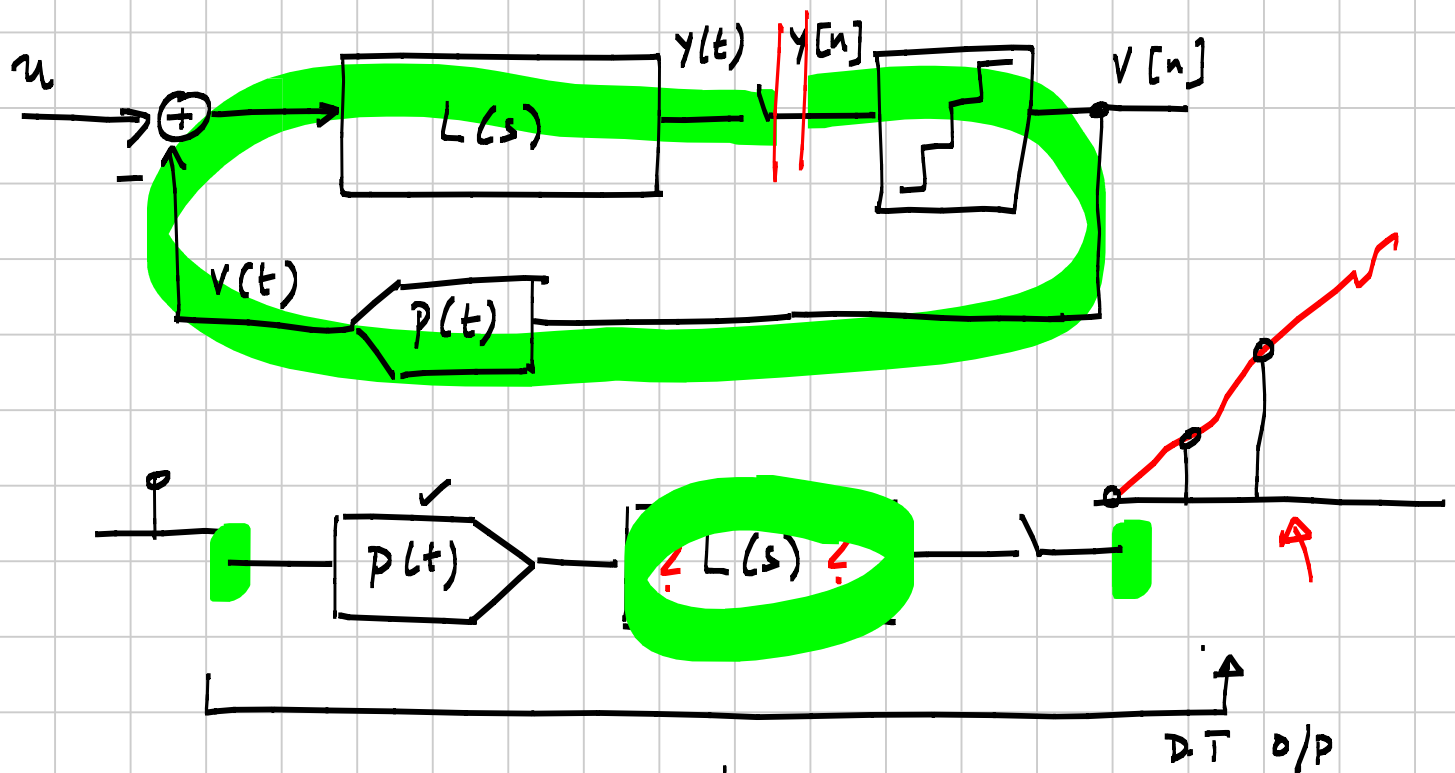
$$\Rightarrow k_N = \frac{1}{\alpha}$$



VLSI Data Conversion Circuits: Lecture 30

Note Title

28-02-2011



$$NTF(z) = \frac{1}{1 + L(z)}$$

Eg. Second order NTF

$$L(s) = \frac{k_1}{s} + \frac{k_2}{s^2}$$

Loop filter $\rightarrow$ pole @ $p_k \Rightarrow$ Impulse response $e^{p_k t}$
 $e^{p_k t} \xrightarrow{1 \text{ Hz}} [e^{p_k}]^n \Rightarrow$ D.T pole @ e^{p_k}

Example :-

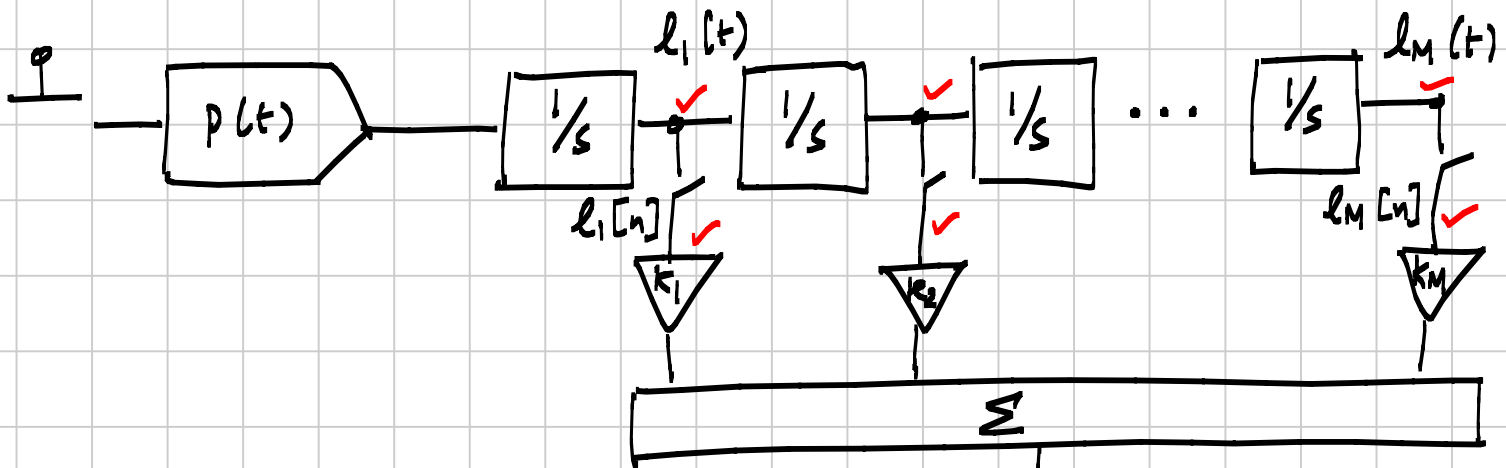
$$a^n u[n] \xleftrightarrow{z} \frac{1}{1 - az^{-1}}$$

C.T $p_k = 0 \Leftrightarrow$ D.T $z_k = 1 \Rightarrow$ Pole is @ $z = a$

$$\text{NTF} = \frac{(1 - z^{-1})^N}{D(z^{-1})} \quad \begin{array}{l} L(z) \text{ has } N \text{ poles @ } z=1 \\ L(s) \text{ " } N \text{ poles @ } s=0 \end{array}$$

$$\Rightarrow L(s) = \frac{k_1}{s} + \frac{k_2}{s^2} + \dots + \frac{k_N}{s^N}$$

$$= \frac{k_1 s^{N-1} + \dots + k_N}{s^N}$$



Given $\text{NTF} = \frac{(1 - z^{-1})^M}{D(z^{-1})} + p(t)$ $k_1 l_1 + k_2 l_2 \dots + k_M l_M$

find $k_1, \dots, k_M$

Step 1: Find $L(z)$ from $\text{NTF} = \frac{1}{1 + L(z)}$

Step 2: Find $l[n]$ corresponding to $L(z)$

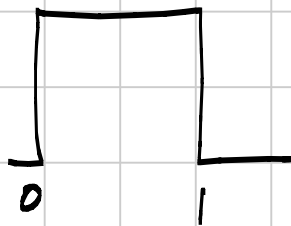
Step 3: $k_1 \underline{l_1[n]} + k_2 \underline{l_2[n]} + \dots + k_M \underline{l_M[n]} = \underline{l[n]}$

$$\begin{bmatrix} \underline{l_1} & \underline{l_2} & \underline{l_3} & \dots & \underline{l_M} \end{bmatrix} \begin{bmatrix} k_1 \\ \vdots \\ k_M \end{bmatrix} = \underline{l} \quad \left. \vphantom{\begin{bmatrix} \underline{l_1} & \underline{l_2} & \underline{l_3} & \dots & \underline{l_M} \end{bmatrix}} \right\} \begin{array}{l} P \\ \text{equations} \end{array}$$

$P \geq M$

$$4f \quad e^{p_k} = z_k \quad \text{or} \quad p_k = \ln z_k$$

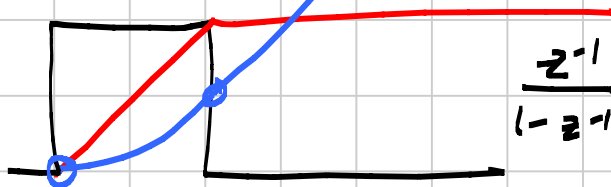
you get a unique solution $k_1 \dots k_M$



$$\rightarrow \boxed{1/s} \rightarrow \{0, 1, \dots\} \frac{z^{-1}}{1-z^{-1}}$$

$$\text{NRZ} \rightarrow \boxed{1/s} \rightarrow \frac{z^{-1}}{1-z^{-1}}$$

$$\text{NRZ} \rightarrow \boxed{1/s^2} \rightarrow [0, \frac{1}{2}, \frac{3}{2}, \frac{5}{2}, \dots]$$



$$\frac{z^{-1}}{1-z^{-1}} \cdot \frac{1}{1-z^{-1}}$$

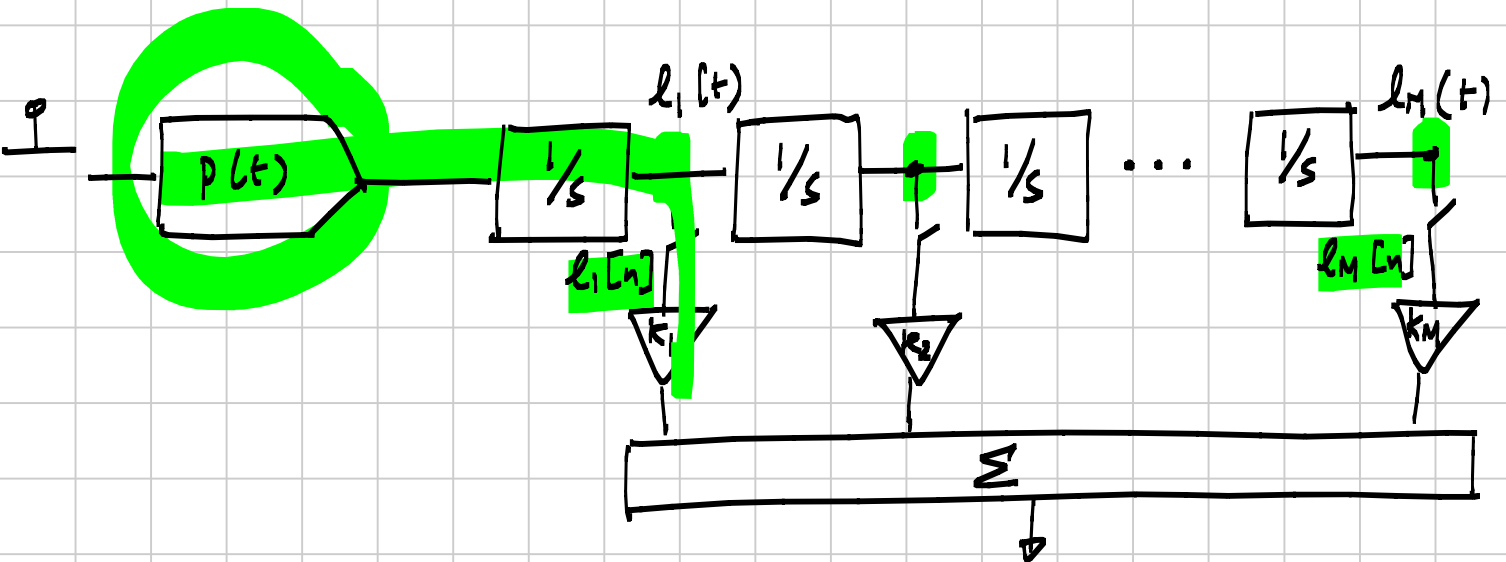
$$0, 1, 1, 1, \dots$$

$$0, 1, 2, 3, \dots$$

$$- 0, \frac{1}{2}, \frac{1}{2}, \frac{1}{2}, \dots$$

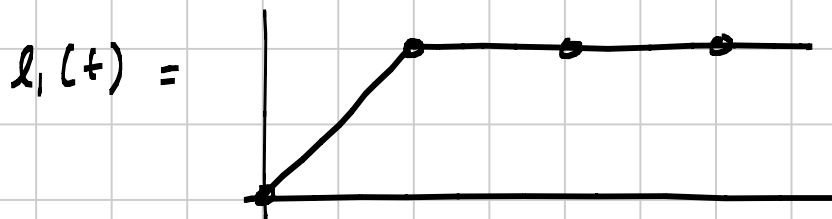
$$\frac{z^{-1}}{(1-z^{-1})^2} = \frac{0.5 z^{-1}}{1-z^{-1}}$$

VLSI Data Conversion Circuits: Lecture 31

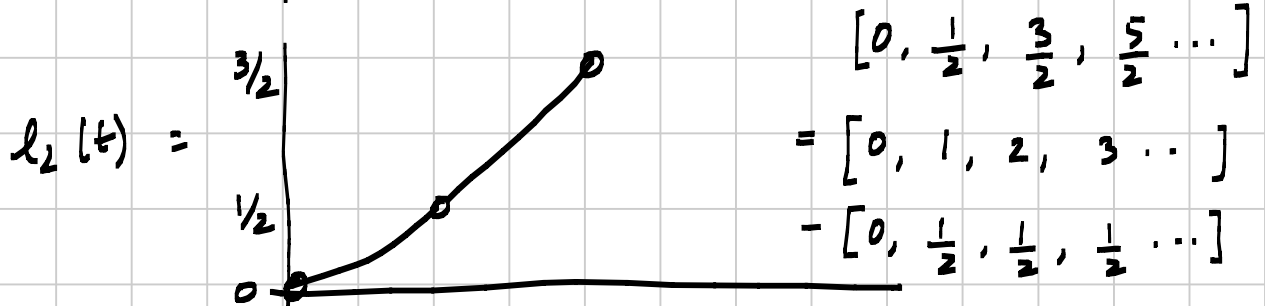


$$k_1 L_1(z) + k_2 L_2(z) + \dots + k_M L_M(z) = L(z)$$

Ex: $p(t) = \text{NRZ pulse}$



$$L_1(z) = \frac{z^{-1}}{1 - z^{-1}}$$



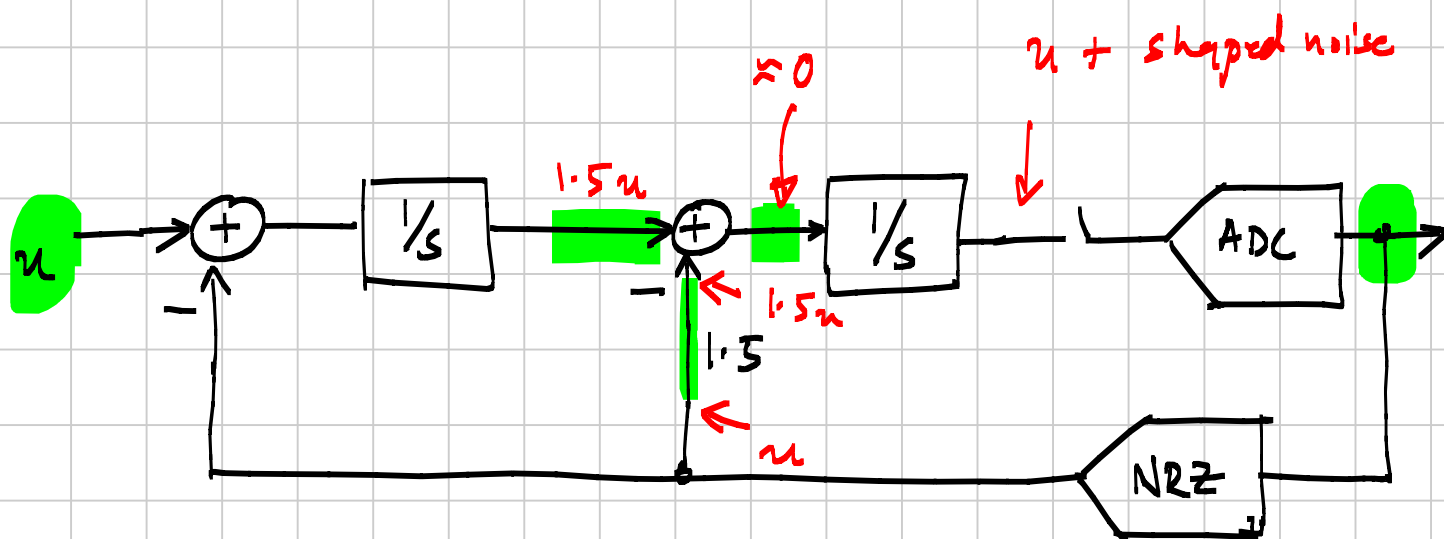
$$\begin{aligned} & [0, \frac{1}{2}, \frac{3}{2}, \frac{5}{2} \dots] \\ & = [0, 1, 2, 3 \dots] \\ & - [0, \frac{1}{2}, \frac{1}{2}, \frac{1}{2} \dots] \end{aligned}$$

$$= \frac{z^{-1}}{(1 - z^{-1})^2} - \frac{0.5 z^{-1}}{(1 - z^{-1})}$$

z-transform method

Loop Filter Implementations

$$L(s) = \frac{k_1}{s} + \frac{k_2}{s^2}$$

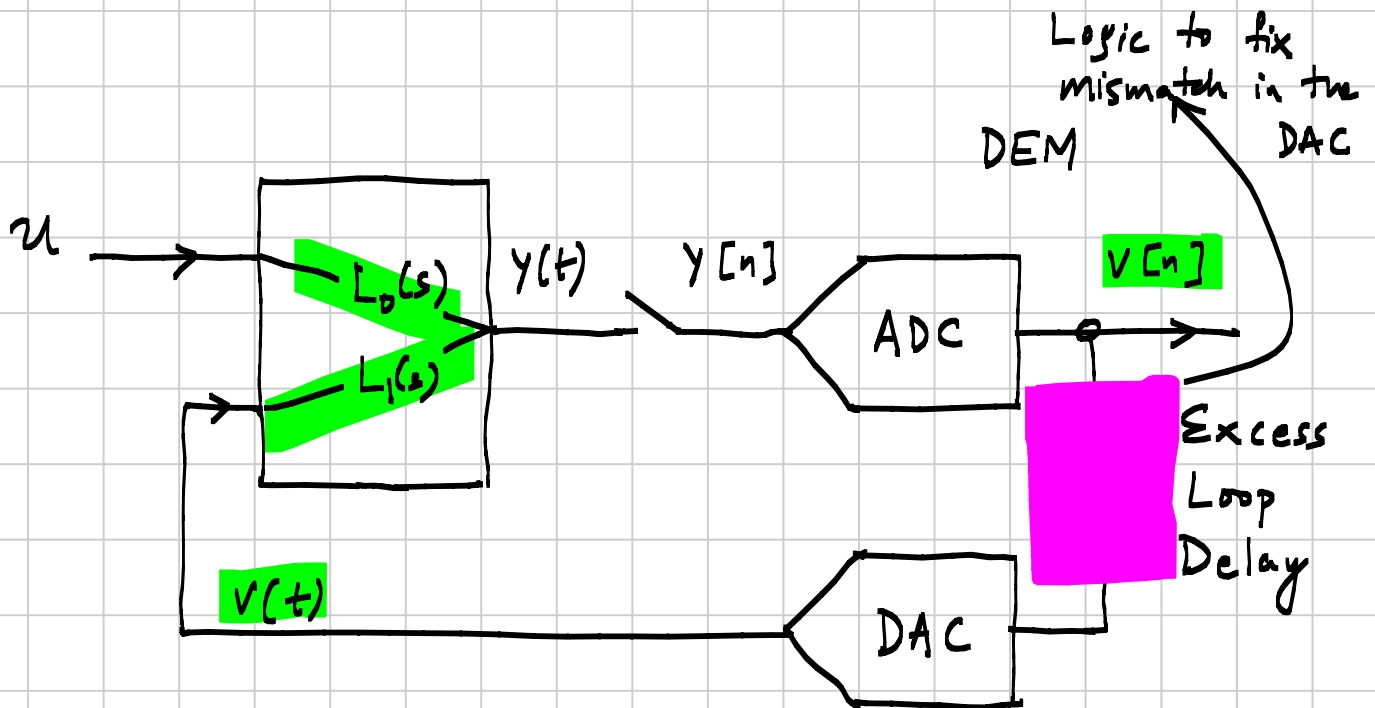


In a CIFB all integrator outputs have a significant input component.

VLSI Data Conversion Circuits: Lecture 32

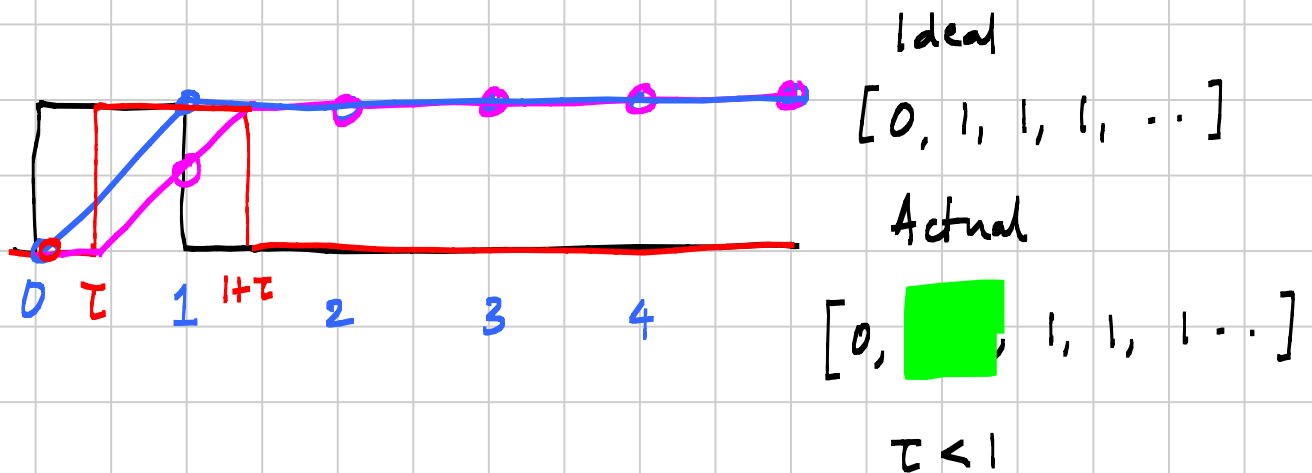
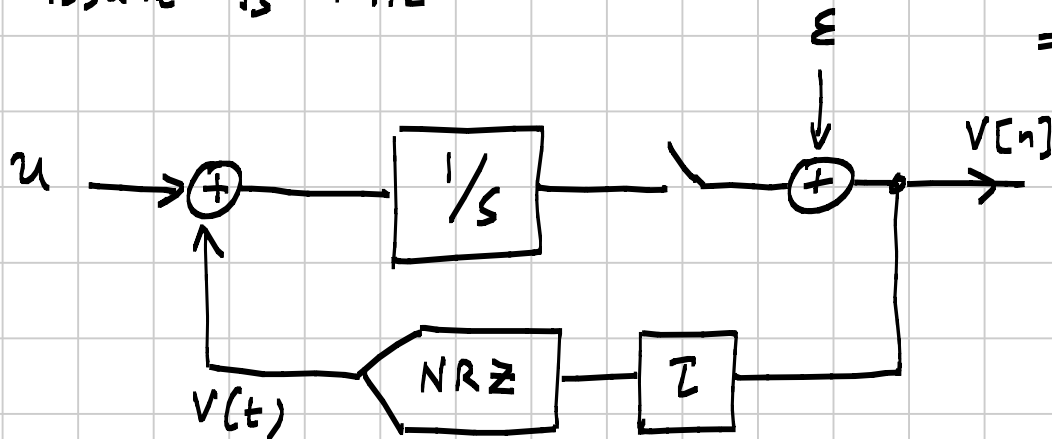
Note Title

05-03-2011



Assume $f_s = 1 \text{ Hz}$

Ideal NTF
 $= 1 - z^{-1}$



Ideal

$$\frac{z^{-1}}{1 - z^{-1}}$$

With ELD

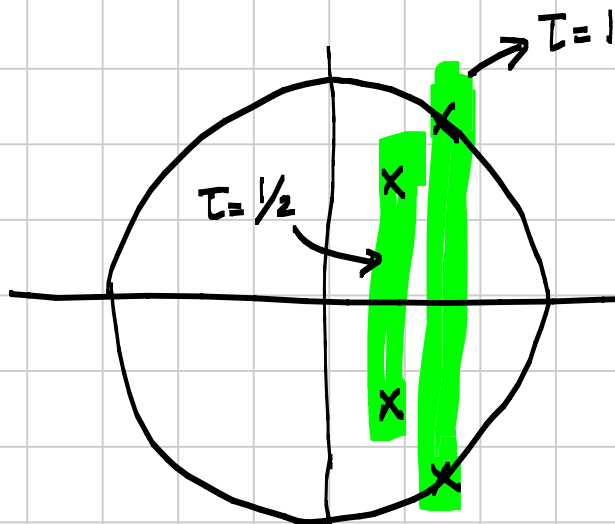
$$\frac{z^{-1}}{1 - z^{-1}} - \tau z^{-1}$$

$$NTF = \frac{1}{1 + \frac{z^{-1}}{1-z^{-1}} - \tau z^{-1}} = \frac{1-z^{-1}}{1 - \tau z^{-1}(1-z^{-1})}$$

$$NTF(z) = \frac{1-z^{-1}}{1 - \tau z^{-1} + \tau z^{-2}}$$

4 real pole location = ($z=0$)

With ELD = $\frac{1}{2} \{ \tau \pm j\sqrt{4\tau - \tau^2} \}$



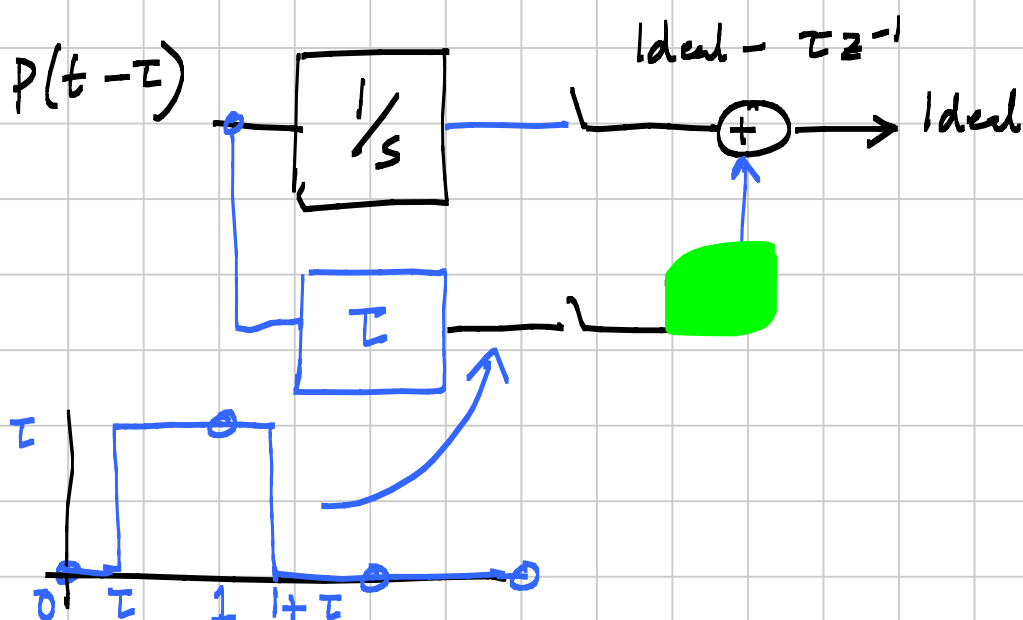
$$\tau = 0.5$$

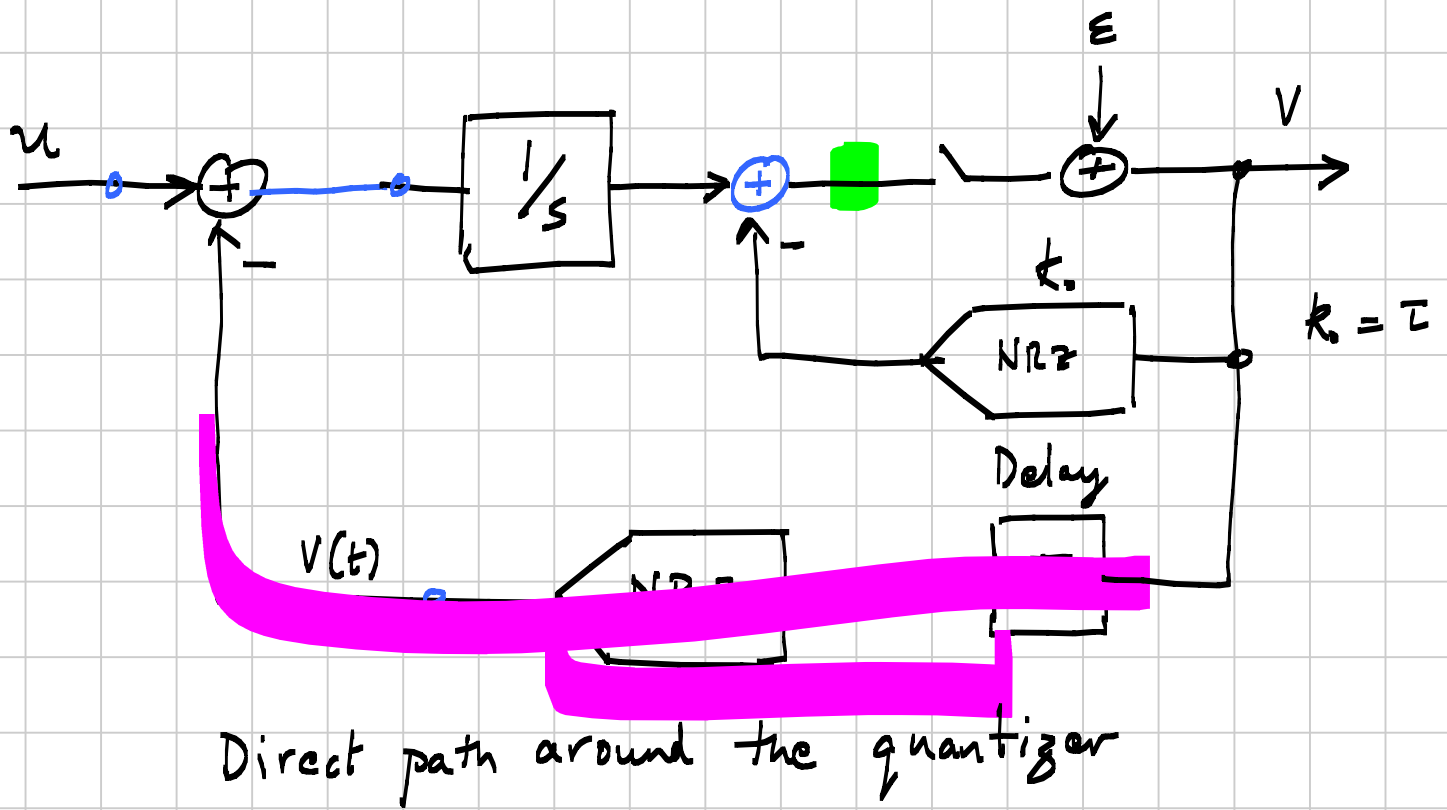
$$\frac{1}{2} \{ 0.5 \pm j\sqrt{1.75} \}$$

$$= 0.25 \pm j\sqrt{0.42}$$

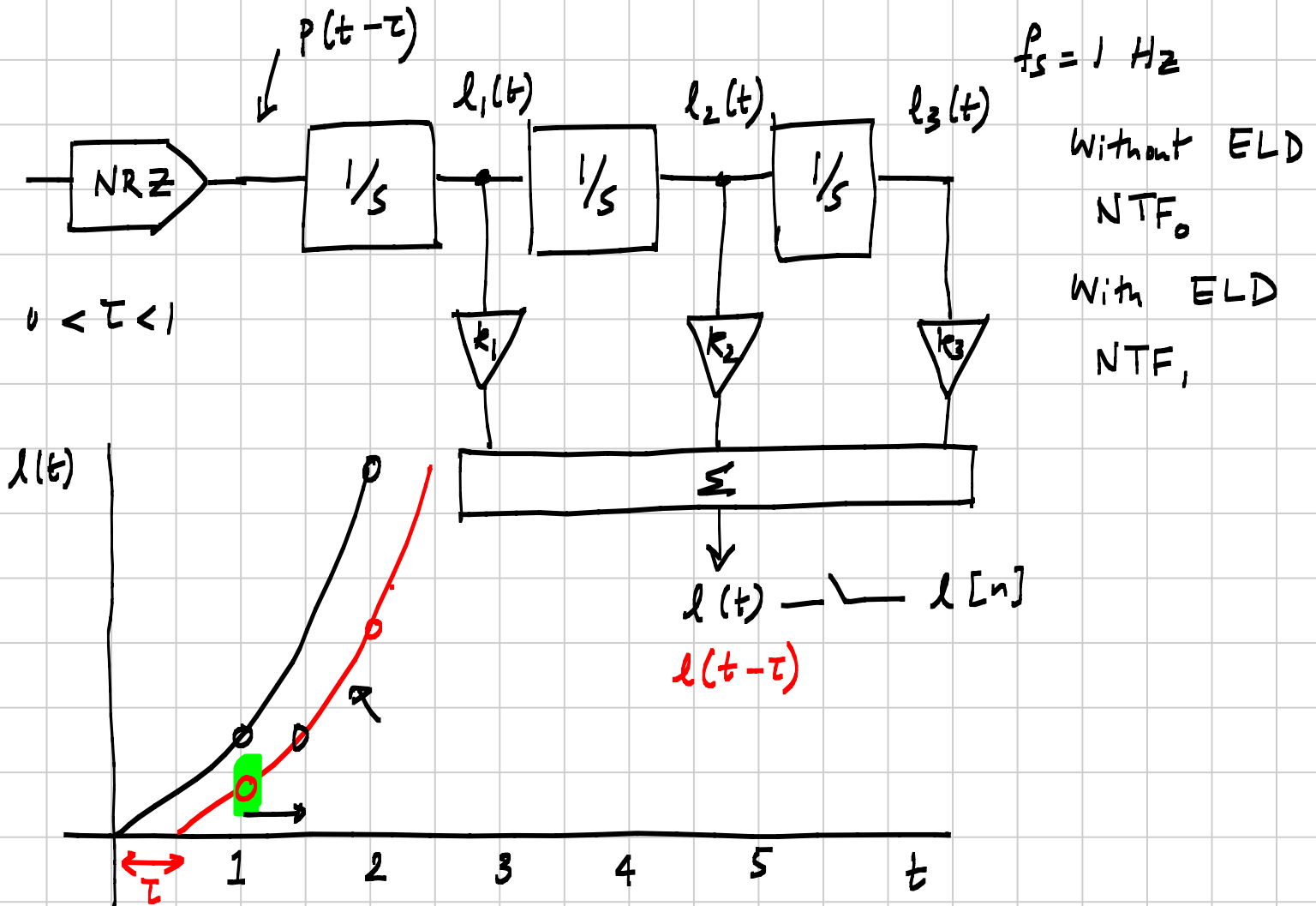
$$\tau = 1$$

$$\frac{1}{2} \{ 1 \pm j\sqrt{3} \}$$





VLSI Data Conversion Circuits: Lecture 33



$$l(t) = k_1 l_1(t) + k_2 l_2(t) + k_3 l_3(t)$$

$$l(t-\tau) = k_1 l_1(t-\tau) + k_2 l_2(t-\tau) + k_3 l_3(t-\tau)$$

$$l(t) = l(t-\tau) + \tau \frac{d l(t-\tau)}{dt} + \frac{\tau^2}{2!} \frac{d^2 l(t-\tau)}{dt^2} + \dots$$

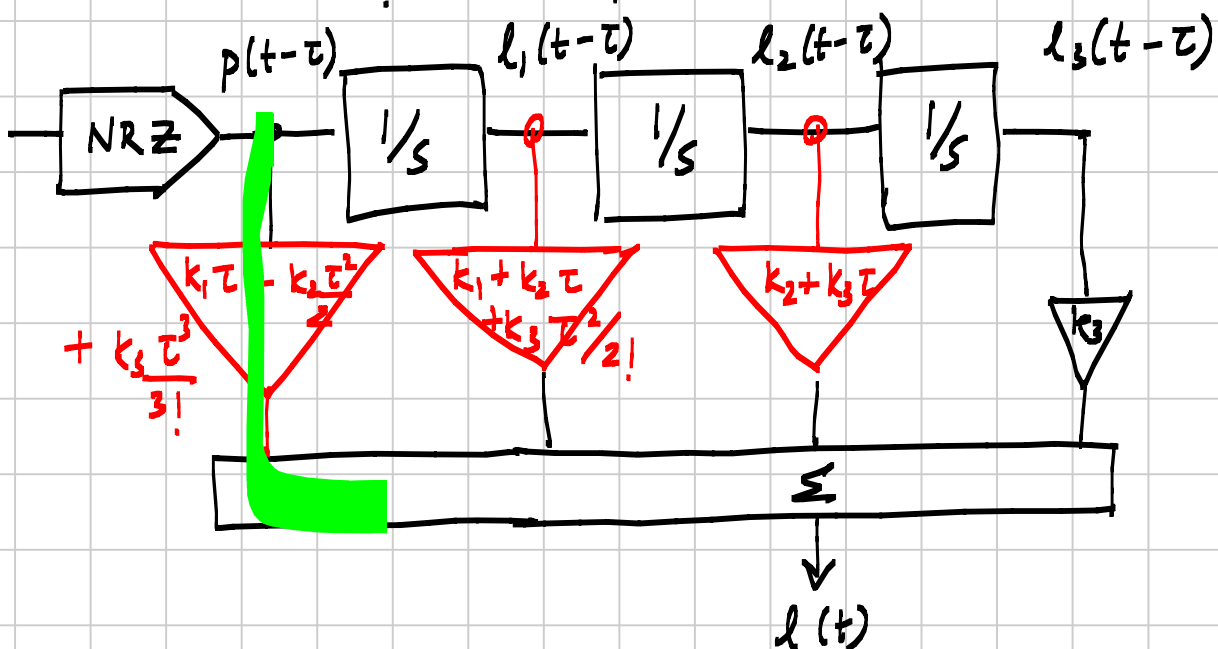
$$l(t) = [k_1 l_1(t-\tau) + k_2 l_2(t-\tau) + k_3 l_3(t-\tau)] \\ + \tau [k_1 \dot{l}_1(t-\tau) + k_2 \dot{l}_2(t-\tau) + k_3 \dot{l}_3(t-\tau)] \\ + \frac{\tau^2}{2!} [k_1 \ddot{l}_1(t-\tau) + k_2 \ddot{l}_2(t-\tau) + k_3 \ddot{l}_3(t-\tau)] \\ + \frac{\tau^3}{3!} [k_1 \dddot{l}_1(t-\tau) + k_2 \dddot{l}_2(t-\tau) + k_3 \dddot{l}_3(t-\tau)]$$

$$= k_3 l_3(t-\tau)$$

$$+ (k_2 + k_3 \tau) l_2(t-\tau)$$

$$+ (k_1 + k_2 \tau + k_3 \frac{\tau^2}{2!}) l_1(t-\tau)$$

$$+ (k_1 \tau + k_2 \frac{\tau^2}{2!} + k_3 \frac{\tau^3}{3!}) p(t-\tau)$$



Without ELD

With ELD

$$k_3$$

$$k_2$$

$$k_1$$

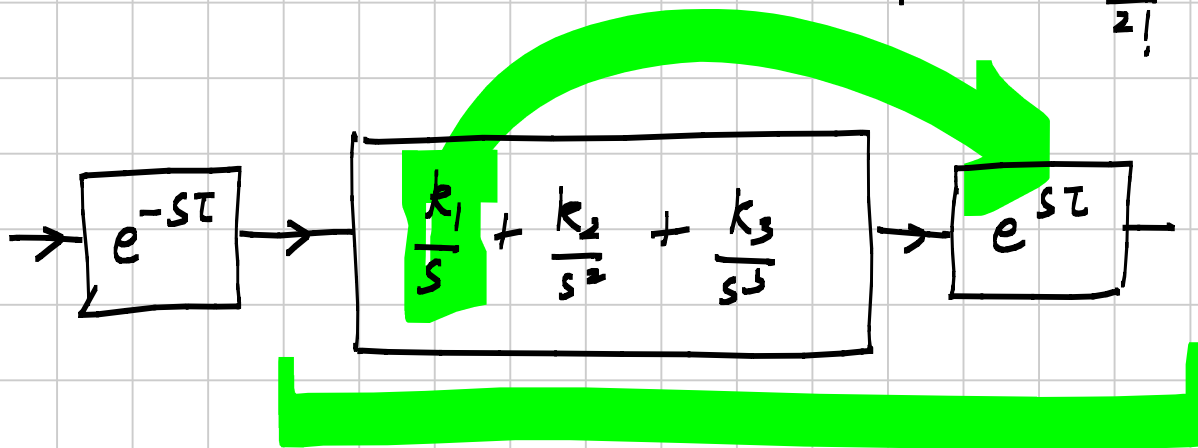
$$0$$

$$\hat{k}_3 = k_3$$

$$\hat{k}_2 = k_2 + k_3 \tau$$

$$\hat{k}_1 = k_1 + k_2 \tau + k_3 \frac{\tau^2}{2!}$$

$$\hat{k}_0 = k_1 \tau + k_2 \frac{\tau^2}{2!} + k_3 \frac{\tau^3}{3!}$$



$$e^{s\tau} = 1 + s\tau + \frac{s^2 \tau^2}{2!} + \frac{s^3 \tau^3}{3!} + \dots$$

$$\frac{k_1}{s} e^{s\tau}$$

$$= \frac{k_1}{s} + k_1 \tau + \frac{k_1 \tau^2}{2!} + \dots$$

$$\frac{k_2}{s^2} e^{s\tau}$$

$$= \frac{k_2}{s^2} + \frac{k_2 \tau}{s} + \frac{k_2 \tau^2}{2!} + \dots$$

$$\frac{k_3}{s^3} e^{s\tau}$$

$$= \frac{k_3}{s^3} + \frac{k_3 \tau}{s^2} + \frac{k_3 \tau^2}{s} + \frac{k_3 \tau^3}{3!} + \dots$$

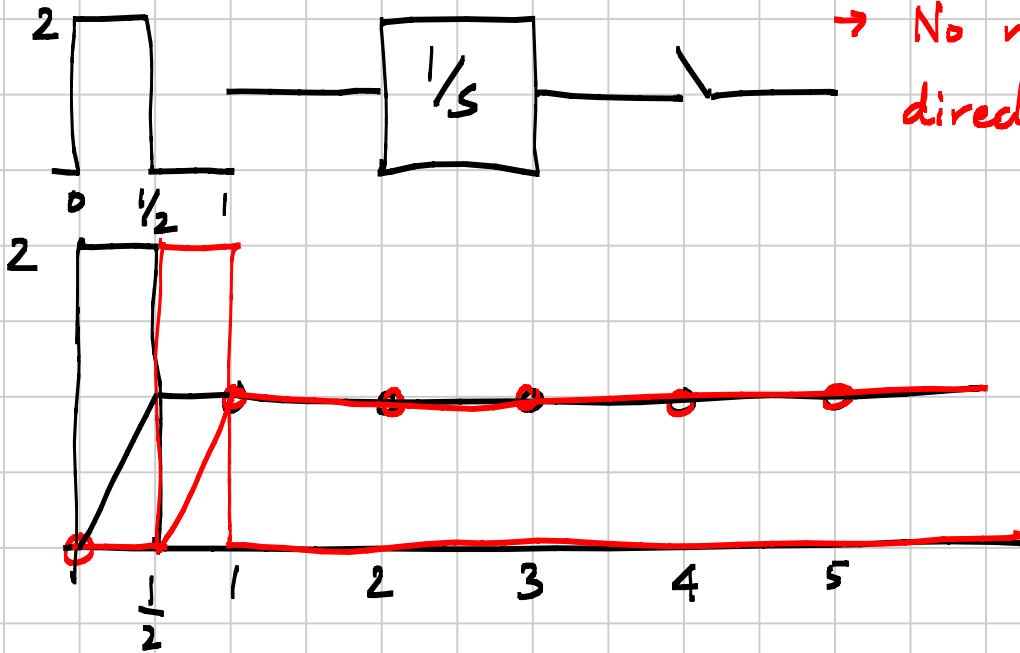
$$\hat{k}_0 = k_1 \tau + k_2 \frac{\tau^2}{2!} + k_3 \frac{\tau^3}{3!} + \dots + \frac{k_N \tau^N}{N!}$$

$$\hat{k}_1 = k_1 + k_2 \tau + k_3 \frac{\tau^2}{2!} + \dots + \frac{k_N \tau^{N-1}}{(N-1)!}$$

$$\hat{k}_{N-1} = k_{N-1} + k_N T$$

k_N

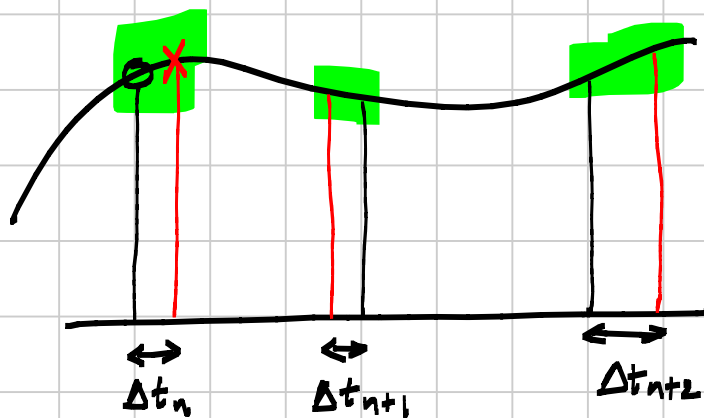
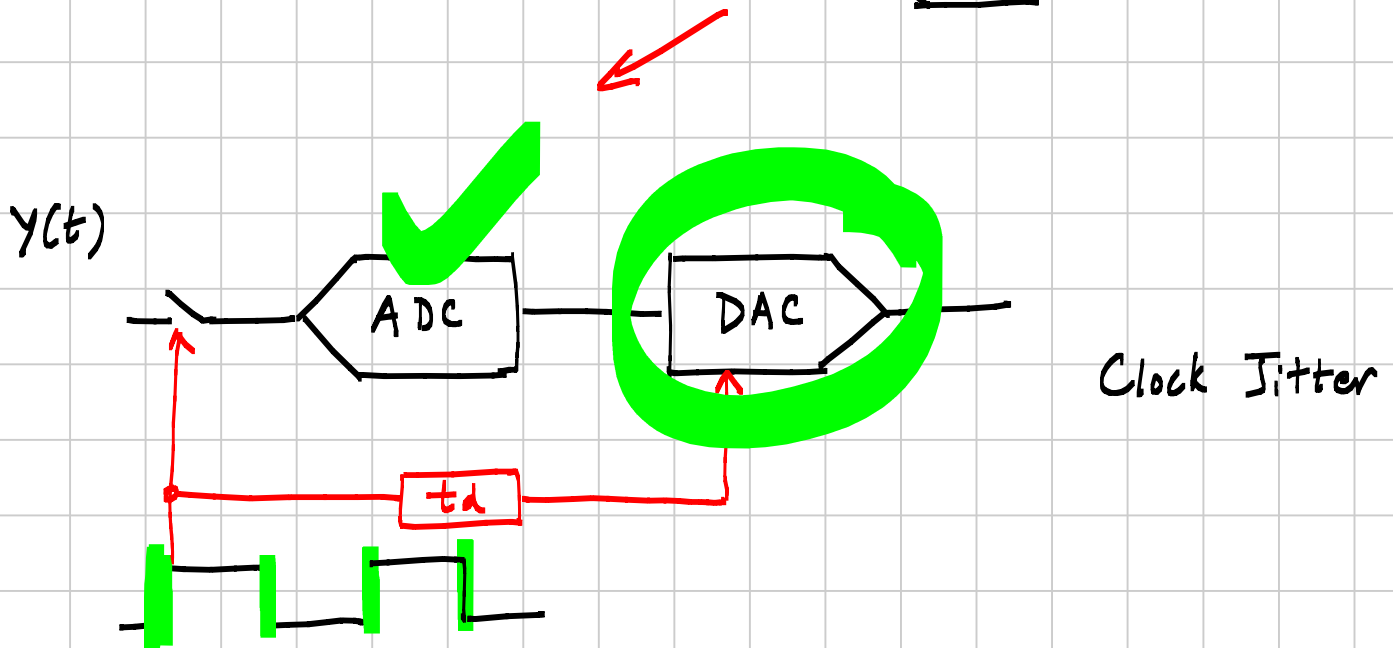
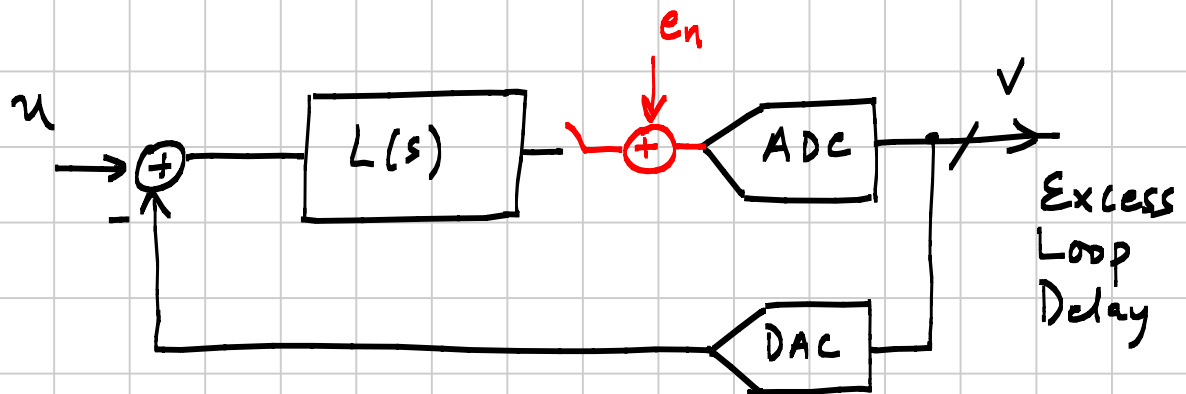
$0 < T < 0.5$ & RZ pulse
 $\rightarrow$ No need for a direct path.



VLSI Data Conversion Circuits : Lecture 34

Note Title

07-03-2011

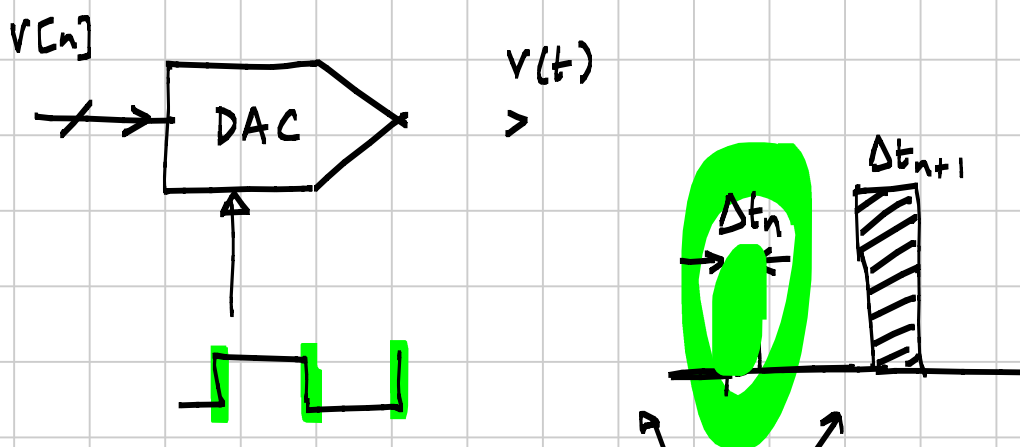
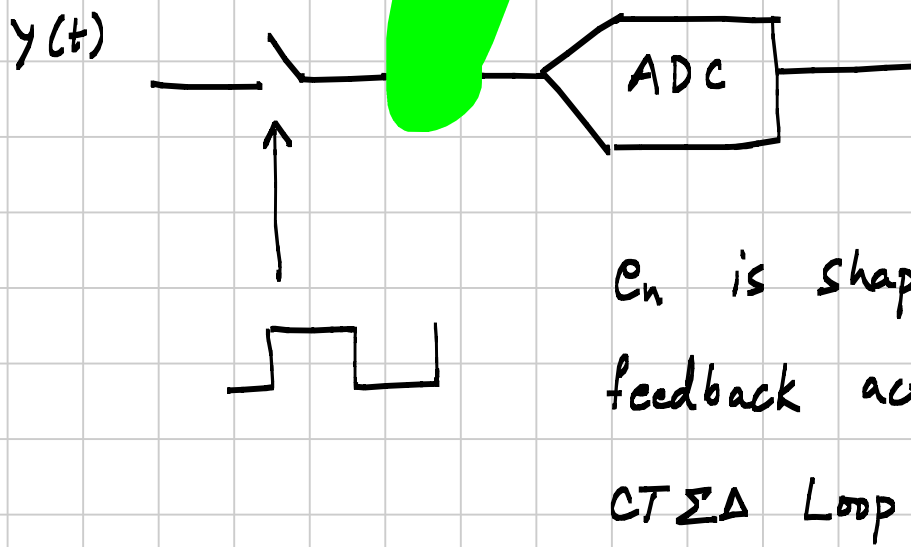


Black : Ideal input samples

Red : Actual samples due to jitter

$$\text{Error in ADC input} \approx \Delta t_n \cdot \left. \frac{dy(t)}{dt} \right|_{t=nT_s}$$

White, Gaussian, $\sigma_{\Delta t}^2$

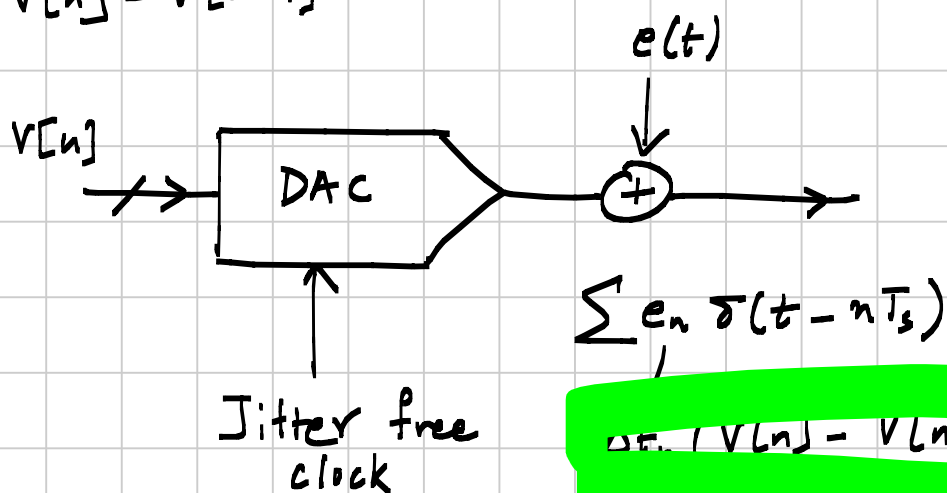
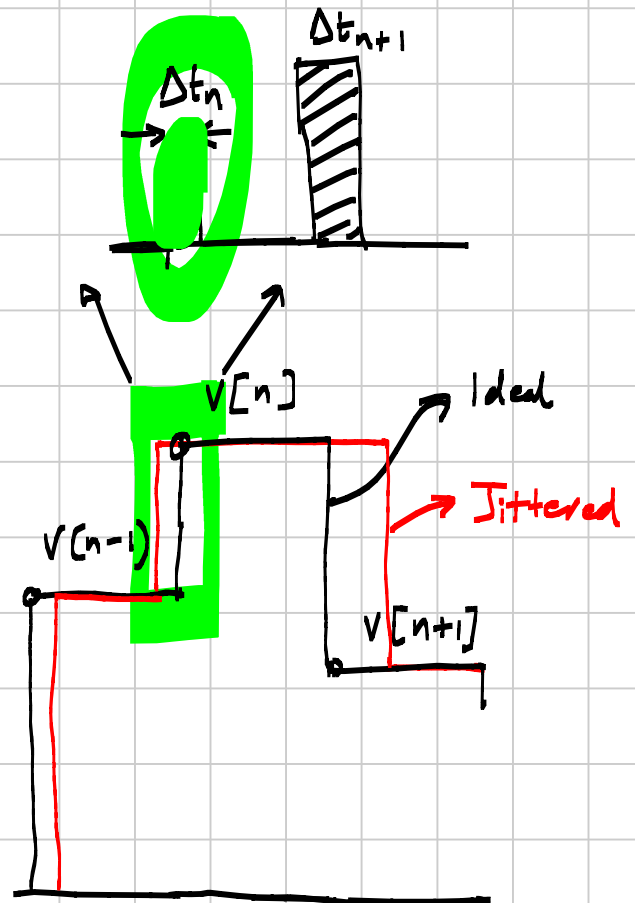


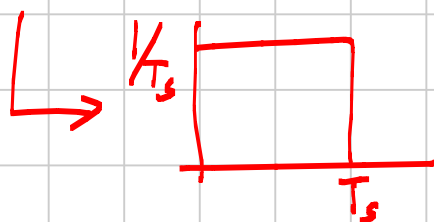
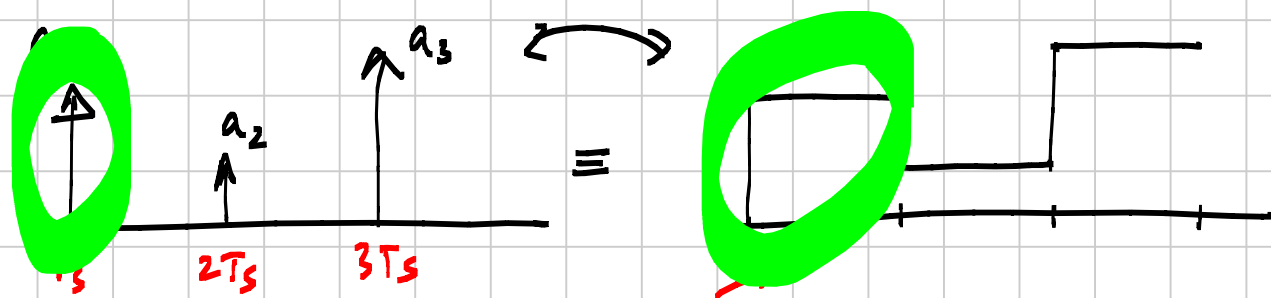
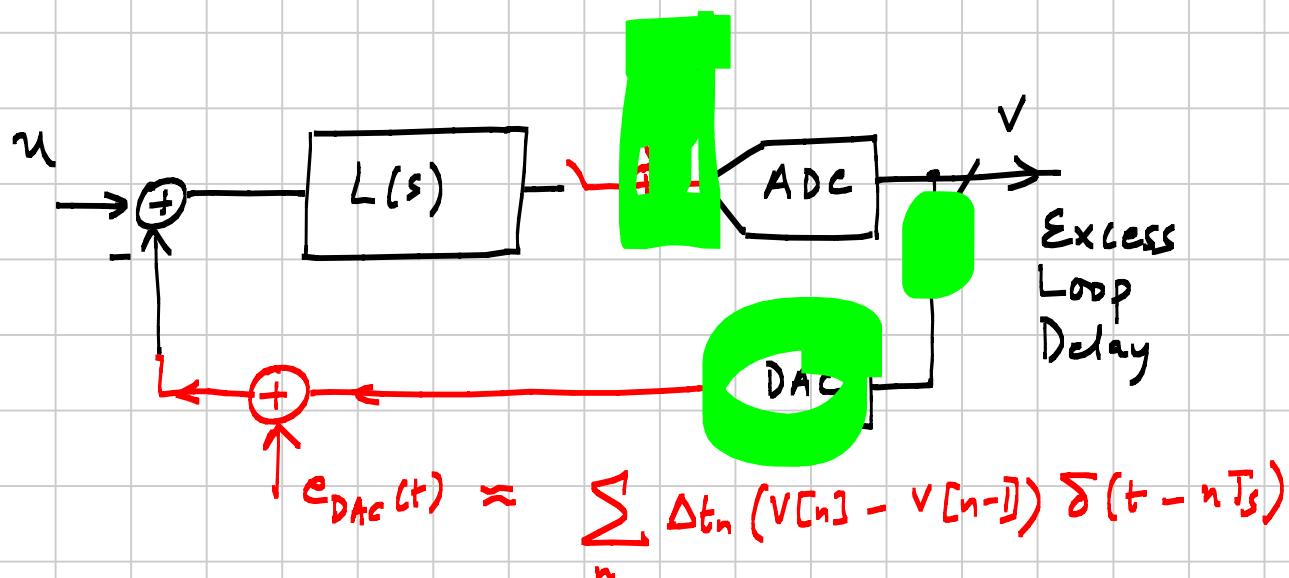
$$\text{Actual} - \text{Ideal} = \text{Error}$$

Error @ n^{th} edge is a pulse

$$\Rightarrow \text{Width} = \Delta t_n$$

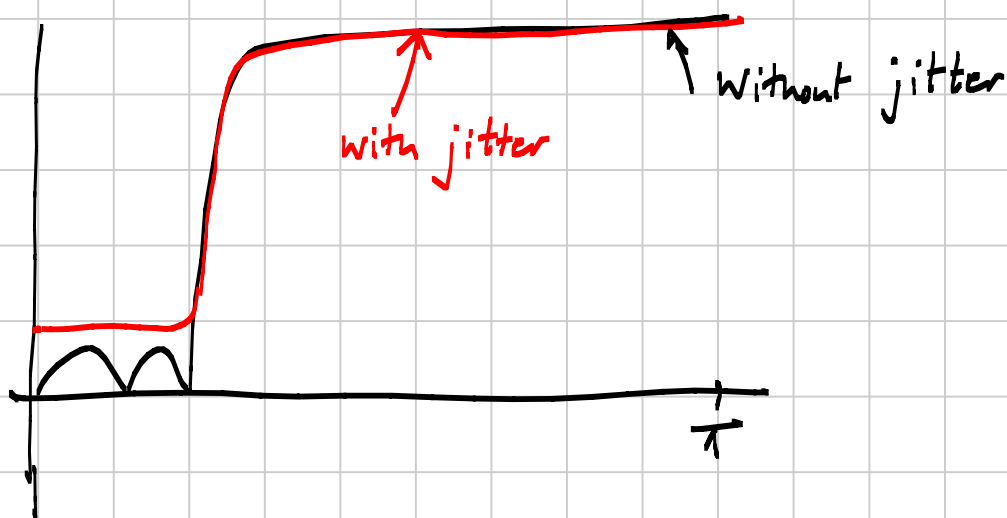
$$\text{Height} = v[n] - v[n-1]$$





Error in the output sequence

$$\Rightarrow \frac{\Delta t_n}{T_s} (V[n] - V[n-1])$$

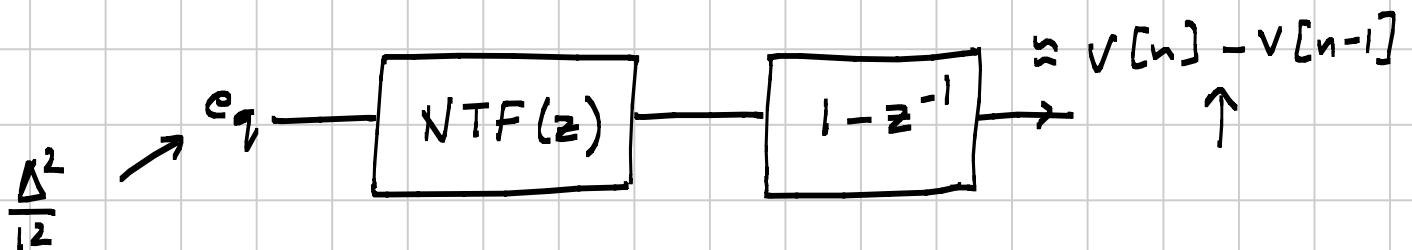


VLSI Data Conversion Circuits : Lecture 35

$$e_j = \frac{\Delta t_n}{T_s} (v[n] - v[n-1]) \Rightarrow \text{white}$$

$$\approx \underbrace{(e_q * h)_n - (e_q * h)_{n-1}}_{\substack{u[n] + (e_q * h)_n \leftarrow v[n] \\ u[n-1] + (e_q * h)_{n-1} \leftarrow v[n-1]}}$$

First difference of the shaped quantization noise



$$\overline{e_j^2} = \frac{\sigma_{\Delta t}^2}{T_s^2} \left[\frac{\Delta^2}{12} \frac{1}{\pi} \int_0^\pi |NTF(e^{j\omega}) (1 - e^{-j\omega})|^2 d\omega \right]$$

$$\text{In band noise power} = \frac{\sigma_{\Delta t}^2}{T_s^2} \frac{\Delta^2}{12\pi \text{DSR}}$$

* High Δ (Poor quantizer resolution) is detrimental to inband SNR (due to jitter)

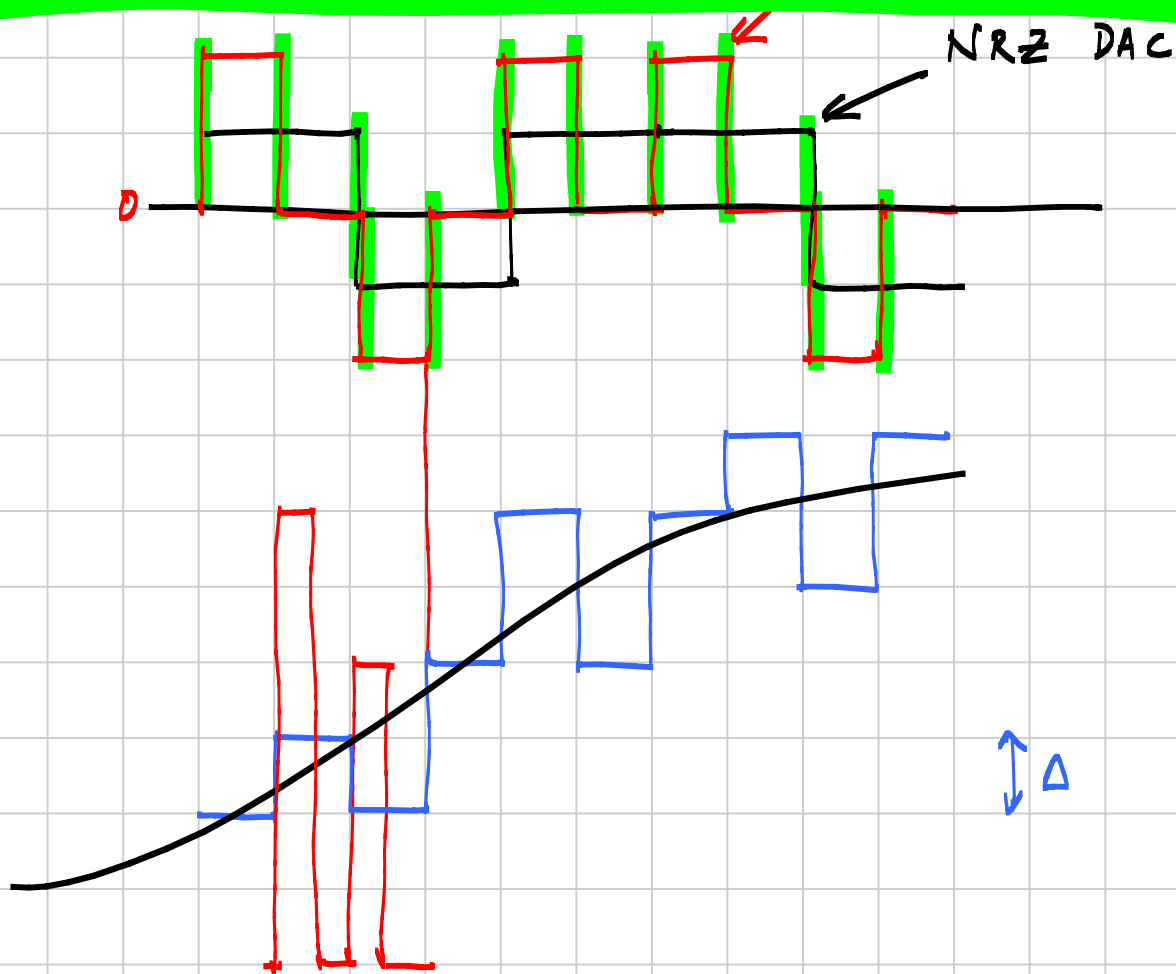
* Aggressive NTF_z will result in more jitter noise.

* Influence of DAC pulse shape

Eg: Single bit modulator

1 -1 1 1 -1

Jitter performance with an RZ DAC is significantly worse!
RZ DAC



$$V_0 \int_0^{\infty} e^{-t/\tau} dt = T$$

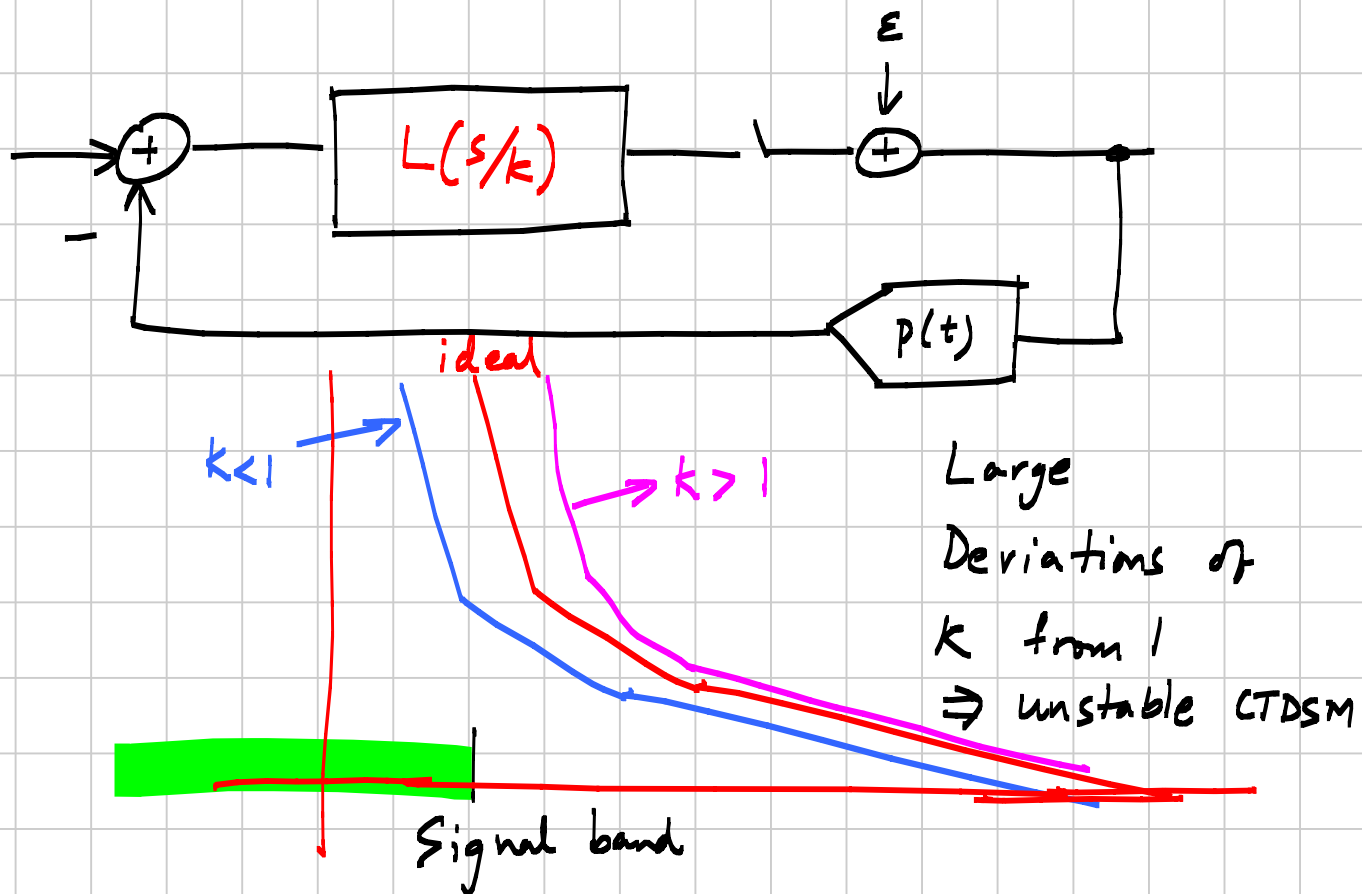
$$\text{if } \tau \ll T,$$

$$V_0 \tau = T \Rightarrow V_0 = T/\tau$$

4f $T \ll T_c$, using an exponentially decaying DAC pulse reduces sensitivity to clock jitter.

→ Switched Capacitor Resistor DAC (SCR)

Loop filter time constant variations

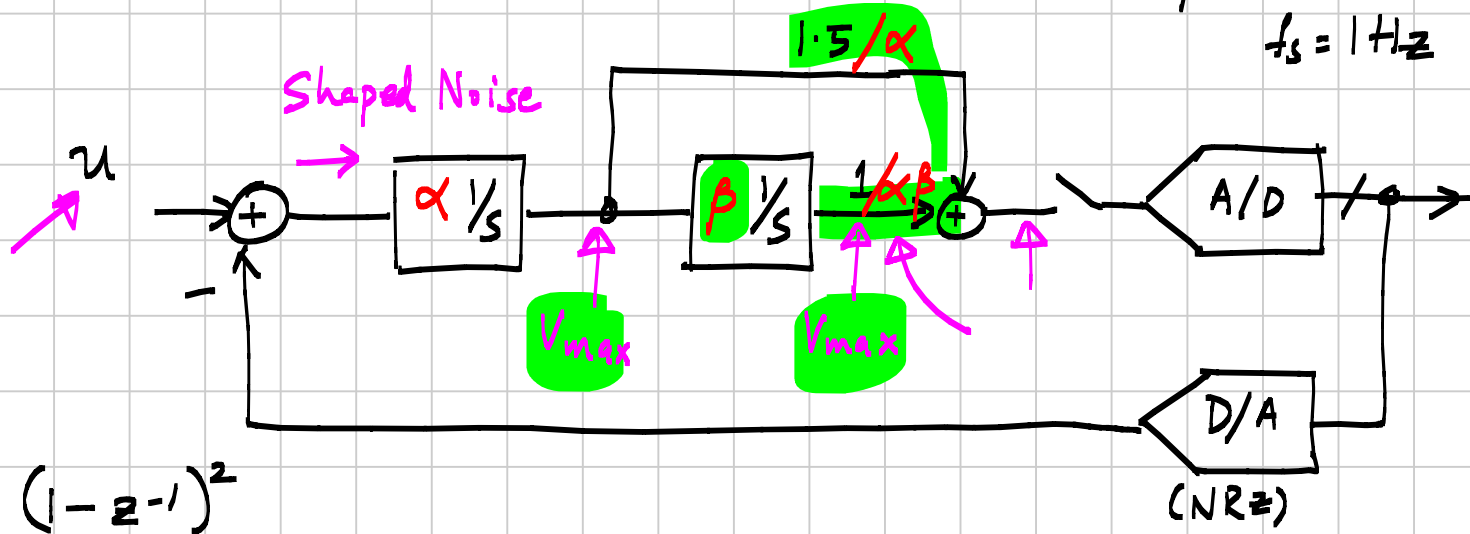


VLSI Data Conversion Circuits: Lecture 36

Note Title

11-03-2011

- * Excess loop delay
- * Clock jitter
- * Time constant variations in the loop filter $f_s = 1 \text{ Hz}$



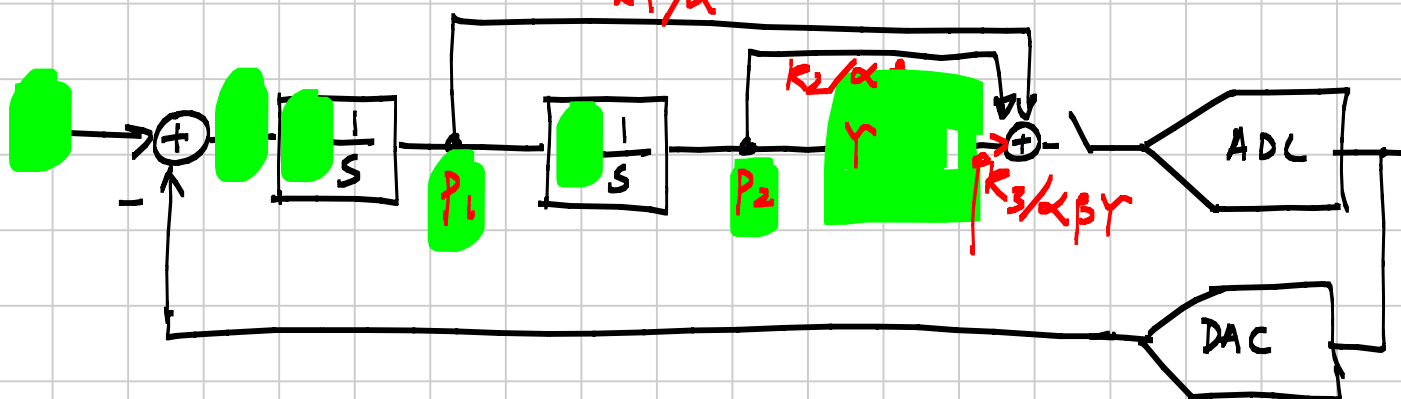
α, β too small $\rightarrow$ summation is difficult
 α, β too large $\rightarrow$ integrators saturate

$\Rightarrow$ Choose α & β so that the peak voltages @ integrator outputs are a little less than V_{max} .

$$\alpha = 1, \beta = 1 \Rightarrow P_1, P_2$$

$$\Rightarrow \alpha = \frac{V_{max}}{P_1}, \beta = \frac{V_{max}}{P_2}$$

Dynamic Range Scaling

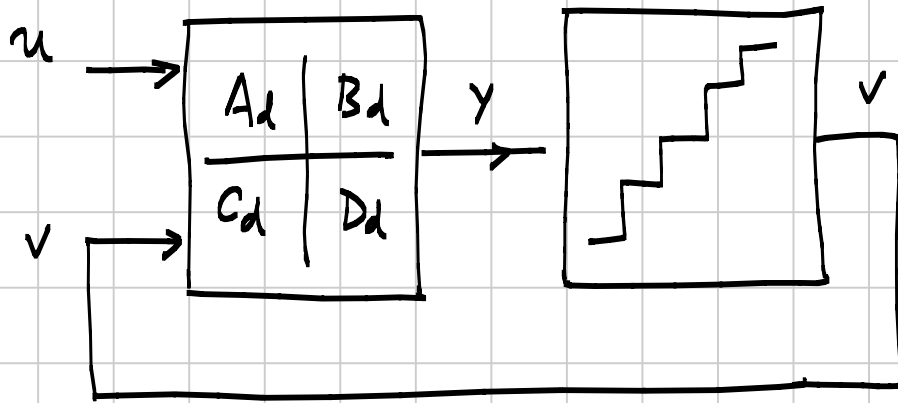


$$\alpha = \frac{0.8 V_{\max}}{P_1}$$

$$\beta = \frac{0.9 V_{\max}}{P_2}$$

$$\gamma = \frac{V_{\max}}{P_3}$$

VLSI Data Conversion Circuits: Lecture 37



$$x[n+1] = A_d x[n] + B_d \begin{bmatrix} u \\ v \end{bmatrix}$$

$$y[n] = C_d x[n] + D_d \begin{bmatrix} u \\ v \end{bmatrix}$$

$$A_d = \begin{matrix} n & \times & n \end{matrix}$$

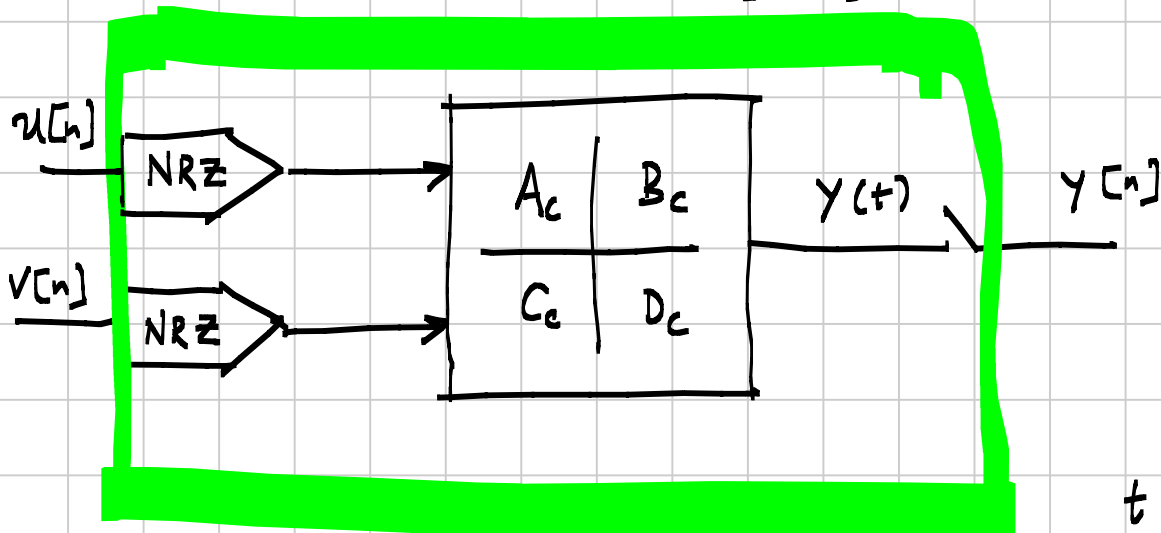
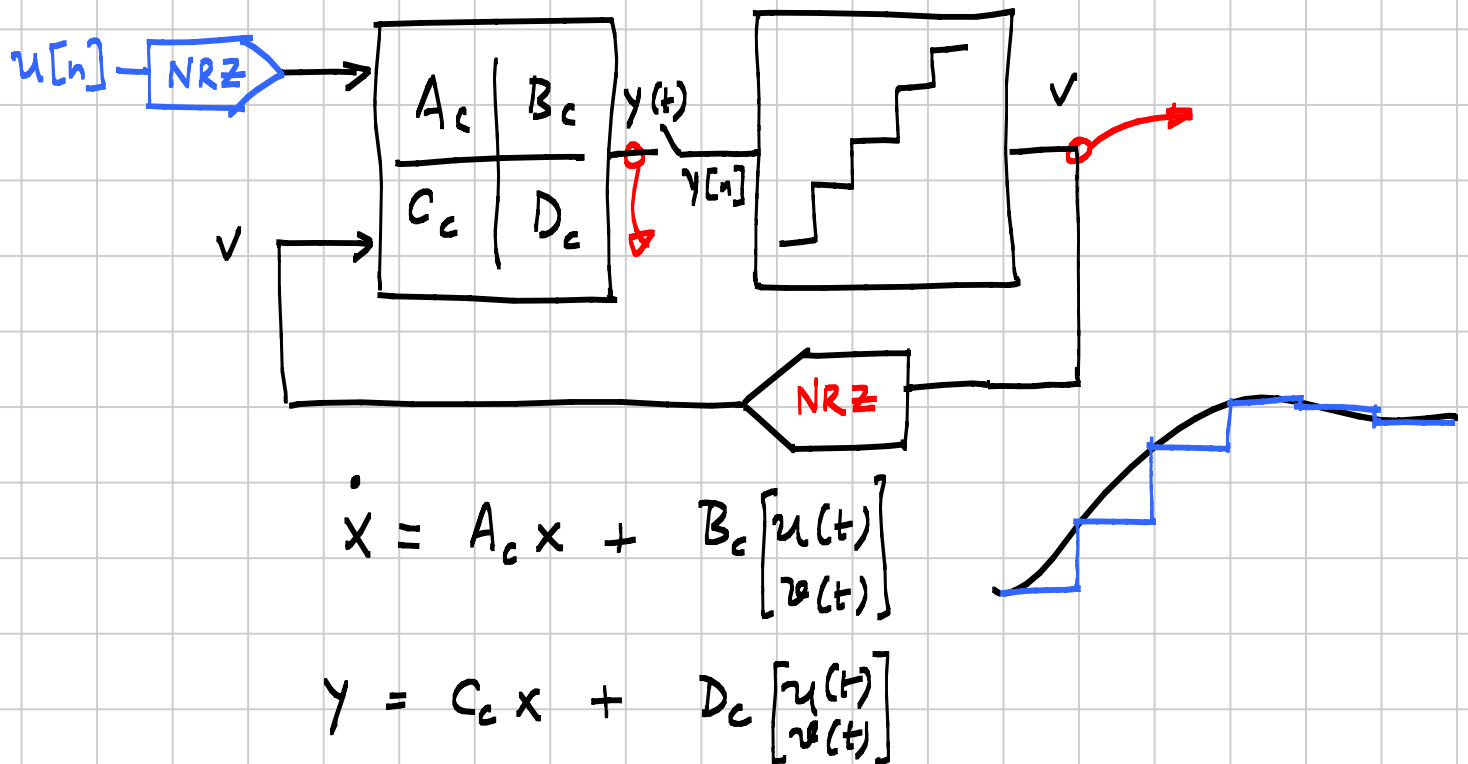
$$B_d = \begin{matrix} n & \times & 2 \end{matrix}$$

$$C_d = \begin{matrix} 1 & \times & n \end{matrix}$$

$$D_d = \begin{matrix} 1 & \times & 2 \end{matrix}$$

$$\left. \begin{array}{c|c} A_d & B_d \\ \hline C_d & D_d \end{array} \right\} \begin{matrix} n+2 \\ n+1 \end{matrix}$$

ABCD_d



$$\dot{x} = A_c x + B_c \begin{bmatrix} u(t) \\ v(t) \end{bmatrix} \quad y(t) = \int_0^t h(t-\tau) u(\tau) d\tau$$

$n \Rightarrow x[n] \quad n+1 ?$

$$x[n+1] = e^{A_c} x[n] + \int_0^1 e^{A_c(1-\tau)} B_c \begin{bmatrix} u(\tau) \\ v(\tau) \end{bmatrix} d\tau$$

$u[n] \quad \int_0^1 e^{A_c(1-\tau)} B_{c1} d\tau$

$B_c = [B_{c1} \ B_{c2}]$

$$+ v[n] \int_0^1 e^{A_c(1-\tau)} B_{c2} d\tau$$

$$v[n] e^{A_c} e^{-A_c \tau} B_{c2} d\tau$$

$$v[n] e^{A_c} (-A_c^{-1}) e^{-A_c \tau} B_{c2} \Big|_0^1$$

$$= v[n] e^{A_c} A_c^{-1} [I - e^{-A_c}] B_{c2}$$

$$= A_c^{-1} (e^{A_c} - I) B_{c2} v[n]$$

$$x[n+1] = e^{A_c} x[n] + A_c^{-1} (e^{A_c} - I) B_c \begin{bmatrix} u[n] \\ v[n] \end{bmatrix}$$

$$y[n] = C_c x[n] + D_c \begin{bmatrix} u[n] \\ v[n] \end{bmatrix}$$

$$x[n+1] = A_d x[n] + B_d \begin{bmatrix} u \\ v \end{bmatrix}$$

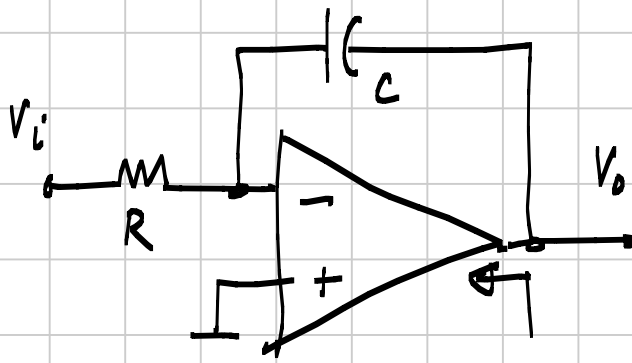
$$y[n] = C_d x[n] + D_d \begin{bmatrix} u \\ v \end{bmatrix}$$

$$\rightarrow A_d \rightarrow e^{A_c}$$

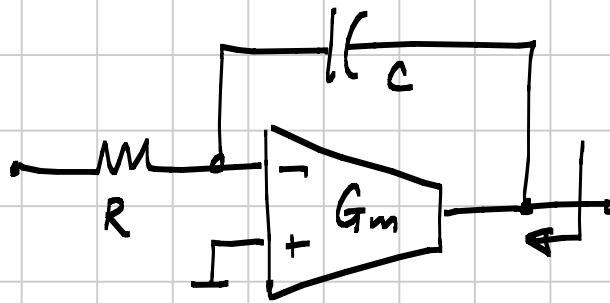
$$\rightarrow B_d \rightarrow A_c^{-1} (A_d - I) B_c$$

$$\rightarrow C_d, D_d \rightarrow C_c, D_c$$

→



$$\frac{V_o}{V_i} = -\frac{1}{sCR}$$



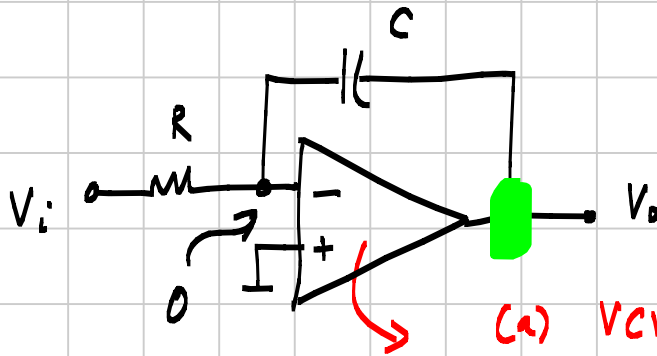
$$G_m \rightarrow \infty$$

OTA
Operational
Transconductance
Amplifier

VLSI Data Conversion Circuits : Lecture 38

Note Title

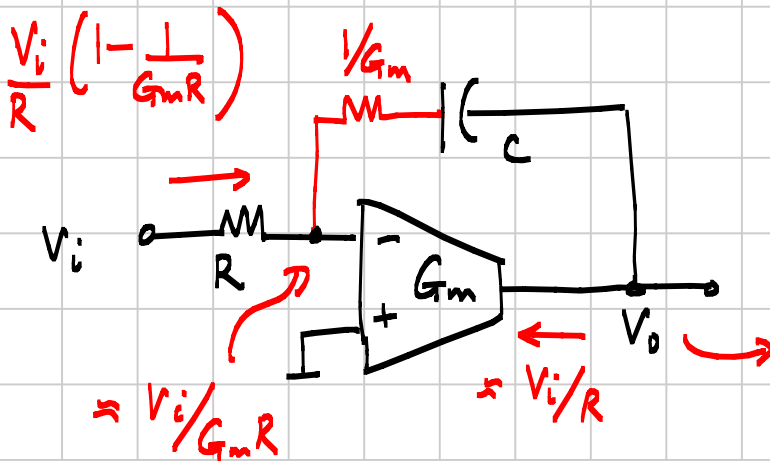
12-03-2011



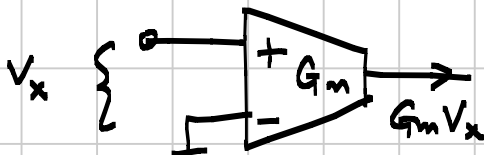
$$\frac{V_o}{V_i} = -\frac{1}{sCR}$$

- (a) VCVS with gain A , $A \rightarrow \infty$
 (b) VCCS with trans. G_m , $G_m \rightarrow \infty$

OTA $\rightarrow$ Operational Transconductance Amplifier



$$\frac{V_i}{G_m R} - \frac{V_i (1 - \frac{1}{G_m R})}{sCR}$$



$$-\frac{V_i}{sCR} + \frac{V_i}{sCR} \cdot \frac{1}{G_m R} + \frac{V_i}{G_m R}$$

$$= \frac{-V_i \alpha}{sCR} + \frac{V_i sCR / G_m R}{sCR}$$

$$= \frac{-V_i \alpha}{sCR} \left(1 - \frac{sC}{\alpha G_m} \right)$$

Ideal: $-\frac{V_i}{sCR}$

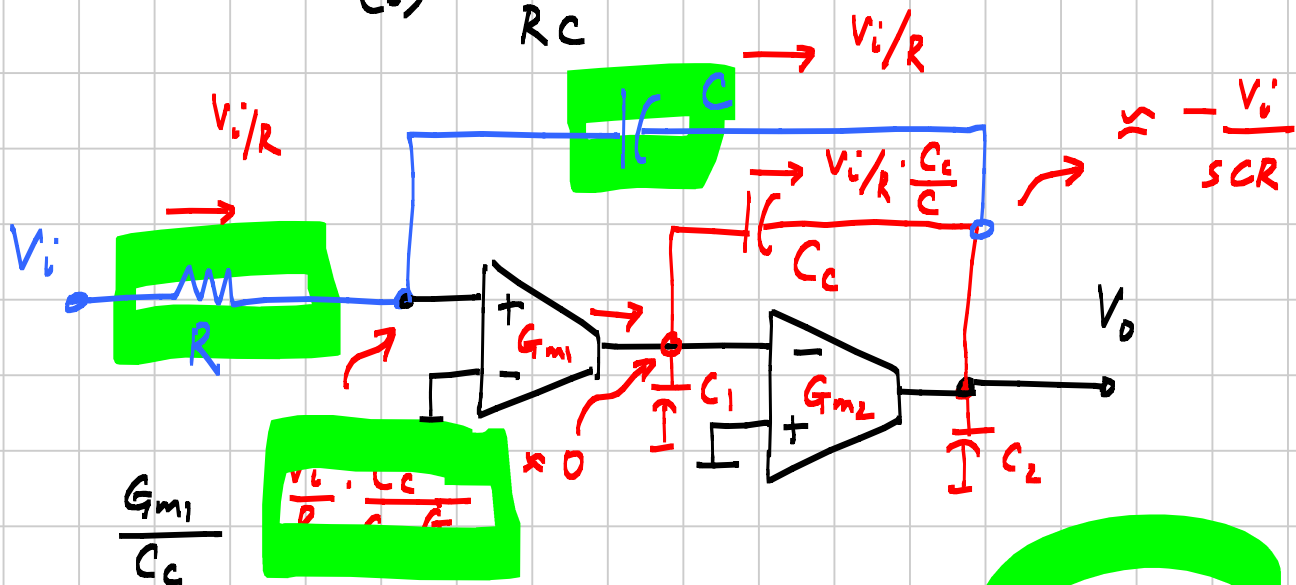
Actual: $-\frac{V_i \alpha}{sCR} \left(1 - \frac{sC}{\alpha G_m} \right)$

$$\alpha = 1 - \frac{1}{G_m R}$$

Finite G_m causes an apparent reduction of the unity gain frequency of the integrator.

fixes $\rightarrow$ (a) Increase G_m

(b) $\frac{\alpha}{RC} \Rightarrow \hat{C} = \alpha C$

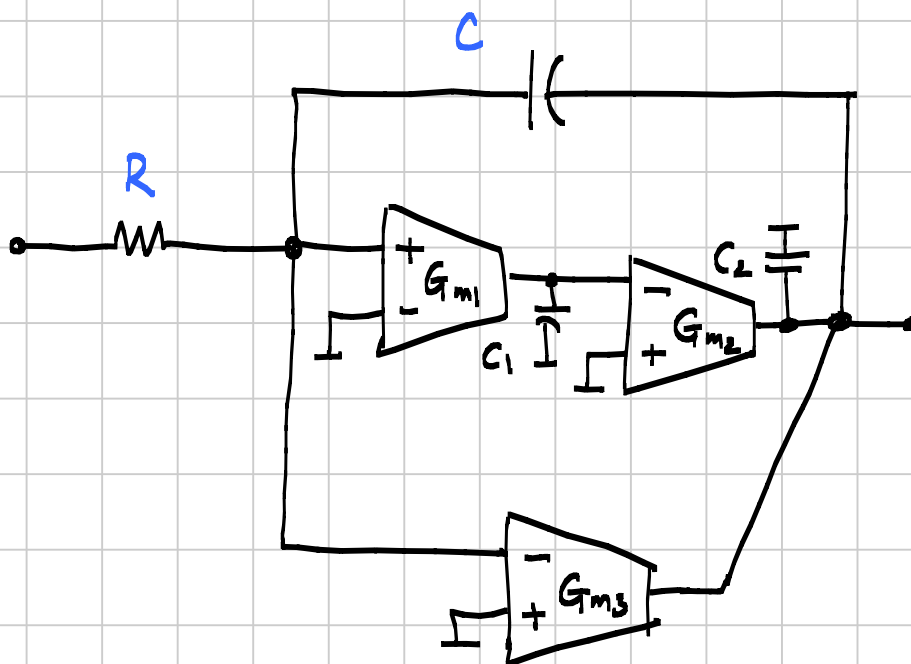


$G_{m2} \rightarrow$ large
for better
phase margin

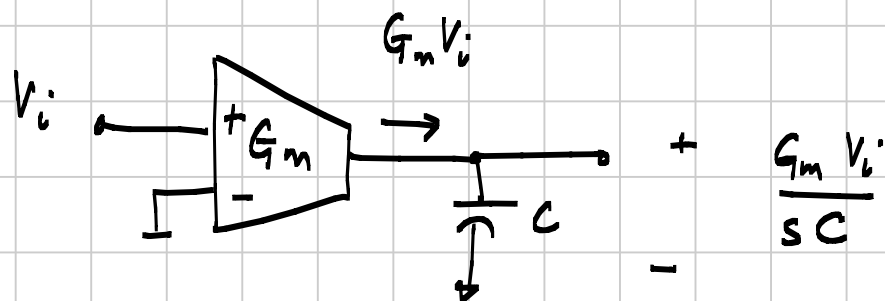
Virt. gnd voltage $\approx$

$$\frac{V_i}{G_{m1} R} \cdot \frac{C_c}{C}$$

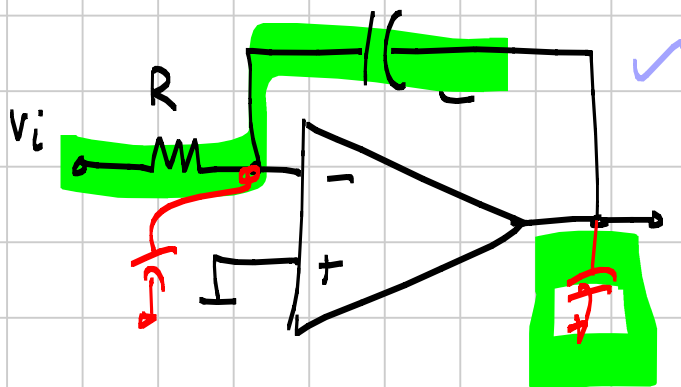
factor of
improvement
over a single
stage design



Feedforward
Compensation



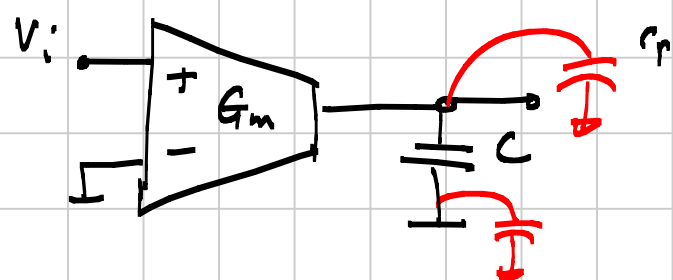
Transconductance Capacitance
($G_m - C$) integrator.



$$\omega_n = 1/RC$$

Stray insensitive

Lower Speed

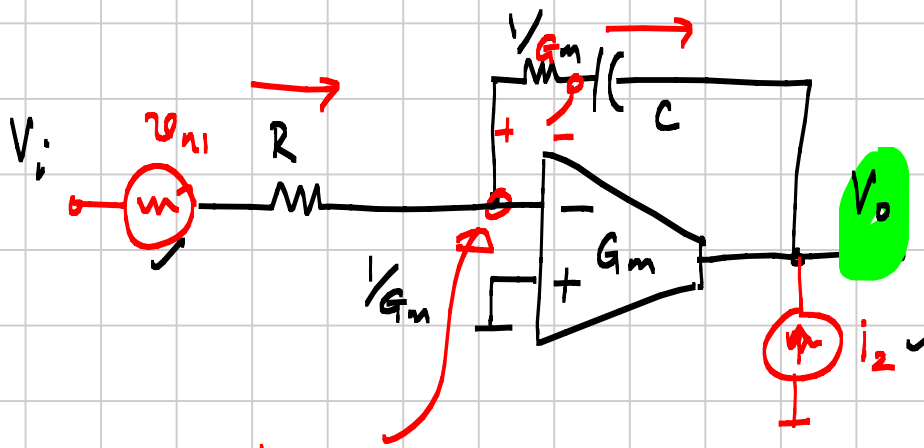


$$\omega_o = \frac{G_m}{C}$$

Stray sensitive

High Speed

VLSI Data Conversion Circuits : Lecture 39



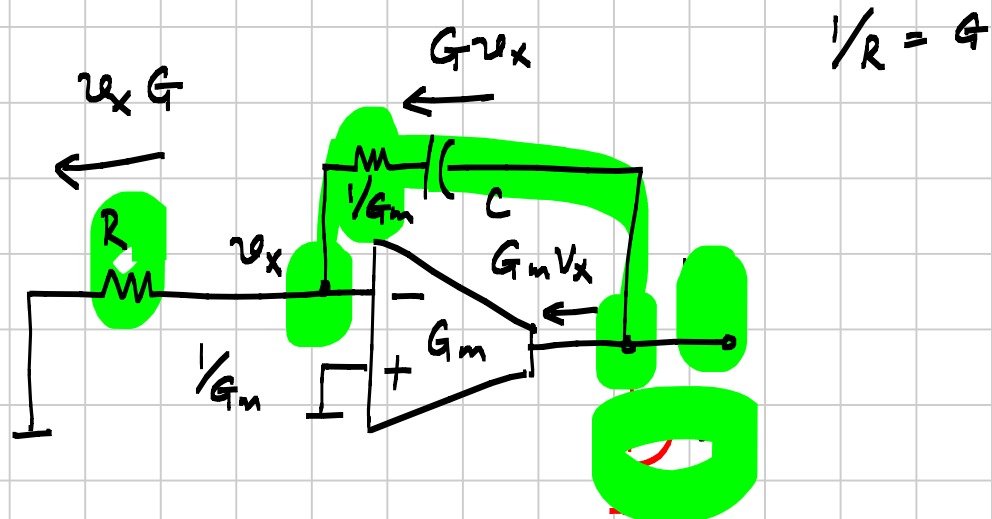
$$S_{V_1} = 4kTR$$

$$S_{I_2} = 4kT G_m$$

$$V_o = - \frac{V_i}{R} \cdot \frac{G_m R}{1 + G_m R} \cdot \frac{1}{sC}$$

$$\frac{V_o}{V_i} = - \frac{1}{sCR} \cdot \frac{G_m R}{1 + G_m R} \rightarrow H_1$$

Noise @ o/p due to $v_{n1} \Rightarrow 4kTR \cdot |H_1(f)|^2$



$$i_{n2} = (G + G_m) V_x$$

$$V_x = \frac{V_o \cdot R}{R + \frac{1}{sC} + \frac{1}{G_m}}$$

$$\Rightarrow i_{n2} = \frac{(G + G_m) R V_o}{R + \frac{1}{sC} + \frac{1}{G_m}}$$

$$S_{v_o}(f) = \left| \frac{R + \frac{1}{j2\pi f C} + \frac{1}{G_m}}{(G + G_m)R} \right|^2 4kT G_m \eta$$

$$= \left| \frac{\frac{G_m R + 1}{G_m} + \frac{1}{j2\pi f C}}{1 + G_m R} \right|^2 4kT G_m \eta$$

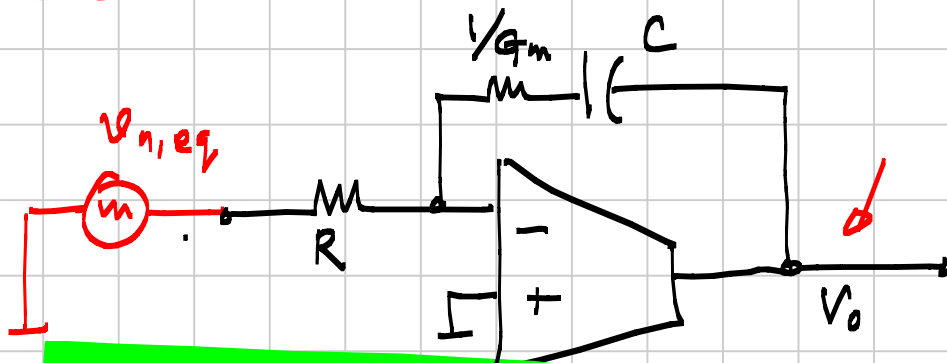
$$G_m R \gg 1$$

$$\approx \left| \frac{R + \frac{1}{j2\pi f C}}{G_m R} \right|^2 4kT G_m \eta$$

$$\approx \left| \frac{1}{G_m} + \frac{1}{j2\pi f R C G_m} \right|^2 4kT G_m \eta$$

Total O/P Noise =

$$\underbrace{\left| \frac{1}{G_m} + \frac{1}{j2\pi f R C G_m} \right|^2 4kT \eta G_m}_{\text{Due to DTA}} + \underbrace{\left| \frac{1}{j2\pi f R C} \frac{G_m R}{1 + G_m R} \right|^2 4kT R}_{\text{Due to R}}$$



$$S_{v_{o,eq}}(f)$$

$$\left| \frac{1}{j2\pi f R C} \frac{G_m R}{1 + G_m R} \right|^2 4kT R$$

$$S_{v,eq}(f) = 4kTR +$$

$$\frac{\left| \frac{1}{G_m} + \frac{1}{j2\pi fRC G_m} \right|^2 4kT\eta G_m}{\left| \frac{1}{j2\pi fRC} \right|^2}$$

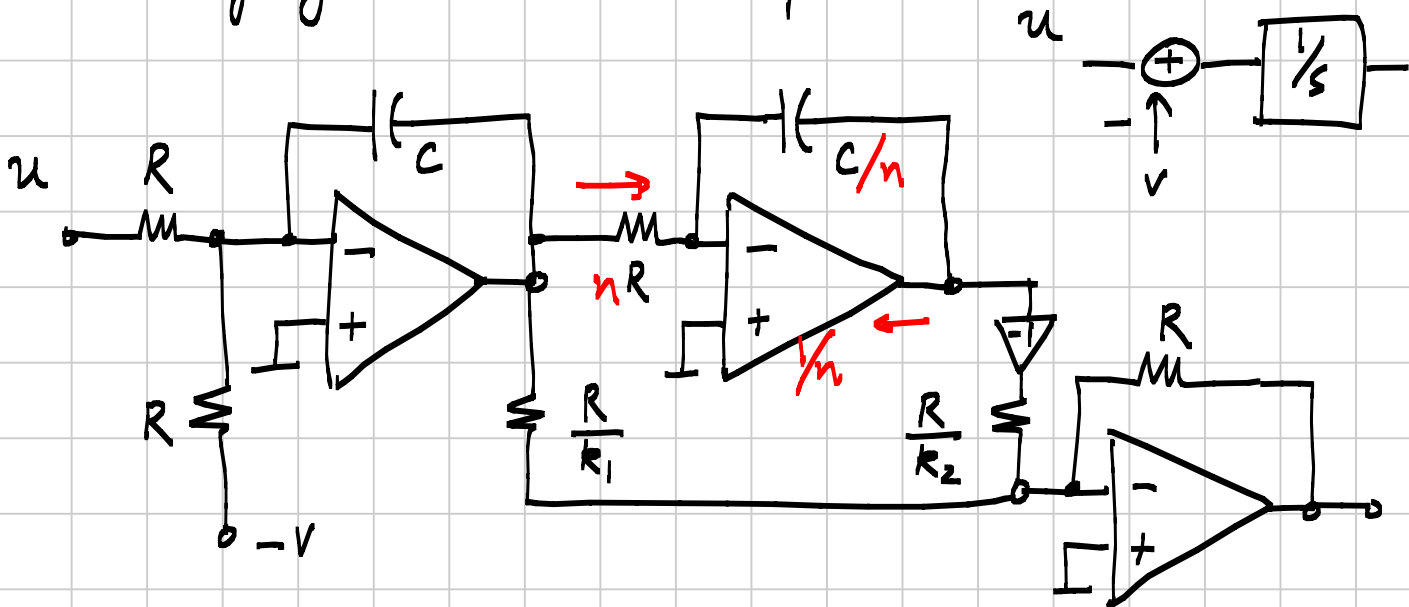
$$\approx 4kTR + 4kT\eta G_m \left\{ \left| \frac{1}{G_m} + \frac{j2\pi fRC}{G_m} \right| \right\}^2$$

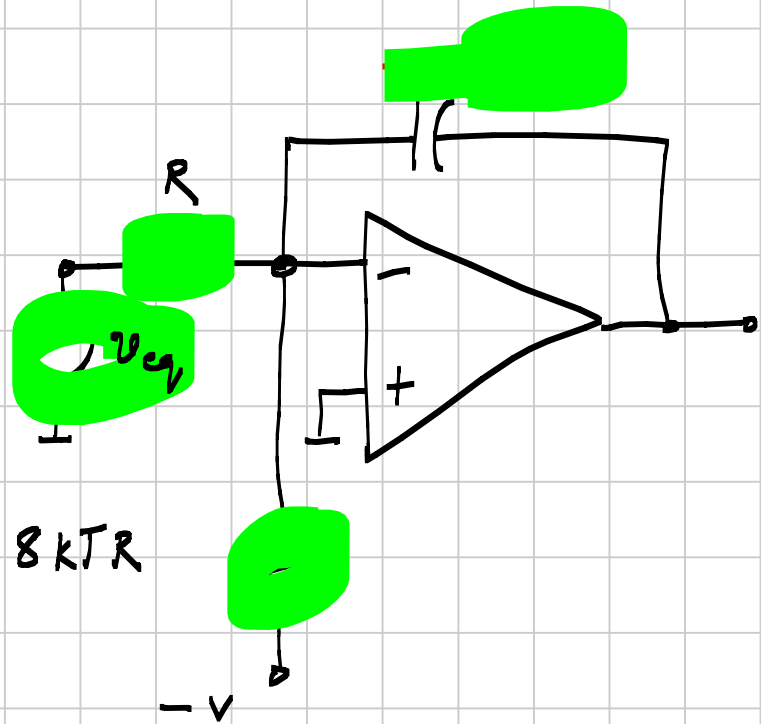
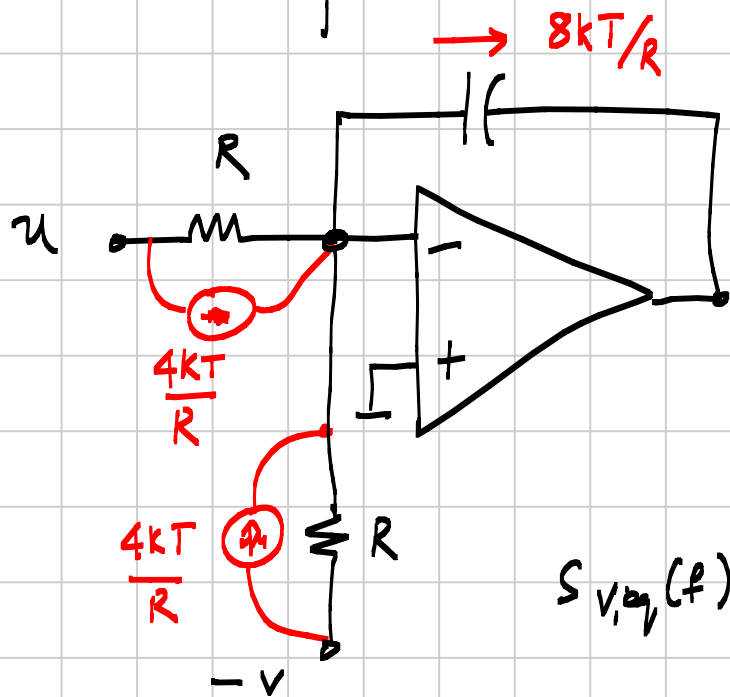
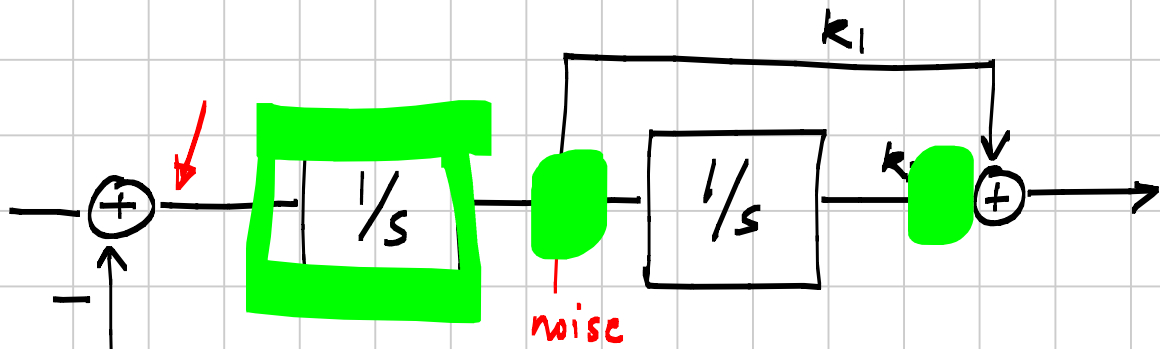
$$\approx 4kTR + 4kT\eta \frac{1}{G_m} \left\{ \left| 1 + j \right| \right\}^2$$

② Low frequencies, spectral density is

$$\approx 4kTR + 4kT\eta \frac{1}{G_m}$$

Since $G_m R \gg 1$, input referred noise is largely due to the input resistor.





$$S_{V_{eq}}(f) = 8kTR$$

* The first integrator's input referred noise $\approx$ the i/p referred noise of the modulator

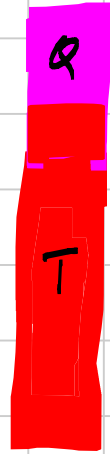
TOTAL Noise = Thermal Noise + Inband shaped Q. Noise

$$\text{Peak SNR} = \frac{MSA^2}{2 \left[\underbrace{8kTR \cdot BW}_{\text{Thermal Noise}} + \underbrace{\text{Inband Q. Noise}}_{\text{Quantization Noise}} \right]}$$

Doubling power in the first integrator

$\Rightarrow$ Thermal noise $\downarrow 2$
power

Total
Noise



* Modulator input noise dominated by
thermal noise

Choose thermal noise $\approx \underline{15-20 \text{ dB}} > Q \cdot \text{Noise}$

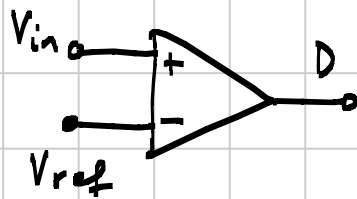
VLSI Data Conversion Circuits : Lecture 40

Note Title

19-03-2011

ADC : Must be low latency

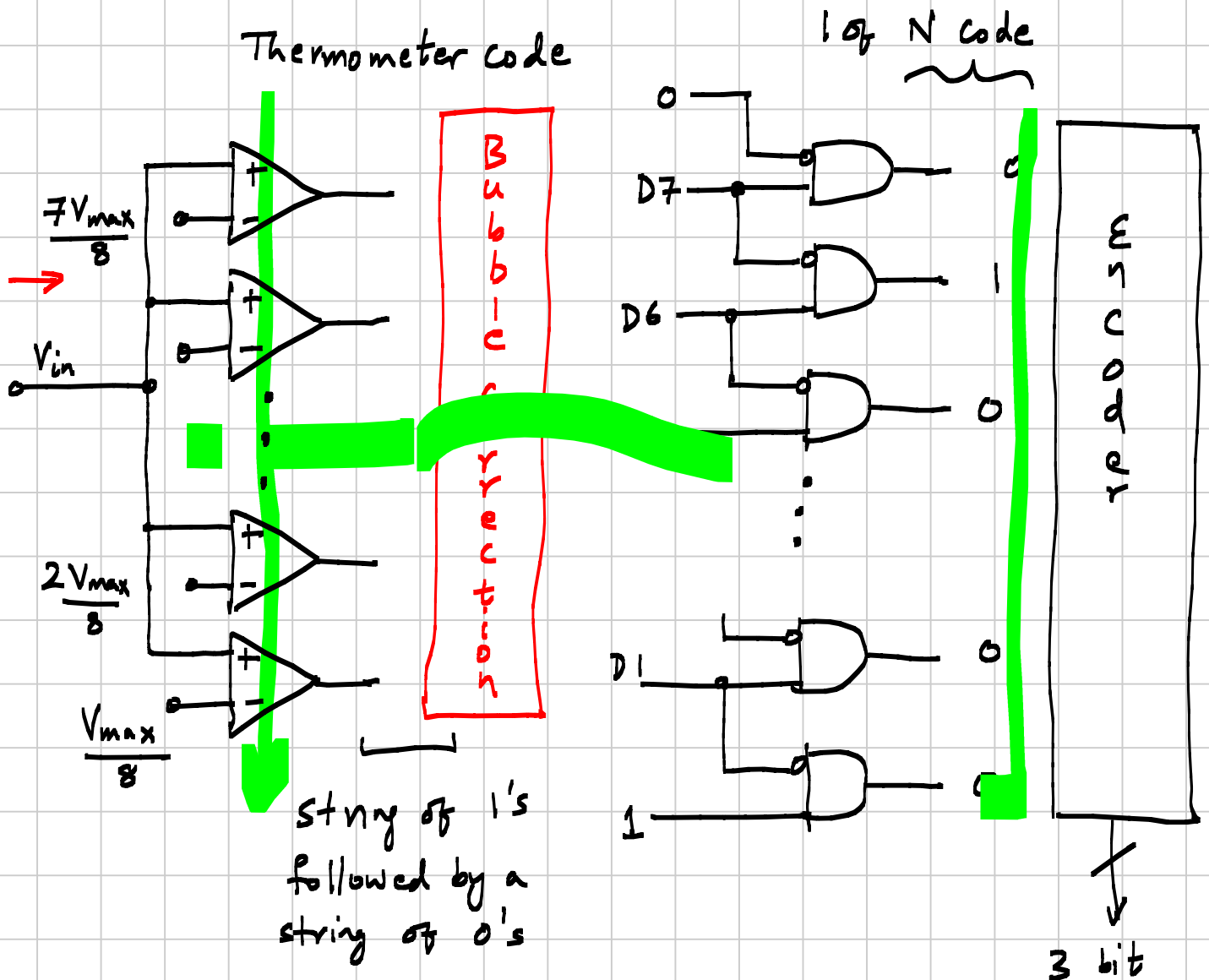
→ Flash A/D Converters



$D = \text{logical } 1 \text{ if } V_{in} > V_{ref}$
 $= \text{logical } 0 \text{ if } V_{in} < V_{ref}$

V_{ref} - Threshold of the comparator

Eg: 3 bit flash ADC ($2^3 - 1$ thresholds = comparators)



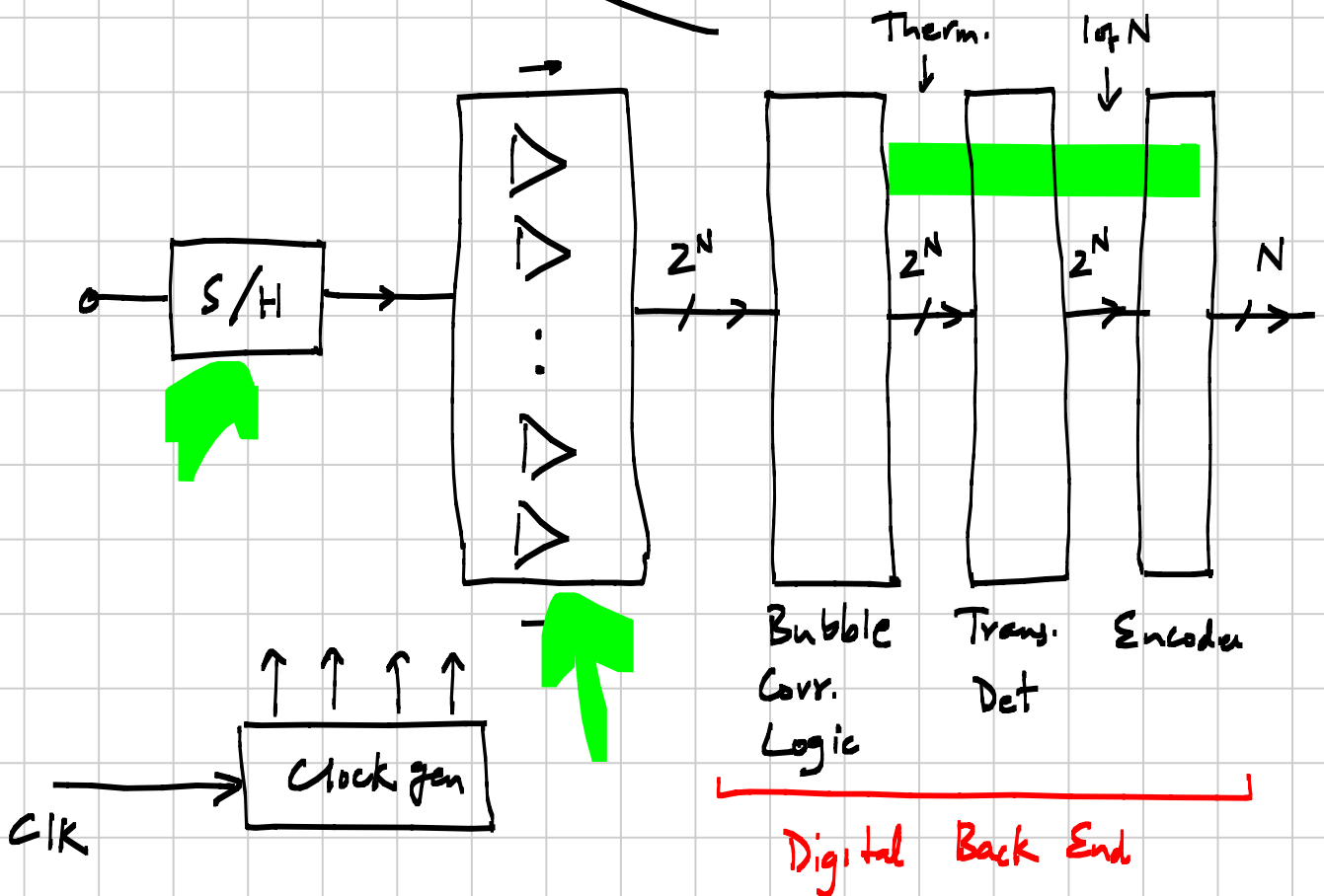
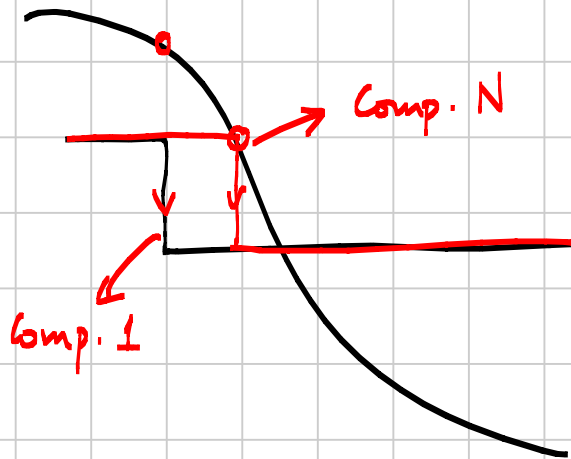
Ideal Thermometer Code

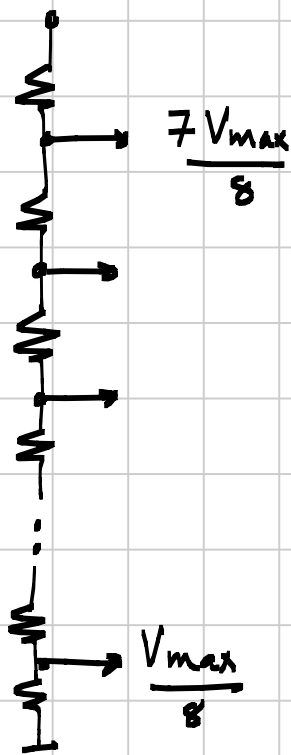
Actual Code due to lack of a S/H, clock skew

"Sparkles"
or
"Bubbles"

0	→	0
0	→	0
1	→	0
0	→	1
1	→	1
1	→	1
1	→	1
1	→	1

Majority of '3'
Corrects 1
bubble



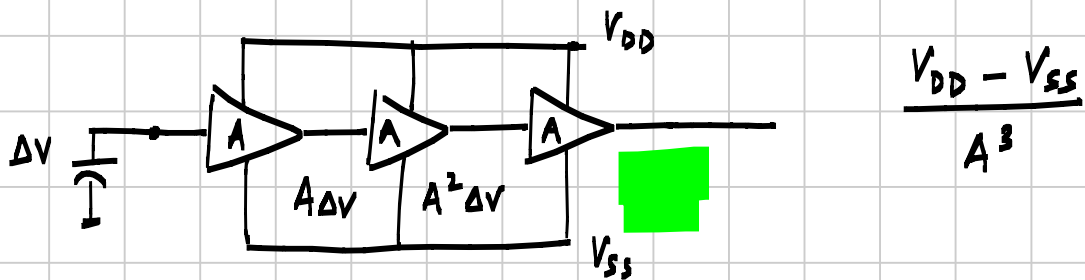


Reference generation

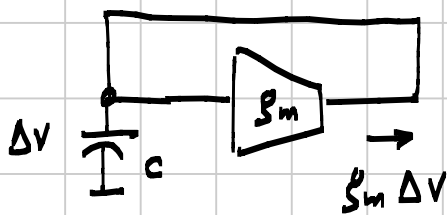
⇒ commonly done using a resistor string

⇒ Process gradients can cause DNL/INL due to resistors not being identical.

VLSI Data Conversion Circuits : Lecture 41



(a) Cascade of amplifiers



$$C \frac{dv}{dt} = g_m v$$

$$v(0) = \Delta V$$

$$v(t) = \Delta V e^{t/\tau} \quad \tau = C/g_m$$

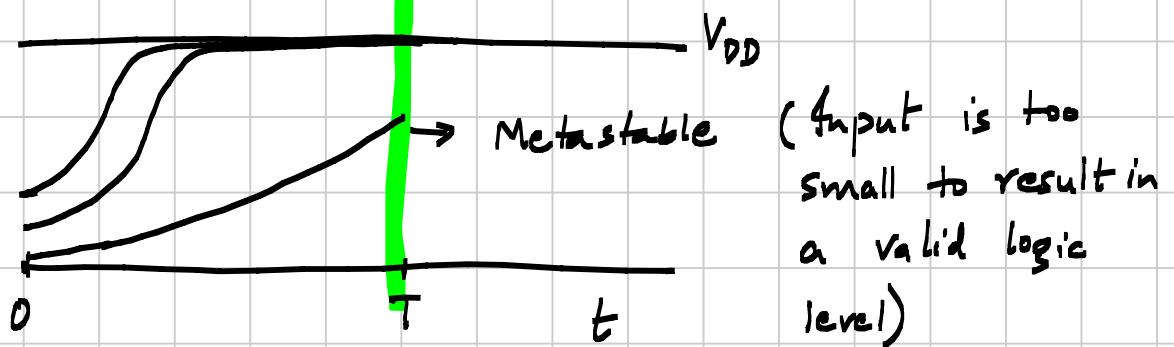
Positive or regenerative feedback.

$\tau = C/g_m \rightarrow$ regenerative time constant.

"Gain" = $\underbrace{e^{t/\tau}} \Rightarrow$ More t , more gain.

$$\text{Min. resolvable input} = \frac{V_{DD}}{e^{T/\tau}}$$

is the time available for comparison



$$\tau = C/g_m \text{ must be made as small as possible}$$

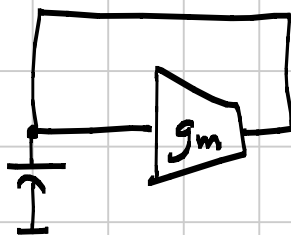
make C as small as possible

⇒ limited by f_T of the MOS transistor

$$\left. \begin{aligned} g_m &= \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) \\ C_{GS} &= C_{ox} W L \end{aligned} \right\} \frac{g_m}{C_{GS}} = \frac{\mu_n (V_{GS} - V_T)}{L^2}$$

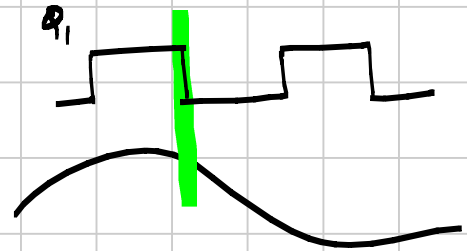
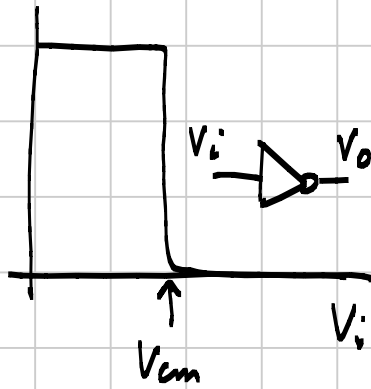
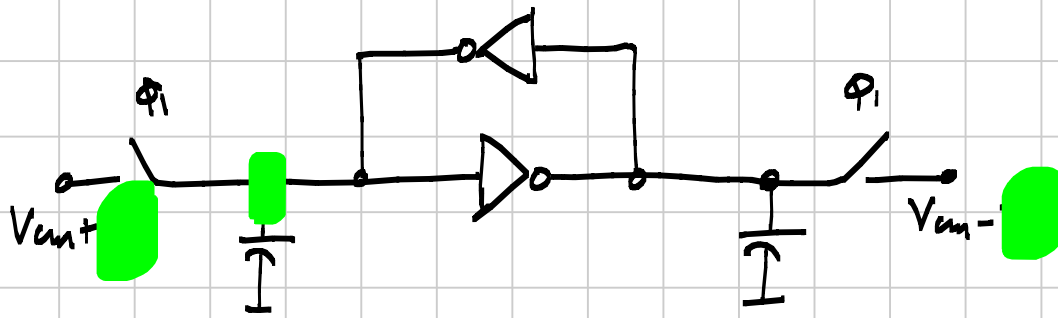
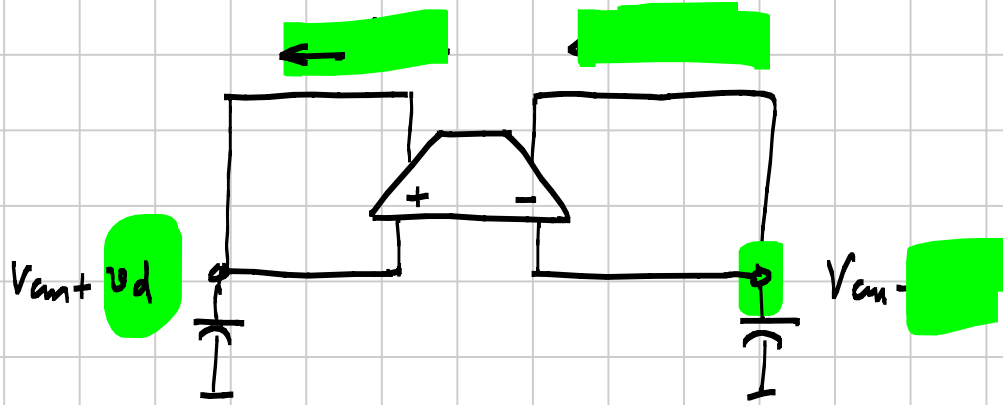
$$\begin{aligned} V_1 & \text{ --- } \\ V_2 & \text{ --- } \end{aligned} \quad \begin{aligned} \frac{V_1 + V_2}{2} + \frac{V_1 - V_2}{2} &= V_{cm} + v_{dm} \\ \frac{V_1 + V_2}{2} - \frac{V_1 - V_2}{2} &= V_{cm} - v_{dm} \end{aligned}$$

$\underbrace{\hspace{1cm}}_{V_{cm}} \quad \underbrace{\hspace{1cm}}_{v_{dm}}$

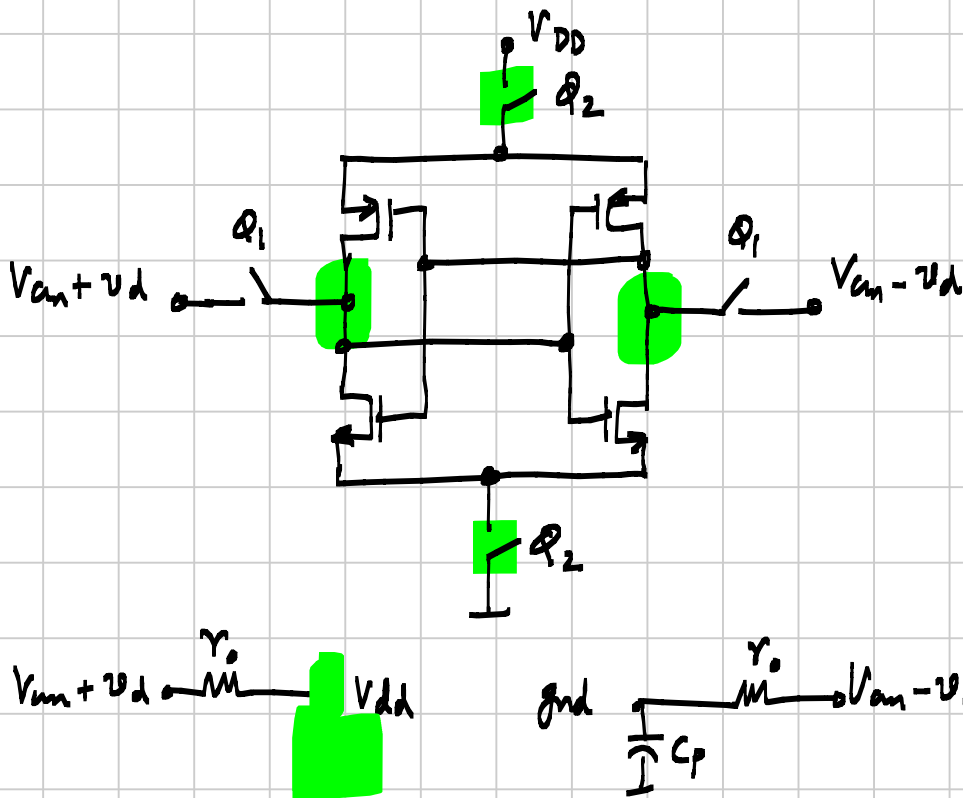


← Single ended comparator

$$\left. \begin{aligned} V_{cm} + v_d \\ V_{cm} - v_d \end{aligned} \right\} \text{ Trying to determine if } v_d > 0 \text{ or } v_d < 0$$



* Latch samples @ the falling edge of ϕ_1



$$\underbrace{(V_{an} + v_d)} + \underbrace{V_{ad} e^{-T/r_i C_p}}$$

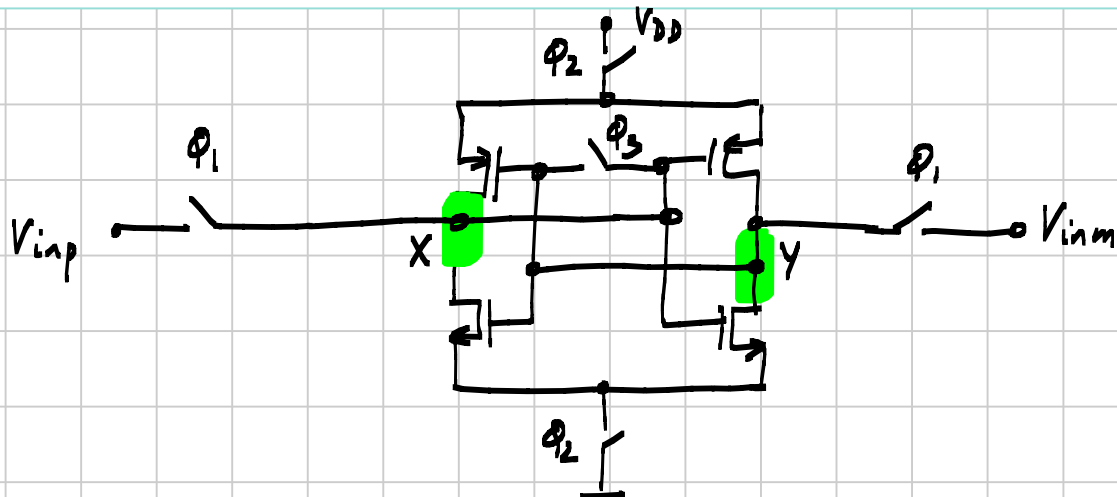
v_d is positive in one cycle,
and just negative in the next

Hysteresis

VLSI Data Conversion Circuits : Lecture 42

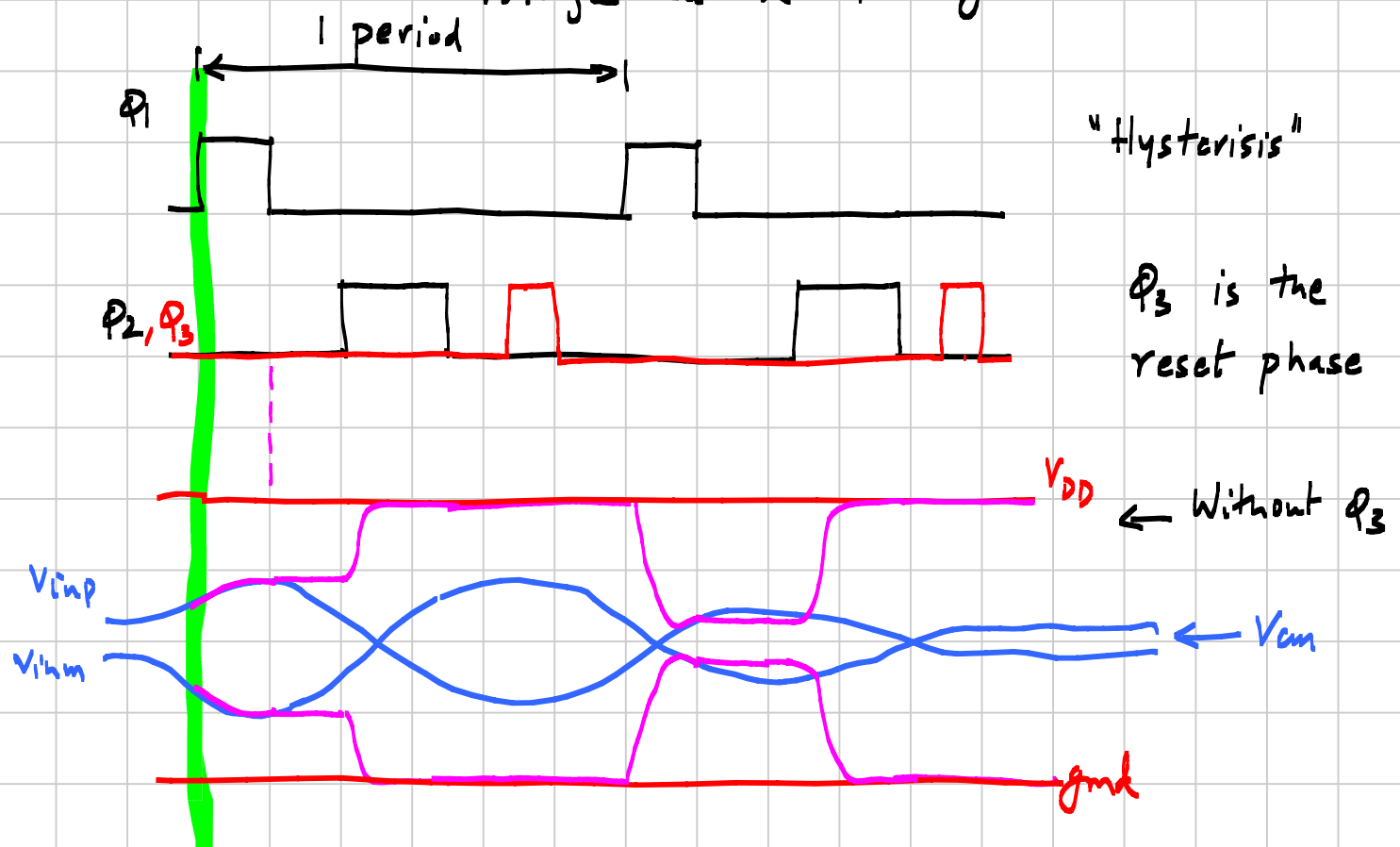
Note Title

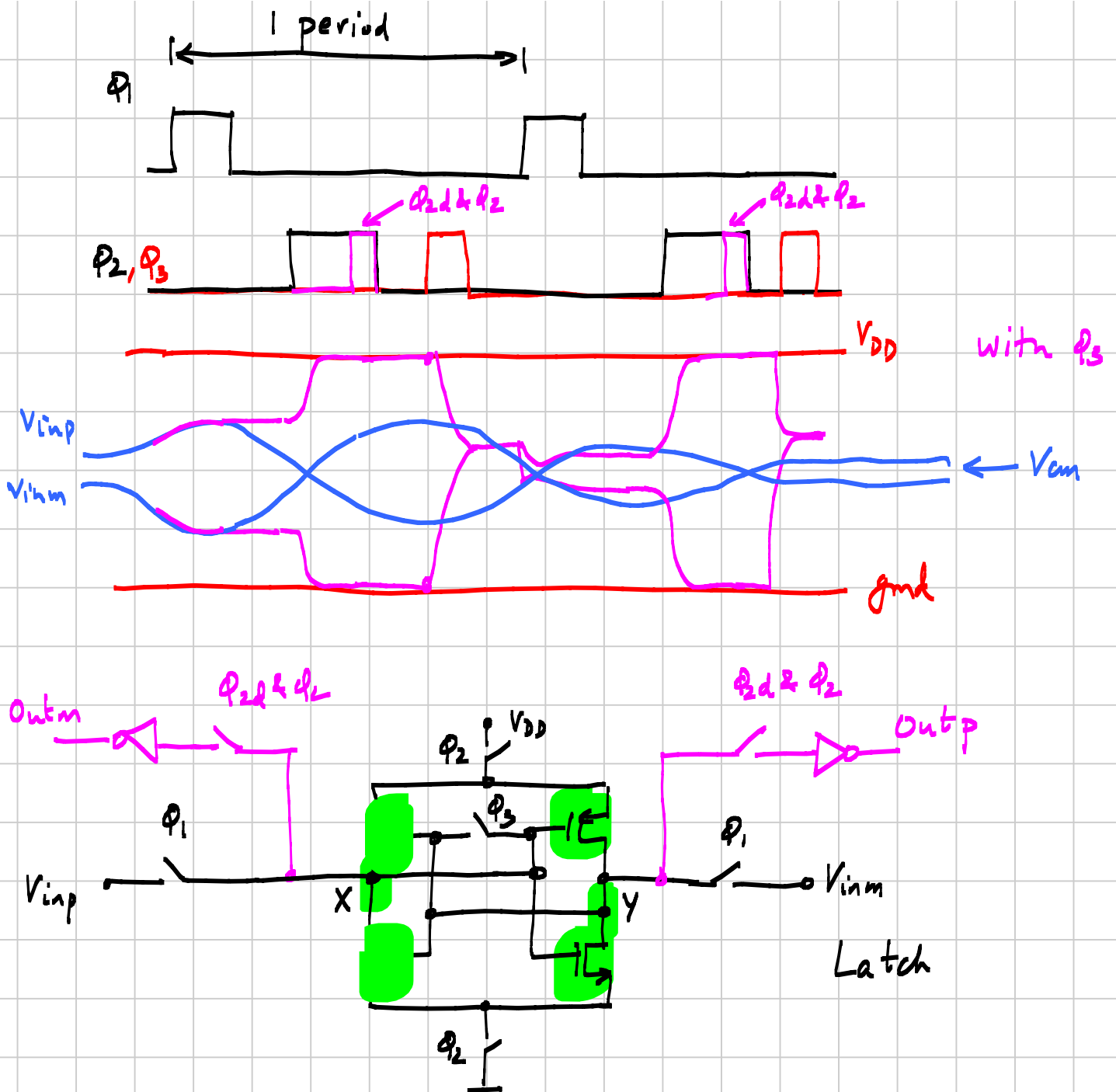
21-03-2011



During $\phi_1 \rightarrow$ Input is sampled across X & Y

During $\phi_2 \rightarrow$ Input is removed,
transconductors are enabled,
voltages at X & Y regenerate





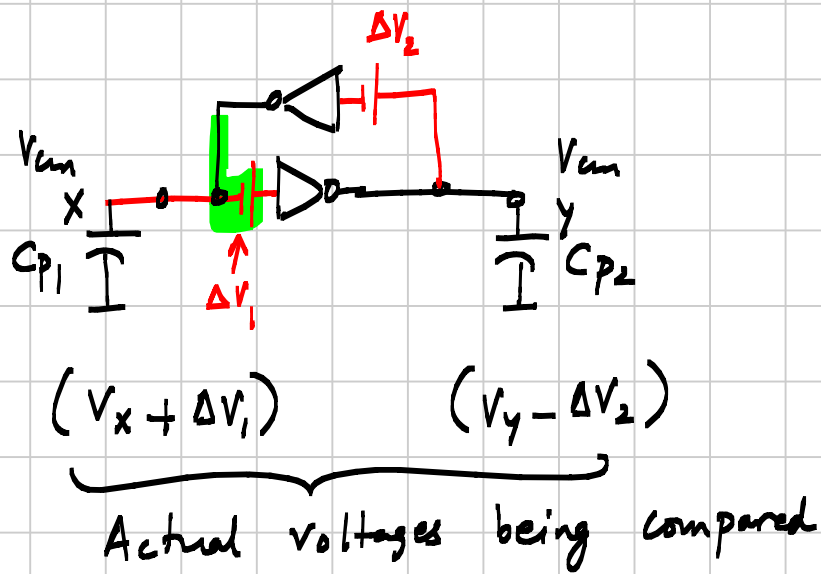
* Nonidealities in Regenerative latches

→ Mismatch in transistors

NMOS & PMOS devices are not exactly identical

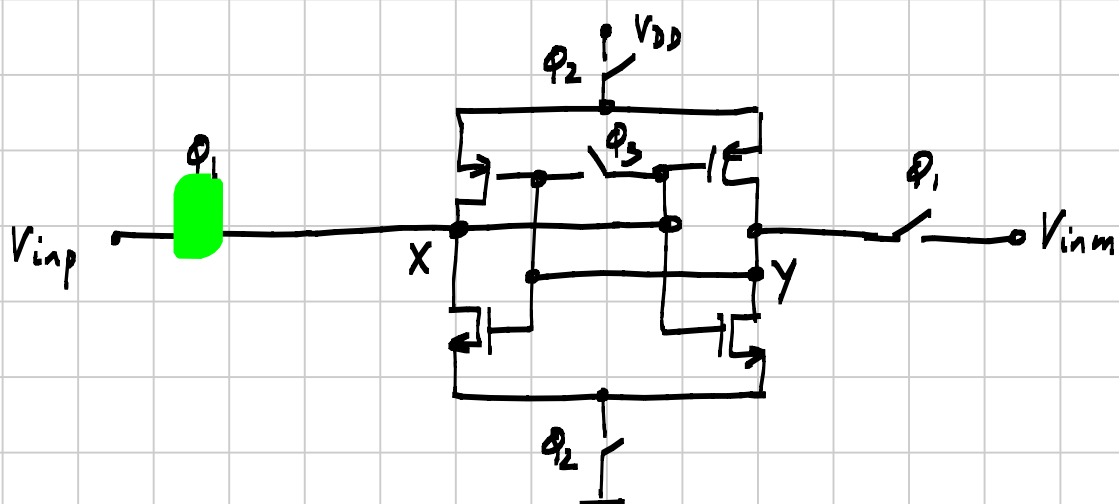
- Thresholds are not the same
- current factor mismatch (β mismatch)

$$\sigma_{V_T} = \frac{A_{V_T}}{\sqrt{WL}} \quad \& \quad \sigma_{\beta/\beta} = \frac{\sigma_{\beta}}{\sqrt{WL}}$$

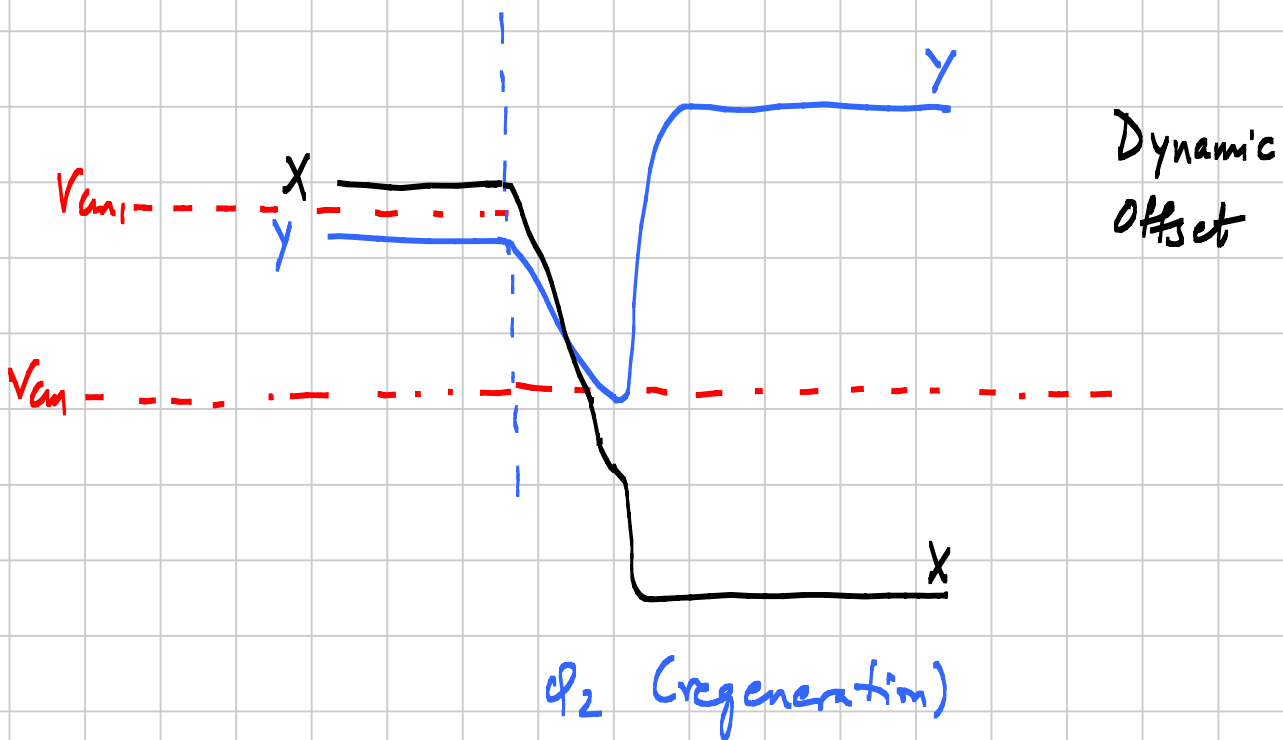
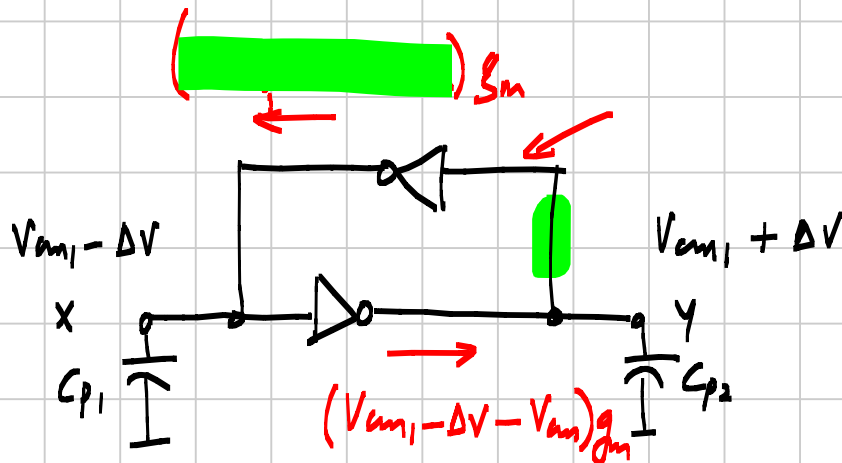


- * Device mismatch causes latch offset
- * Mismatch of C_{p1} & C_{p2} along with switch mismatch result in offset due to charge injection errors.
- * Dynamic mismatch

VLSI Data Conversion Circuits : Lecture 43



$$\boxed{\rightarrow} = V_{cm} \neq V_{cm1}$$

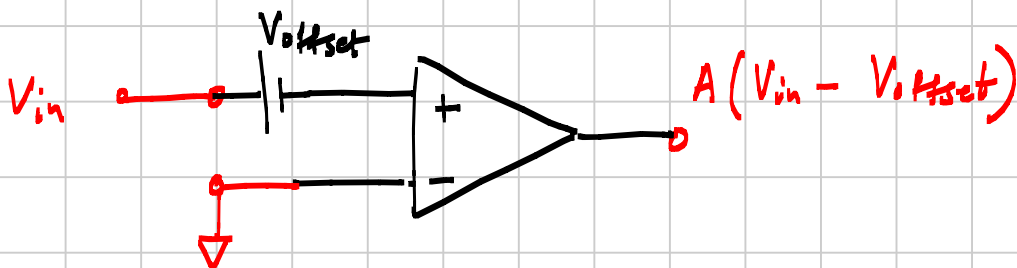
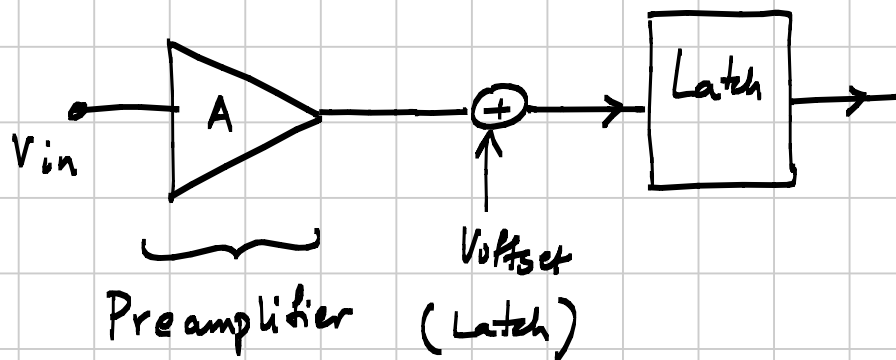
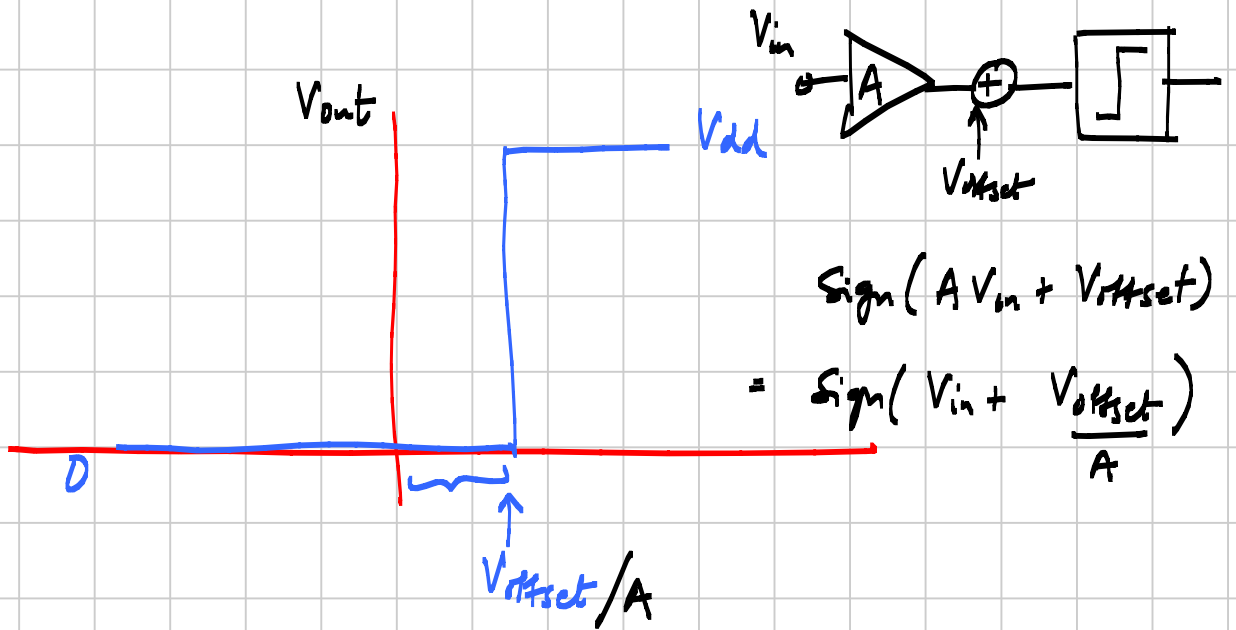
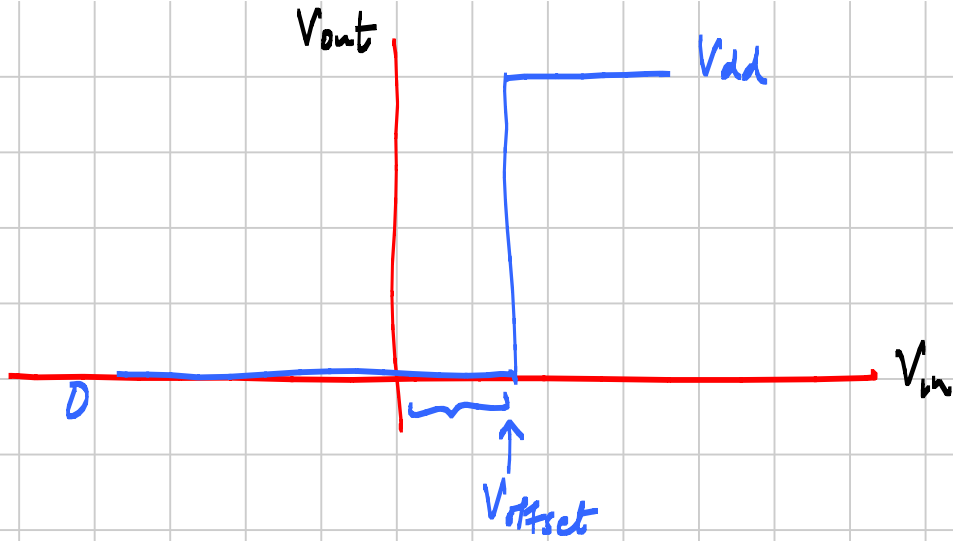


Minimize dynamic offset by choosing $V_{cm1} = V_{cm}$

$\approx 40 - 50 \text{ mV}$ of dynamic offset

Eg: 6 bit flash ADC, 1 V_{pp} diff. signal range

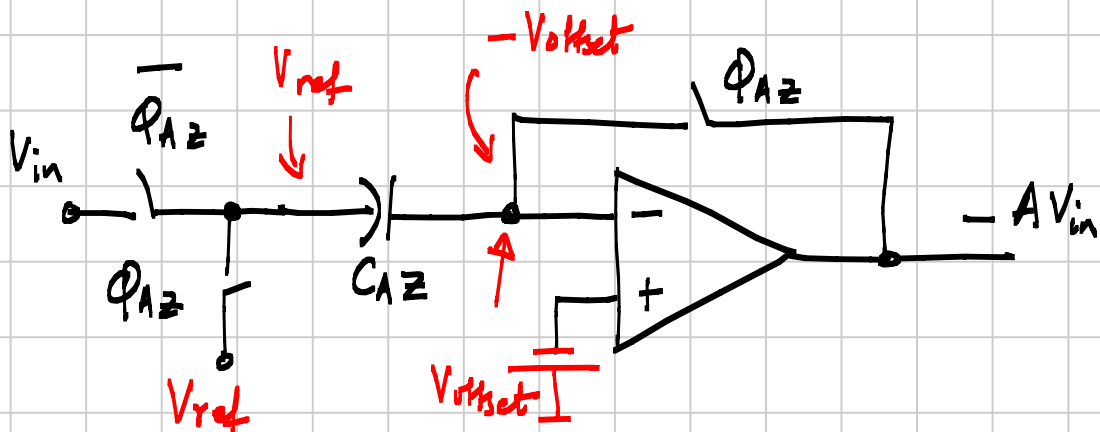
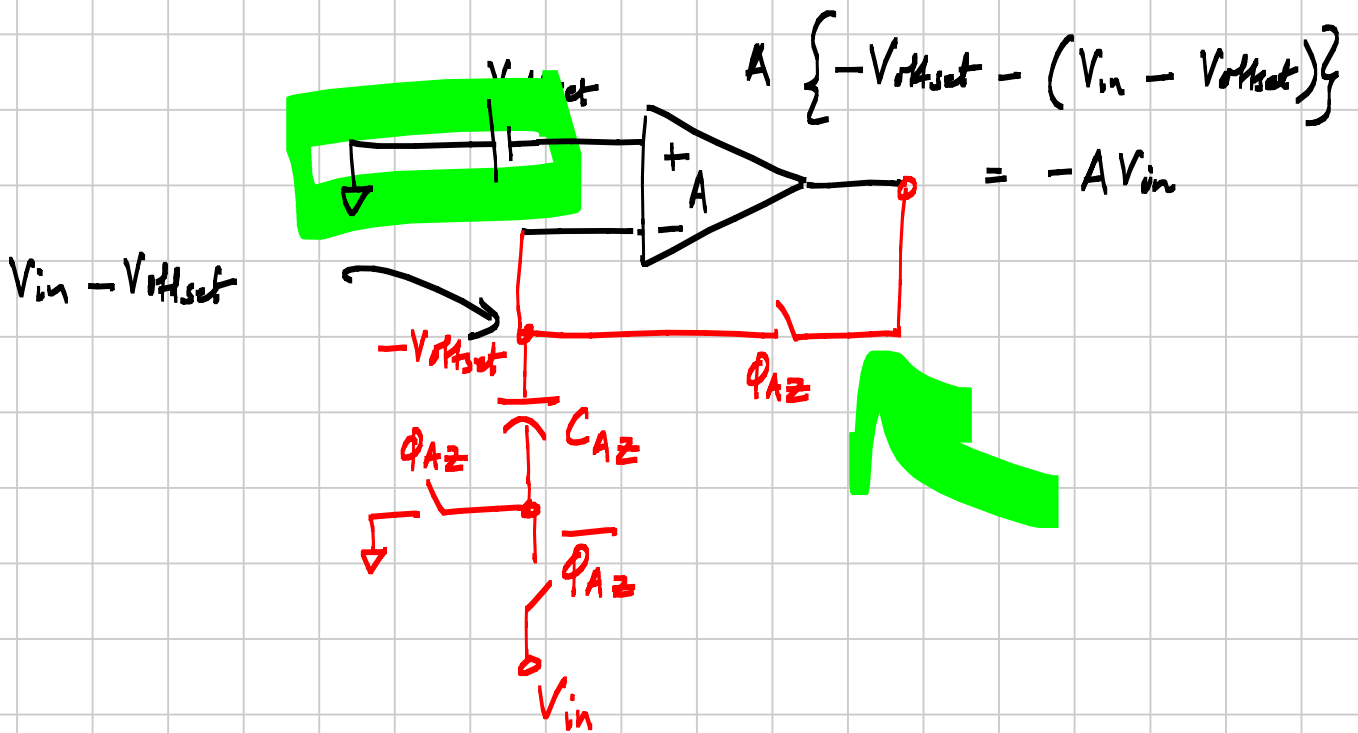
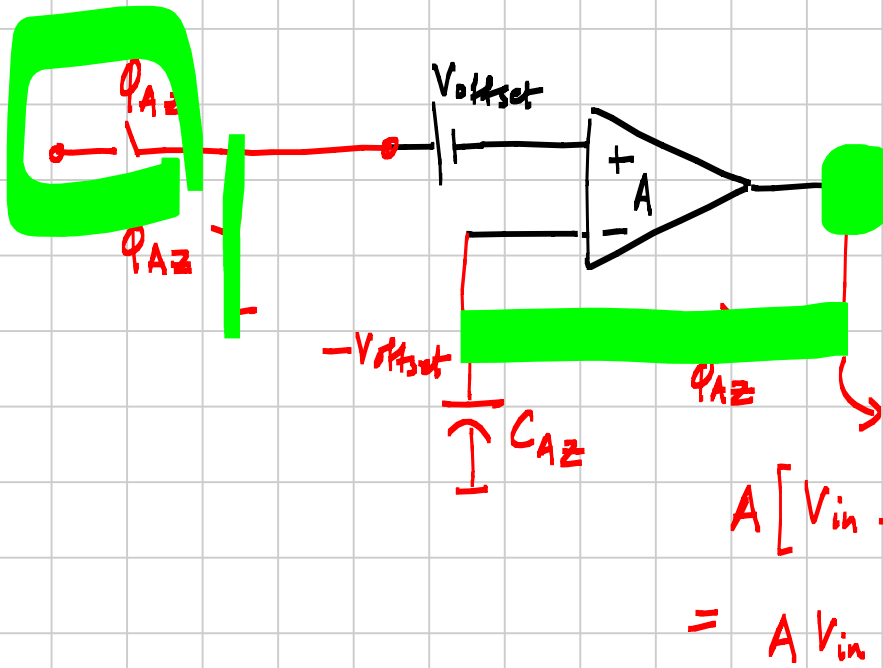
$$\text{LSB size} = \frac{1000 \text{ mV}}{64} \approx 16 \text{ mV}$$



If we know V_{offset} , we apply $V_{in} + V_{offset}$ rather than V_{in}

(i) Apply $V_{in} = 0$
 measure $V_{out} \rightarrow$
 get $V_{offset} \times$
 Amp will saturate

AZ $\rightarrow$ Auto Zero



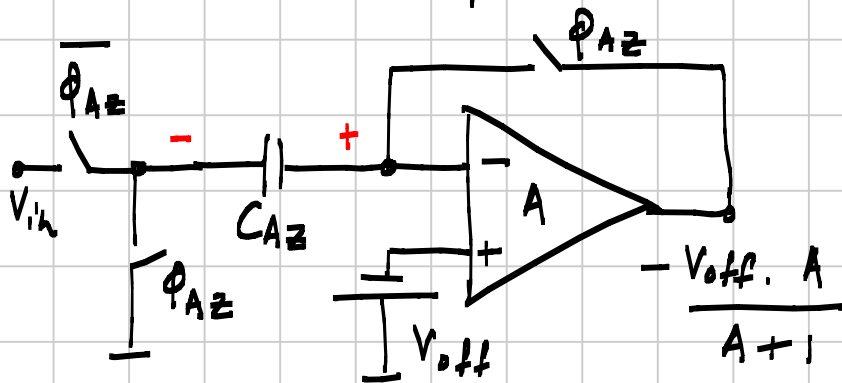
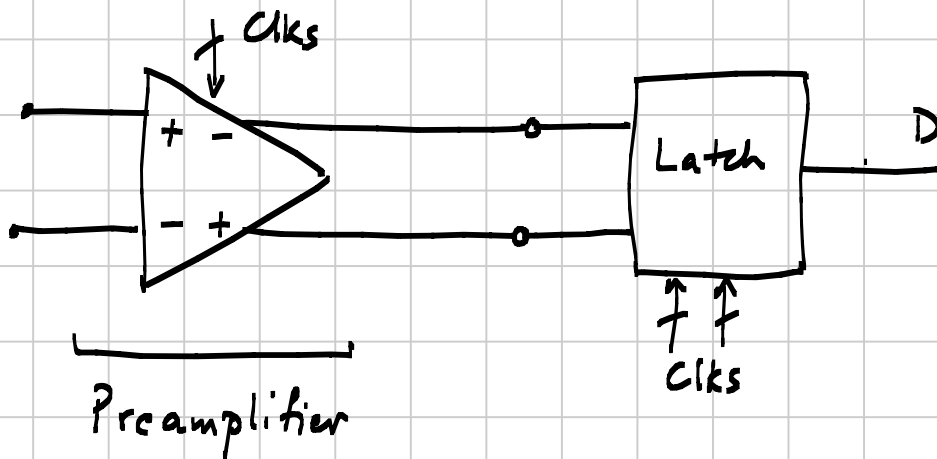
$$A \left\{ - \left[v_{in} - (v_{ref} + v_{offset}) \right] + (-v_{offset}) \right\}$$

$$= -A (v_{in} - v_{ref})$$

VLSI Data Conversion Circuits : Lecture 44

Note Title

21-03-2011

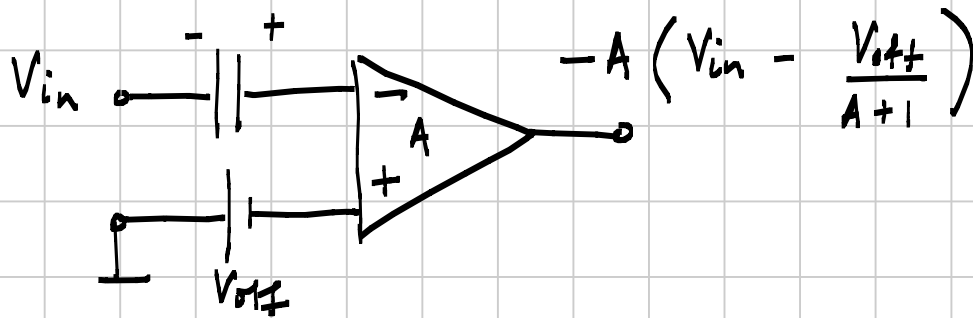


Voltage across C_{A2} at the end of ϕ_{A2}

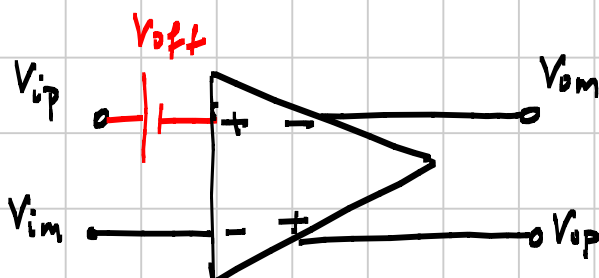
$$= -\frac{V_{off} \cdot A}{A+1}$$

Eq. circuit in the amplify phase (ϕ_{A2})

$V_{off} \cdot (A/A+1)$



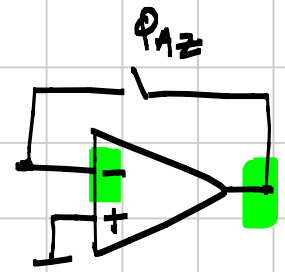
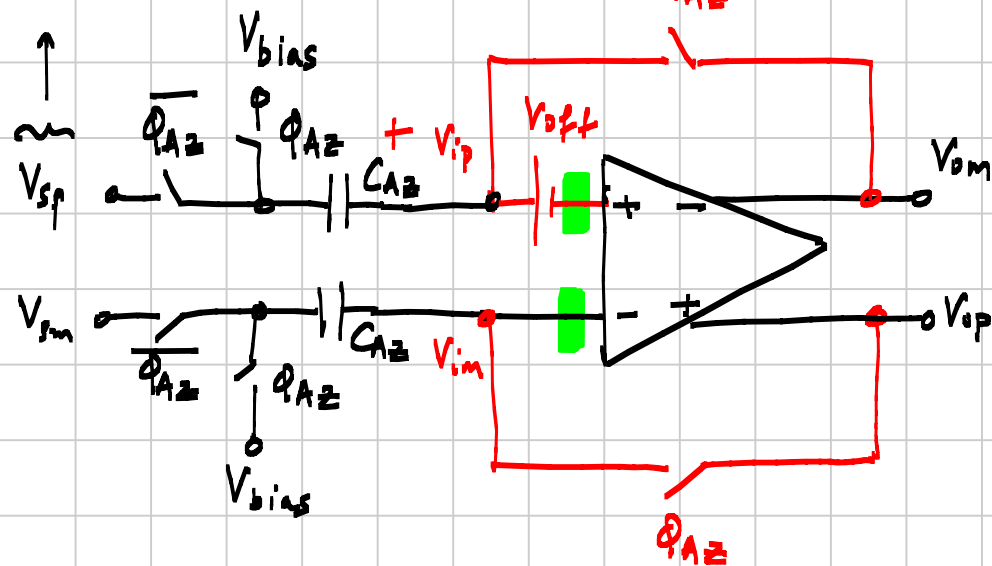
* Must make A very large.



Ideal: $V_{op} - V_{om} = A (V_{ip} - V_{im})$

Actual: $V_{op} - V_{om} = A (V_{ip} - V_{im} - V_{off})$

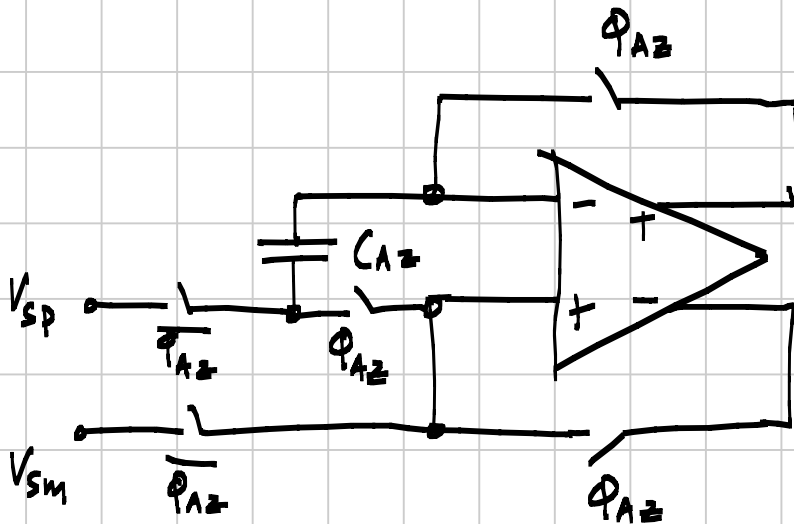
From the S/H

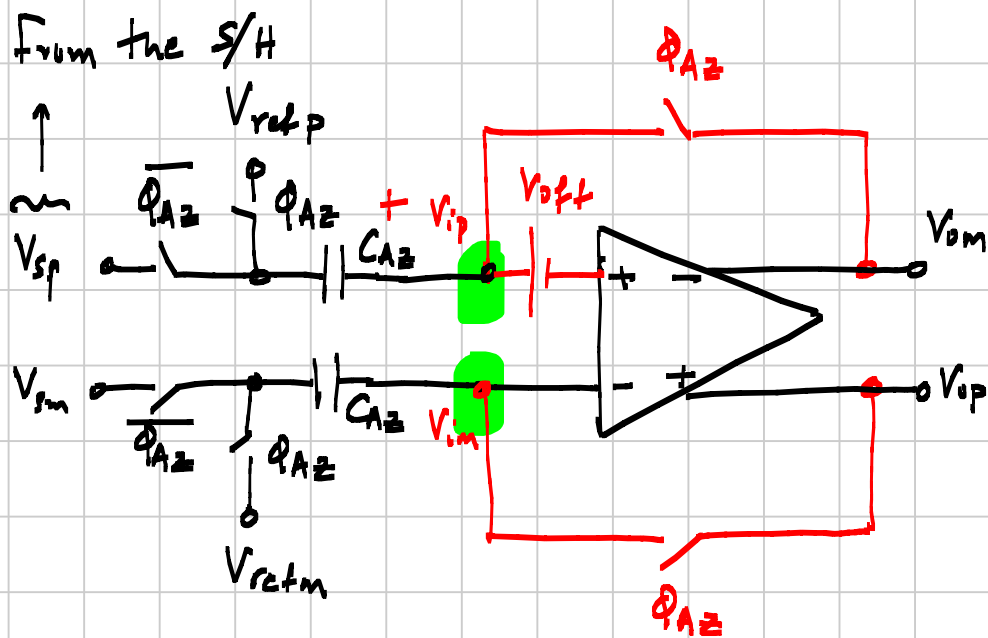


$$\left. \begin{array}{l} V_{om} - V_{bias} \\ V_{op} - V_{bias} \end{array} \right\}$$

$$\left[(V_{om} - V_{off}) - V_{op} \right] A = V_{op} - V_{om}$$

$$\Rightarrow V_{op} - V_{om} = \frac{-V_{off} A}{A + 1}$$





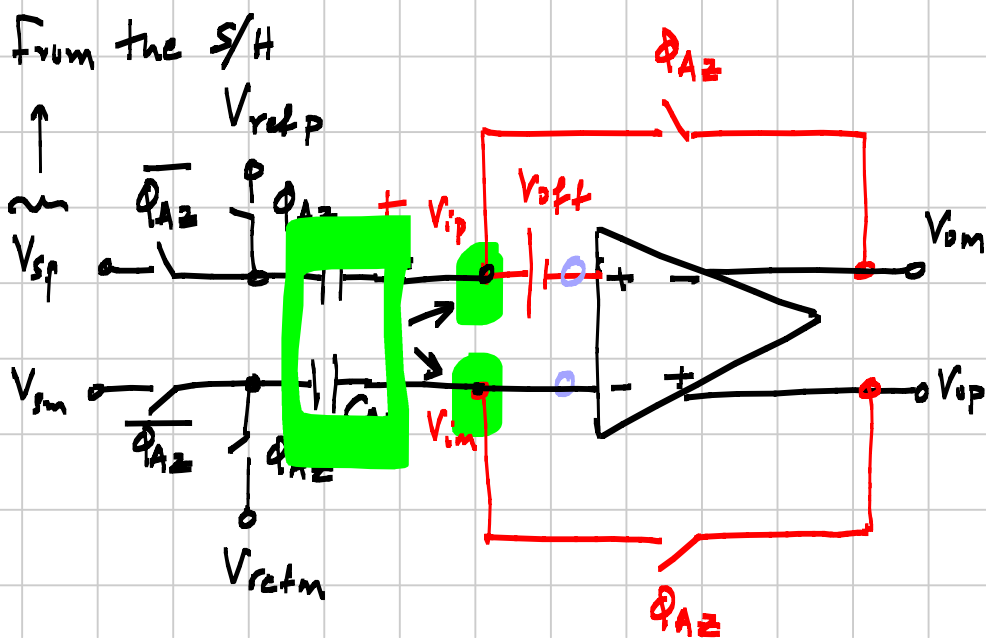
Diff. Voltage across C_{Az}

$$\left[\begin{array}{l} V_{om} - V_{refp} \\ V_{op} - V_{refm} \end{array} \right] = \frac{V_{off} (A/A+1)}{(V_{refp} - V_{refm})}$$

$$[V_{sp} + (V_{om} - V_{refp})] - [V_{sm} + (V_{op} - V_{refm})]$$

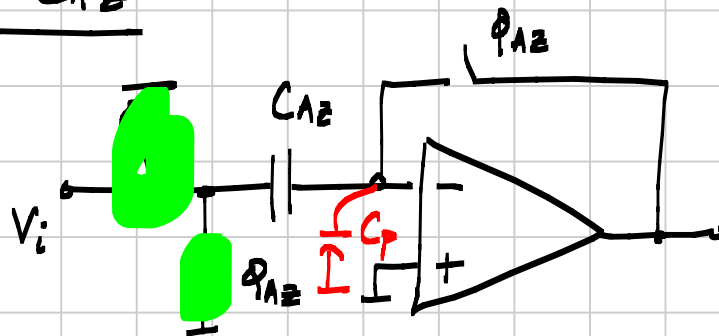
$$V_{ip} - V_{im} = (V_{sp} - V_{sm}) - \underbrace{(V_{op} - V_{om})}_{\text{at the end of } \phi_{Az}} - (V_{refp} - V_{refm})$$

$$= - \frac{V_{off} \cdot A}{A+1}$$



$$V_{op} - V_{om} = -A \left[(V_{sp} - V_{sm}) - (V_{refp} - V_{rem}) - \frac{V_{oh}}{A+1} \right]$$

Choice of C_{A2}



You want it large $\rightarrow$

$$* \frac{C_{A2}}{C_{A2} + C_p} = \text{Close to 1}$$

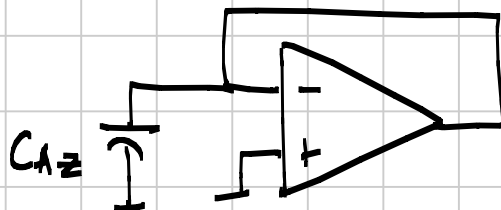


* Charge injection is smaller.

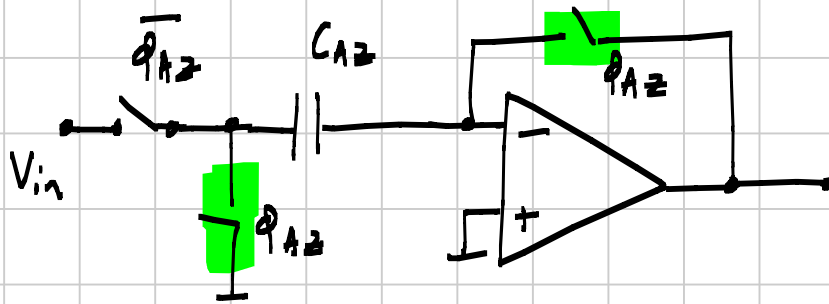
* Leakage

You want it small $\rightarrow$

Setting time becomes smaller.



VLSI Data Conversion Circuits : Lecture 45



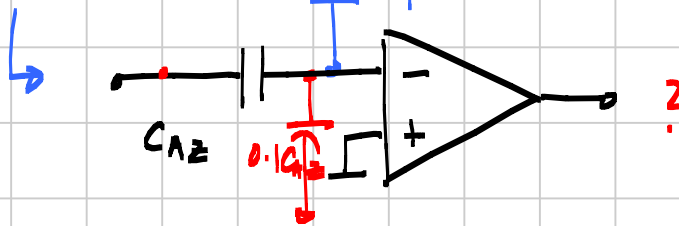
$$\approx 0.1 C_{A2} + C_p$$



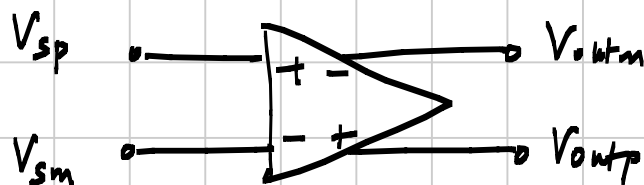
$$\frac{C_{A2}}{C_{A2} + C_p}$$



$$\approx 0.1 C_{A2} + C_p$$

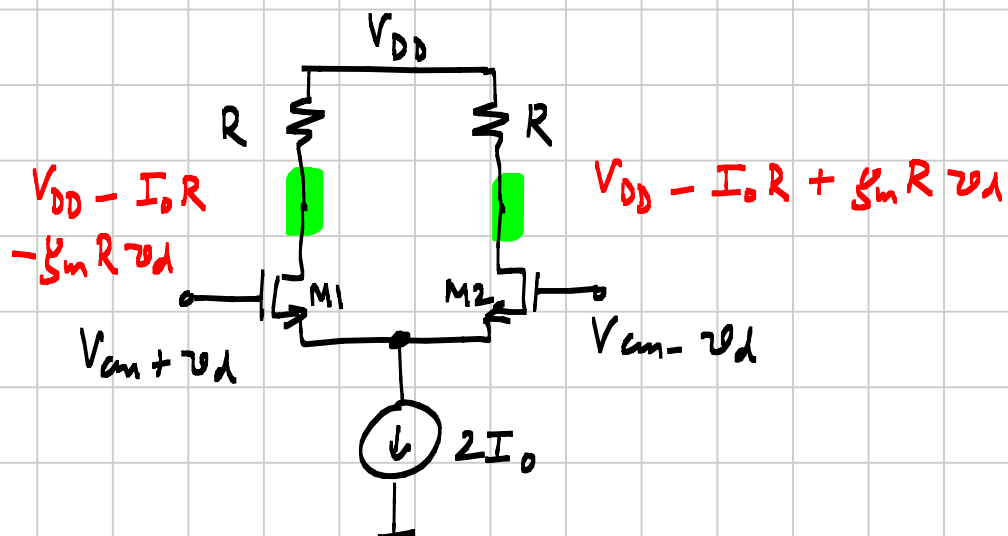


$$\frac{C_{A2}}{C_{A2} + 0.1 C_{A2} + C_p}$$

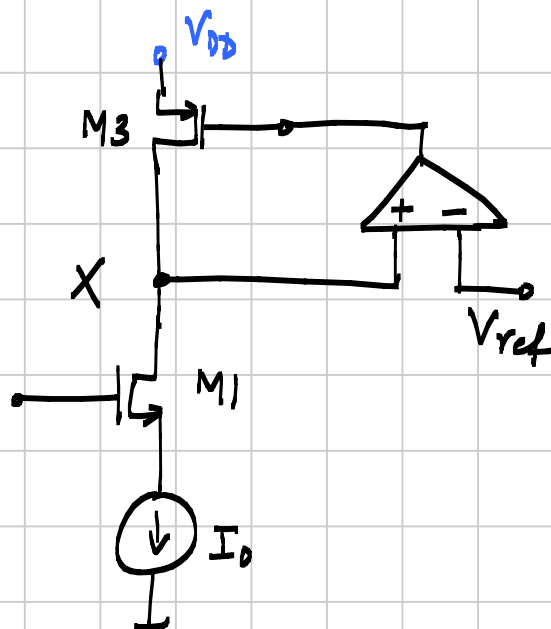
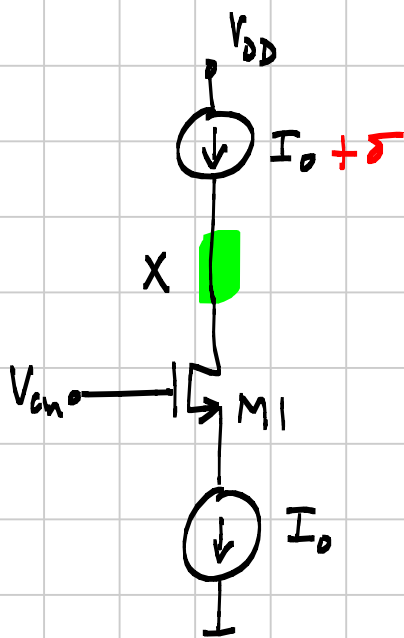
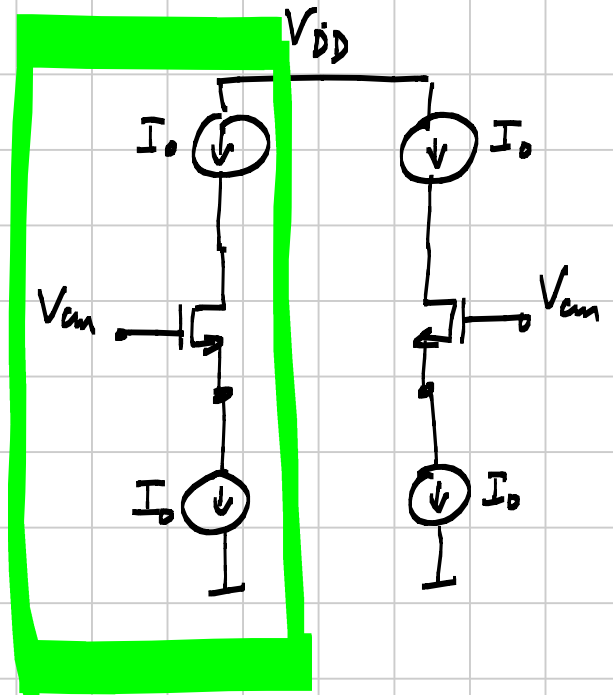
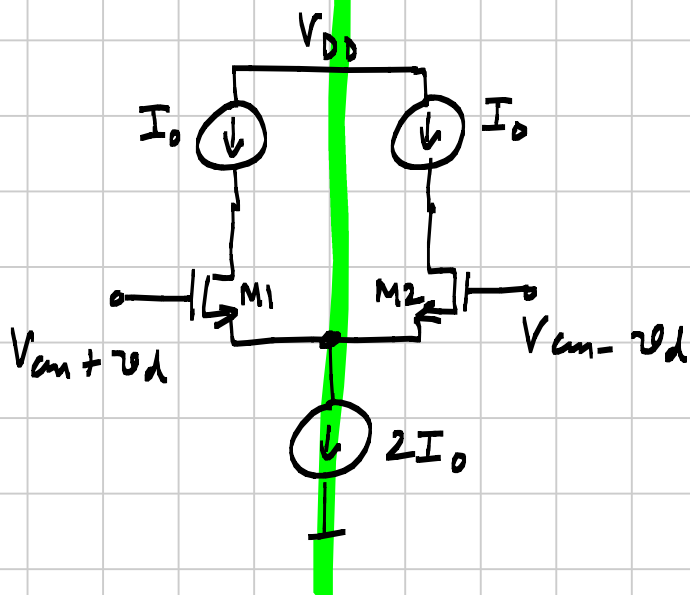


$$V_{outp} - V_{outm} = A (V_{sp} - V_{sm})$$

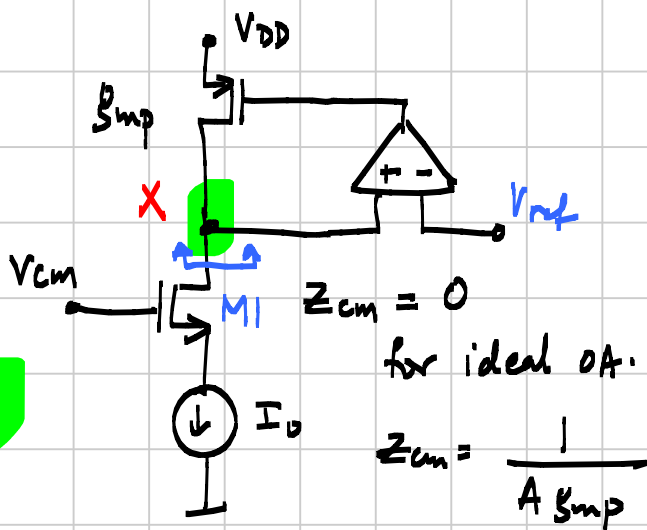
$$\left. \begin{array}{l} V_{sp} \\ V_{sm} \end{array} \right\} \begin{array}{l} V_{cm} + v_d \\ V_{cm} - v_d \end{array}$$



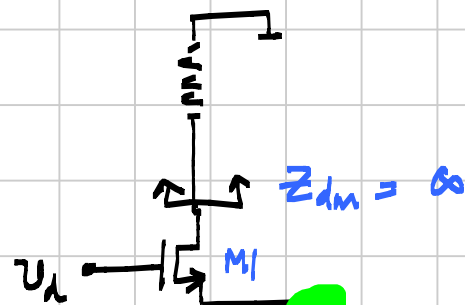
$$\text{Gain} = g_m R$$



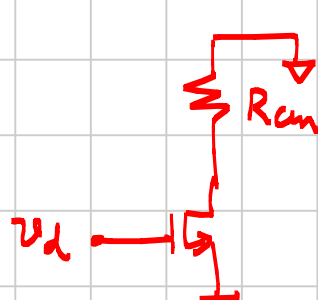
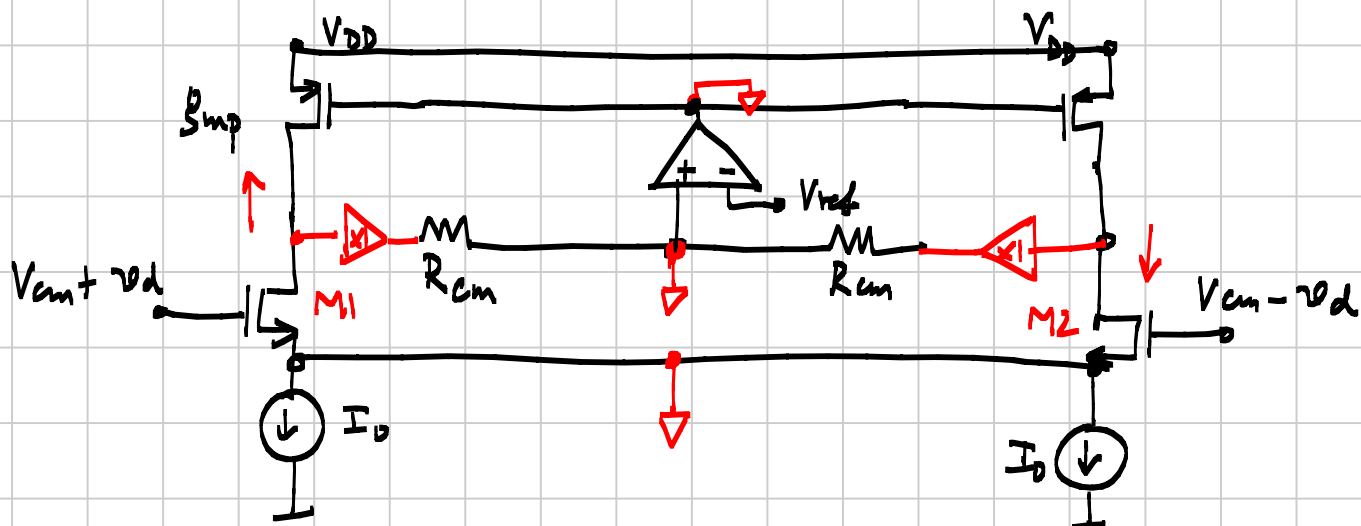
$V_k \uparrow$
 $\Rightarrow I_L$ is too high
 $\Rightarrow$ Must increase V_G



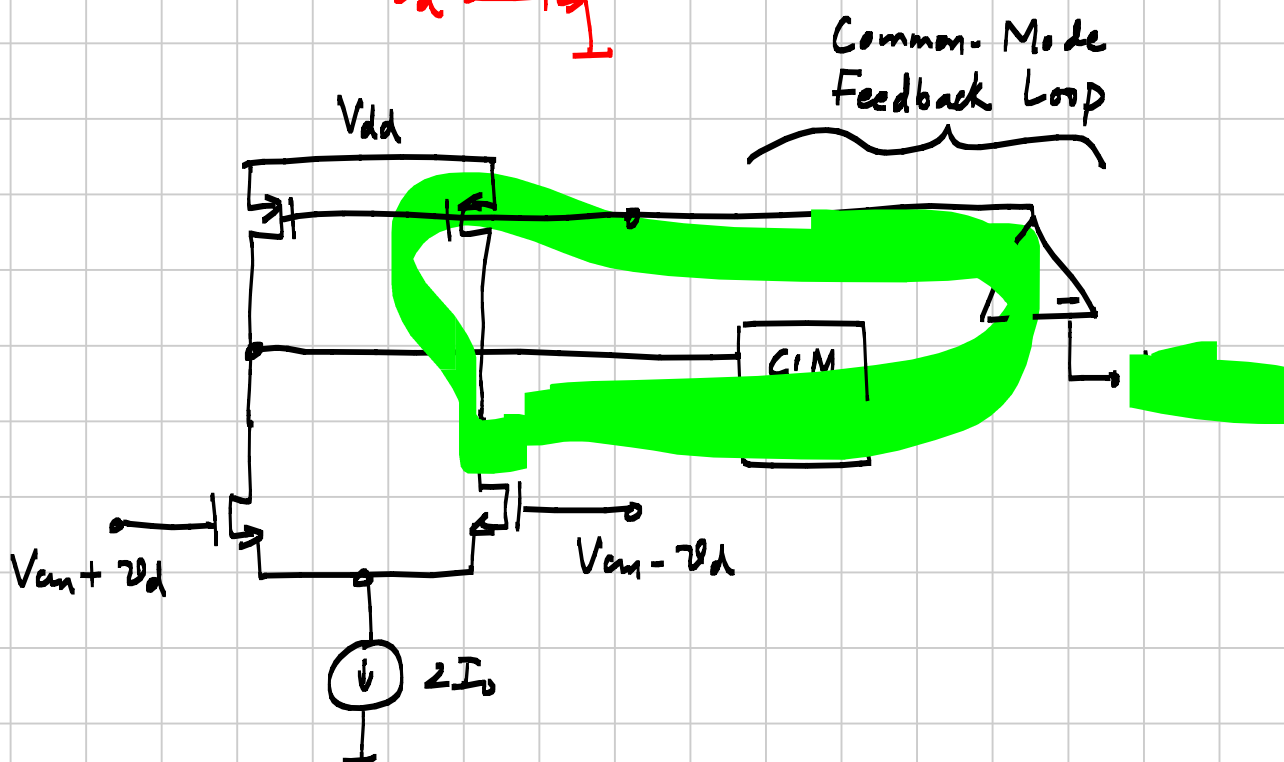
This MUST be the CM eq.



Diff mode eq.

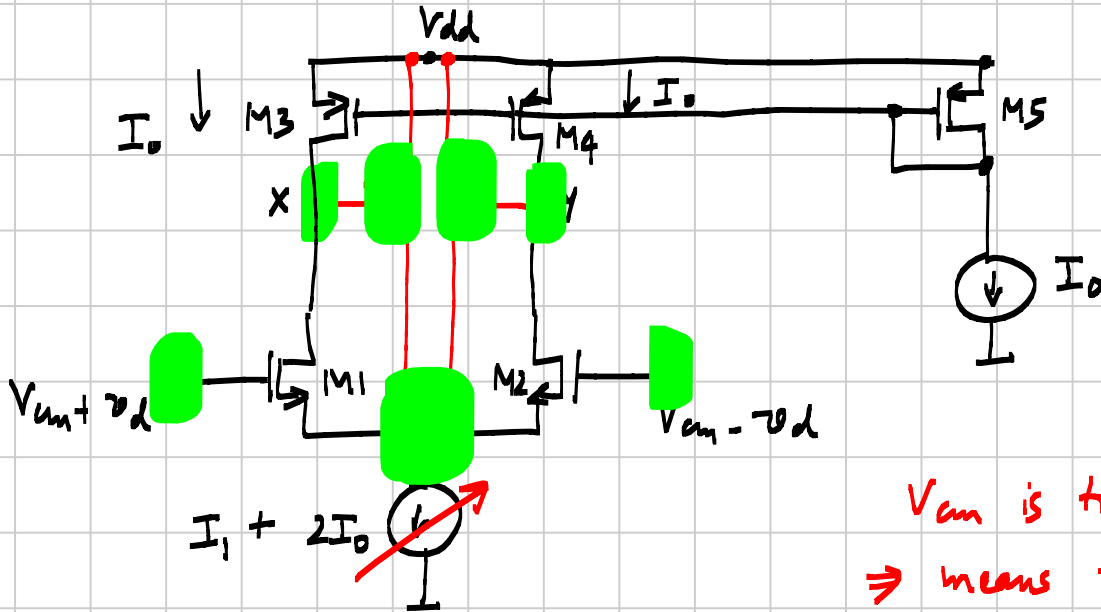


R_{cm} very large

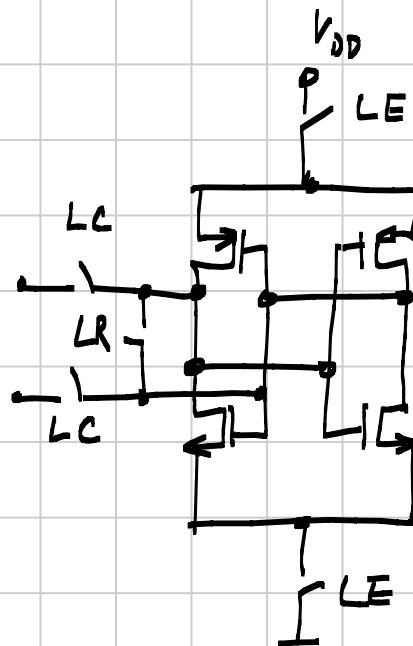
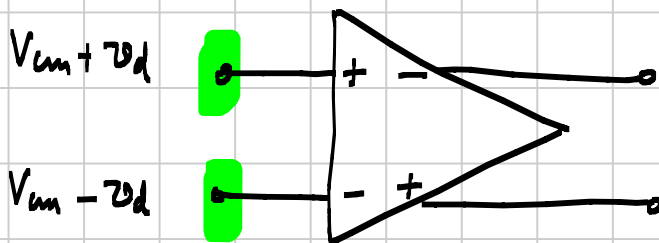
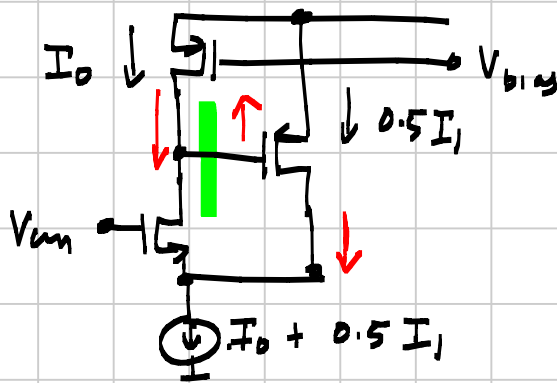


VLSI Data Conversion Circuits : Lecture 46

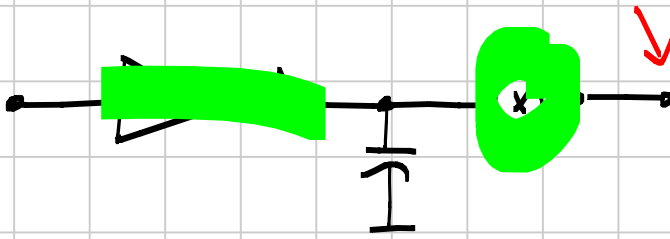
Note Title



V_{cm} is too high
 $\Rightarrow$ means tail I too low
 $\Rightarrow$ MUST increase tail I



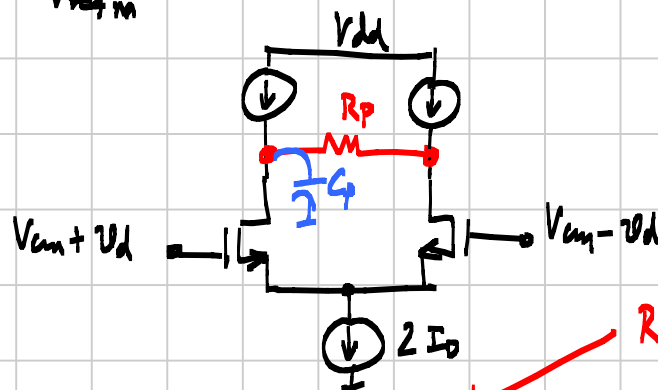
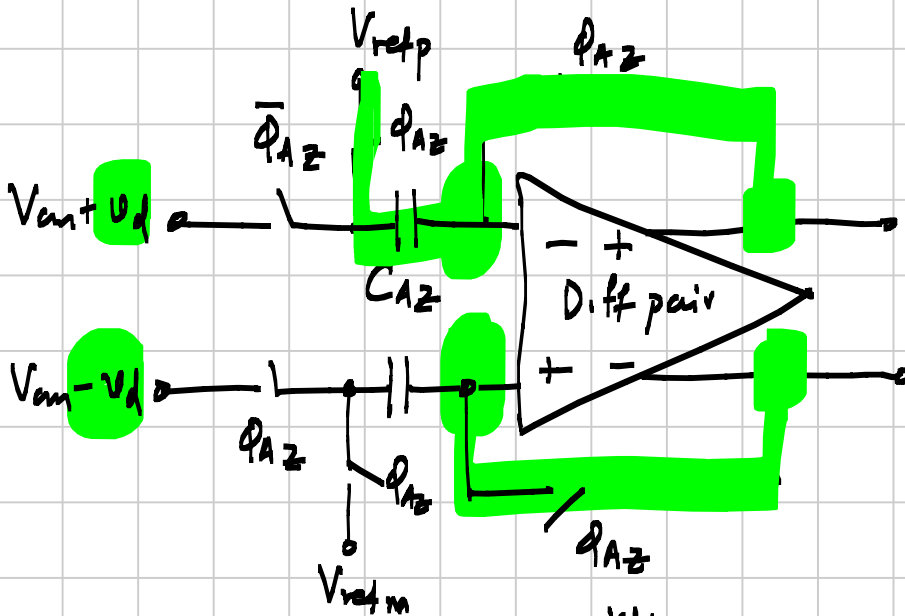
LC $\rightarrow$ Latch Connect
 LE $\rightarrow$ Latch Enable
 LR $\rightarrow$ Latch Reset



Preamp
Latch

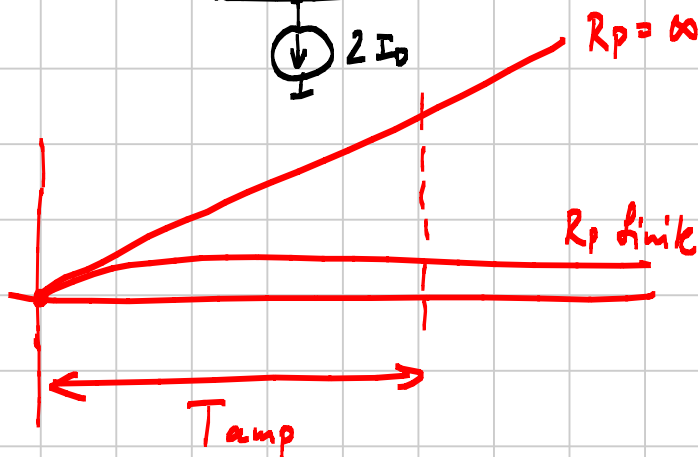
Auto zero

Amplify



Integrating
preamp

$$\frac{g_m R_p}{1 + s C_p R_p}$$



$$\frac{g_m v_d}{C_p}$$

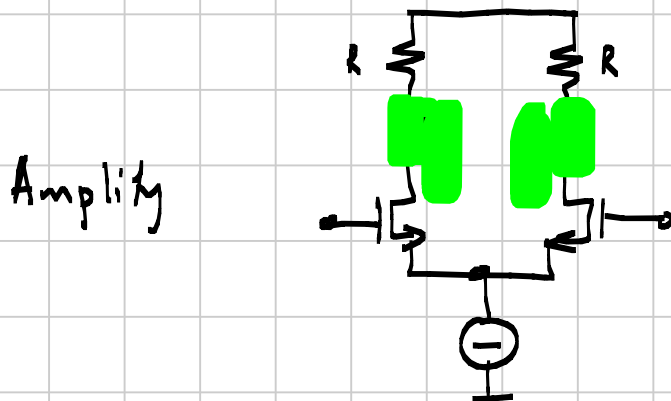
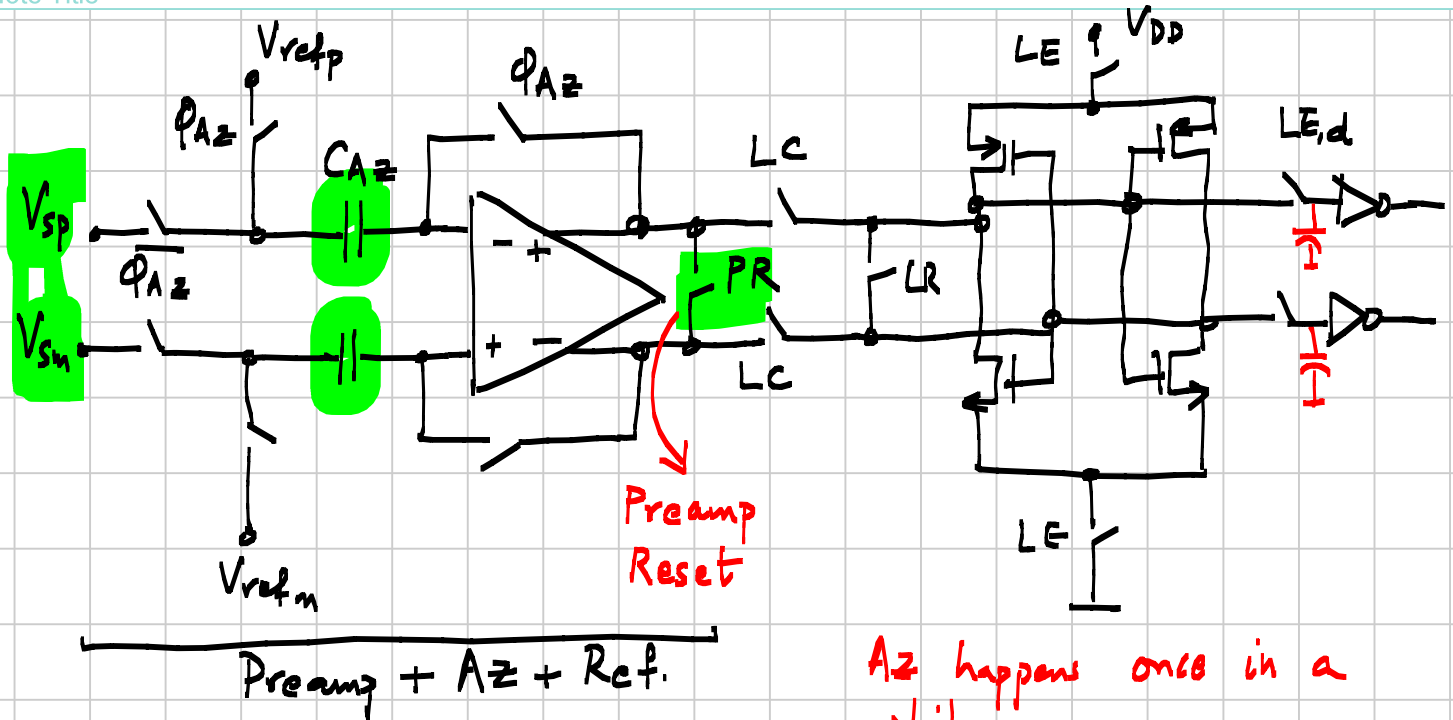
$$\Rightarrow \text{Gain} = \left[\frac{g_{mn}}{C_p} \cdot T_{amp} \right] \text{ Dynamic Gain}$$

if $R_p \rightarrow \infty$



VLSI Data Conversion Circuits : Lecture 47

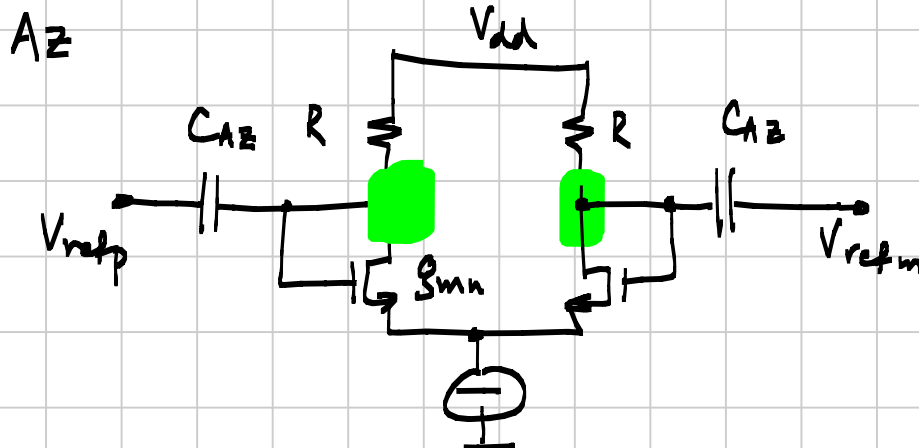
Note Title



$$S_{mn} R \leftarrow \text{Gain}$$

$$\text{Gain} \propto R$$

$$\text{BW} \propto 1/R$$



$R \rightarrow \infty$ } Why:
Active load
with CMFB

Bandwidth

$$\frac{S_{mn}}{C_{AZ}}$$

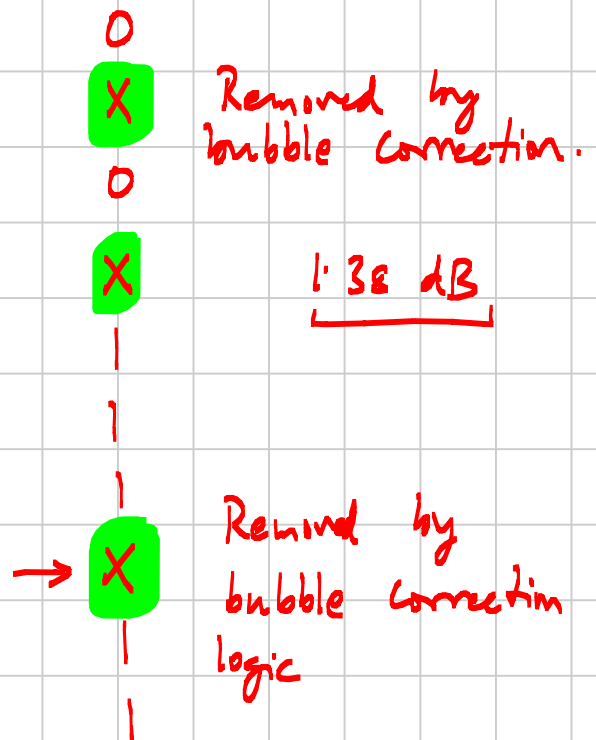
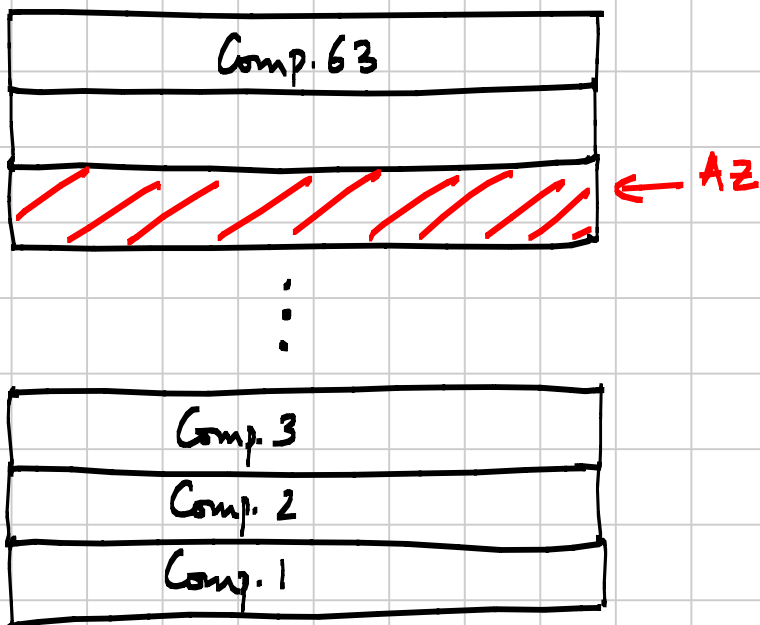
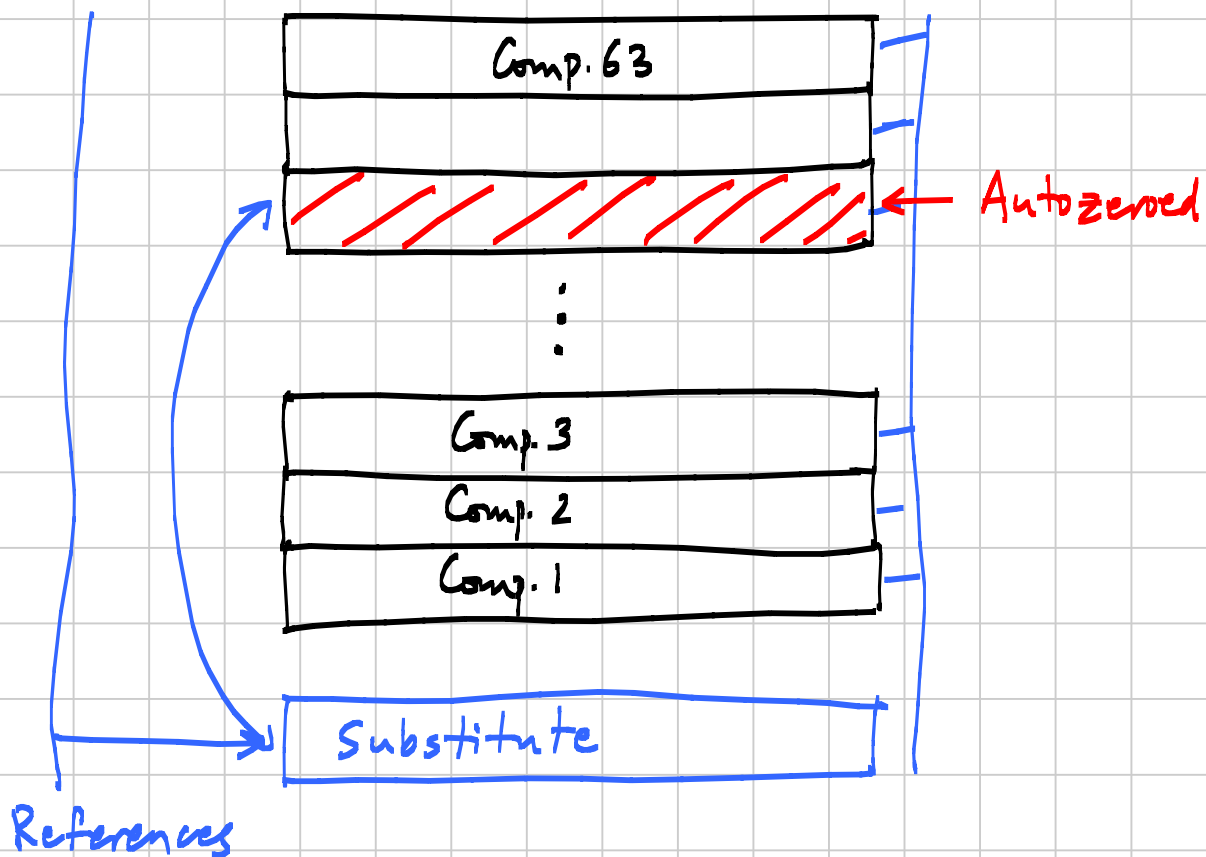
AZ once in a while :

* Comparator is not available for conversion during AZ cycle

→ Foreground AZ, foreground offset correction

→ ADC is UNAVAILABLE during this period

Offset correction by background AZ



VLSI Data Conversion Circuits : Lecture 49

Note Title

* ADC nonidealities are noise-shaped in a $\Sigma\Delta$ loop

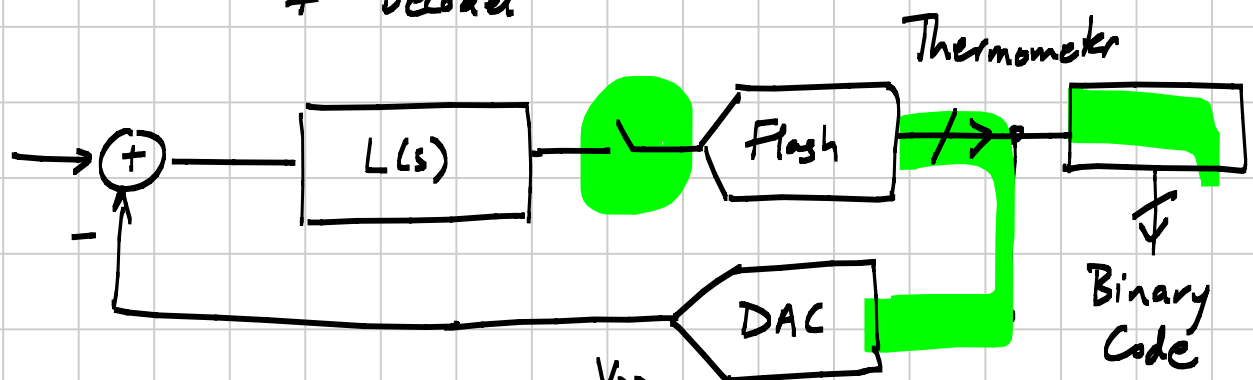
⇒ Quantizer resolution in a $\Sigma\Delta$ is restricted to about 4 bits

⇒ Comparator offsets

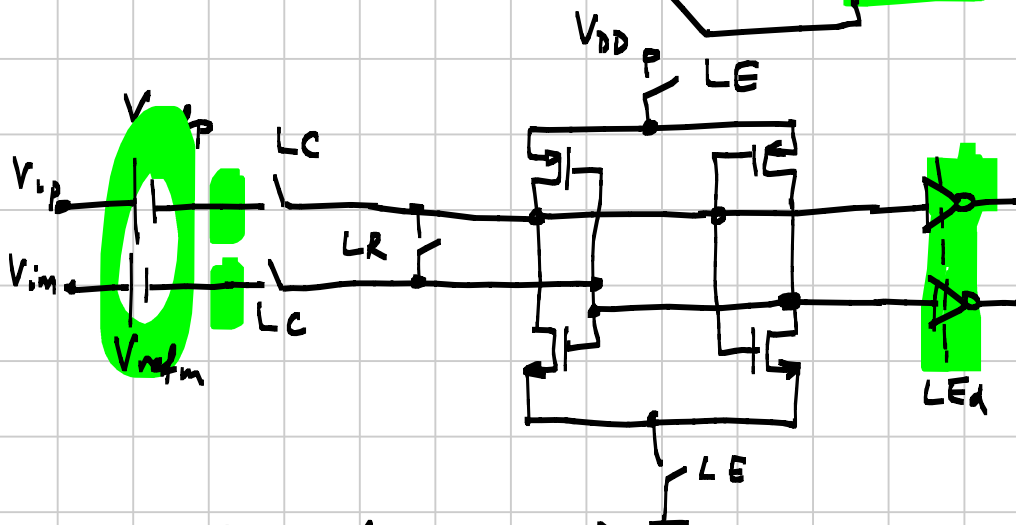
Conventional: Bubble Correction

+ Transition detect

+ Decoder

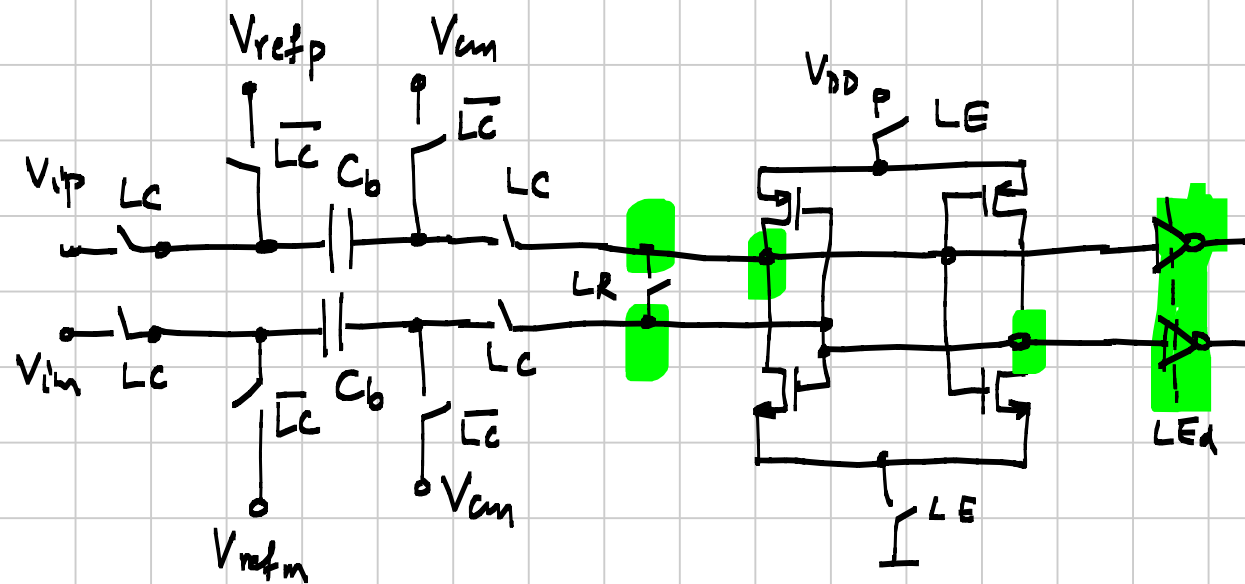


Sampling instant
→ falling edge of LC

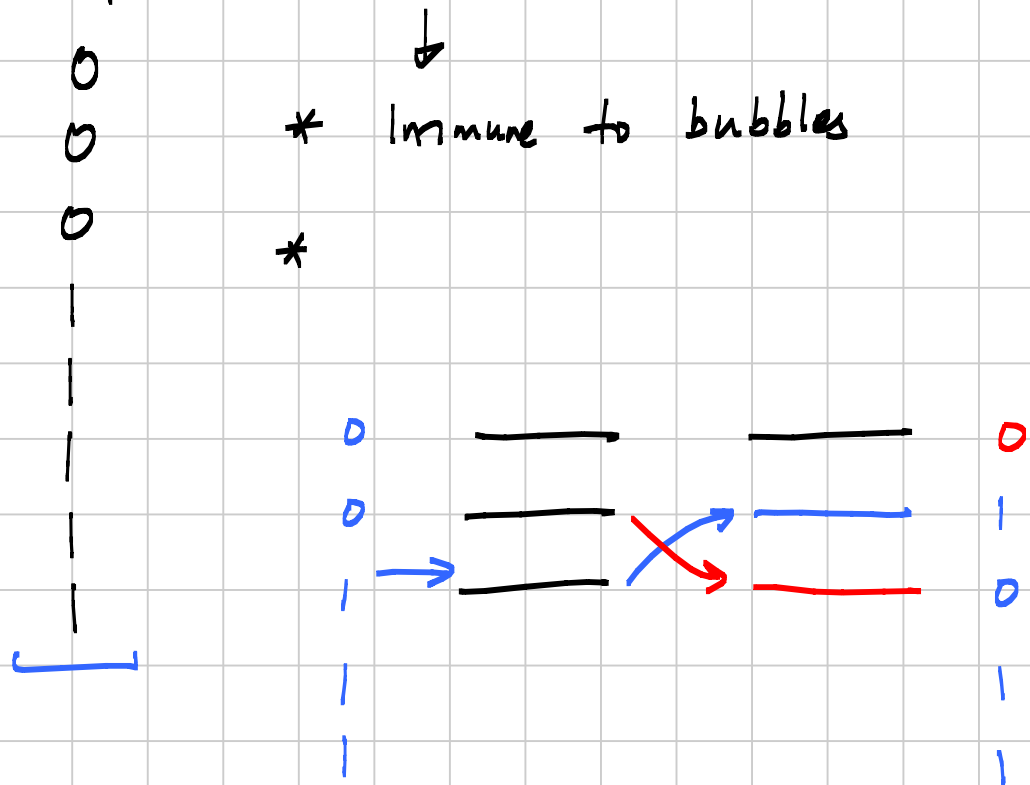


$$(V_{ip} - V_{refp}) - (V_{im} - V_{refm})$$

$$= V_{ip} - V_{im} - (V_{refp} - V_{refm})$$

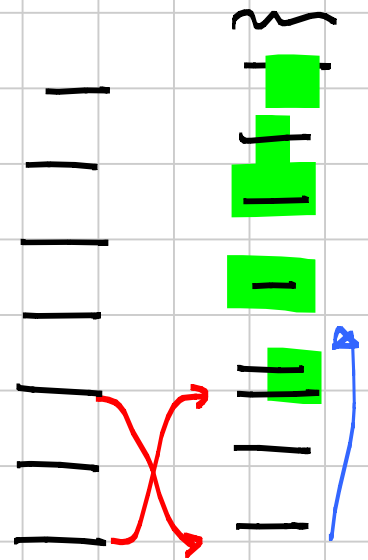
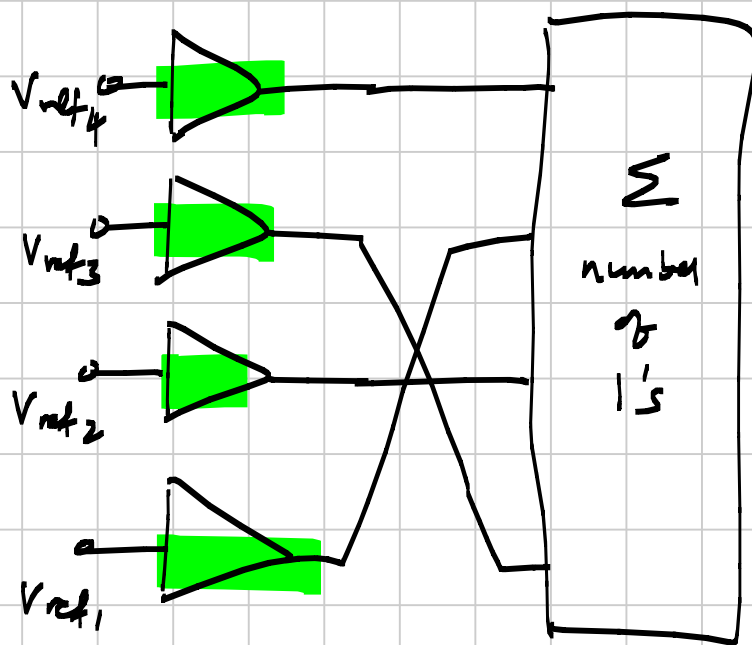


Digital O/P simply adds up the number of 1's in the "thermometer" code.

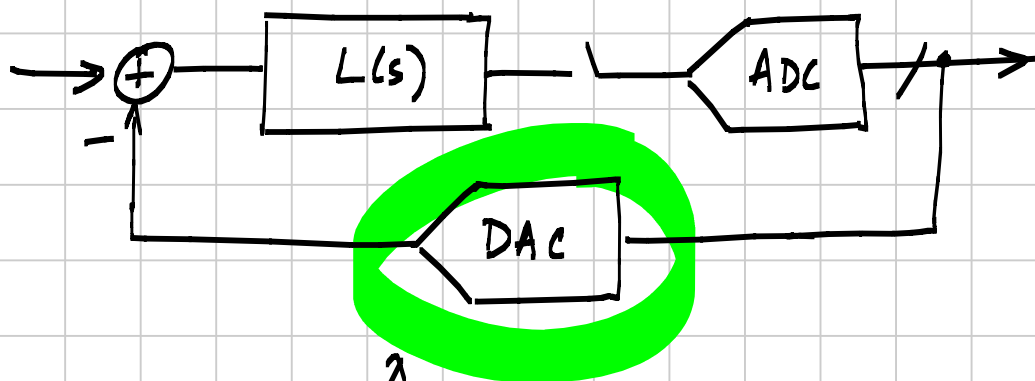


In a regular flash (Bubble correction + Transition Detect + Decoder)

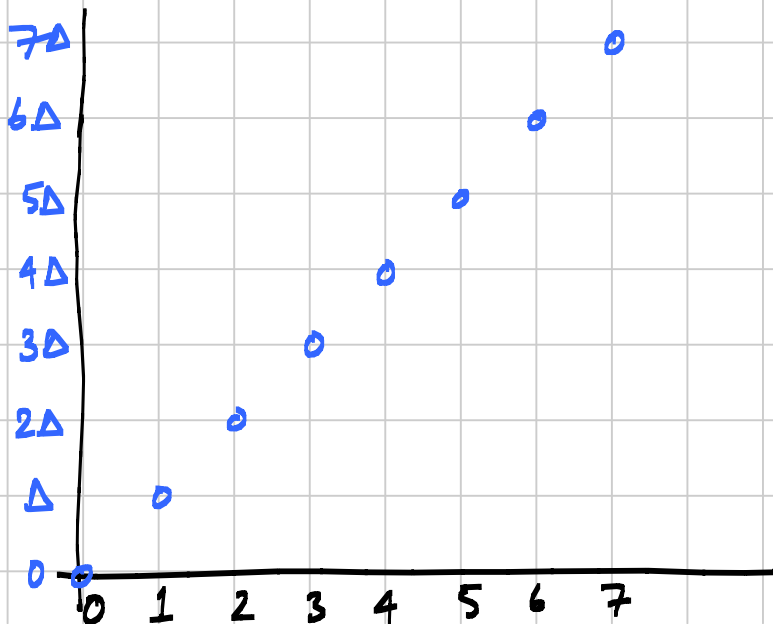
* position of a comparator in the array matters



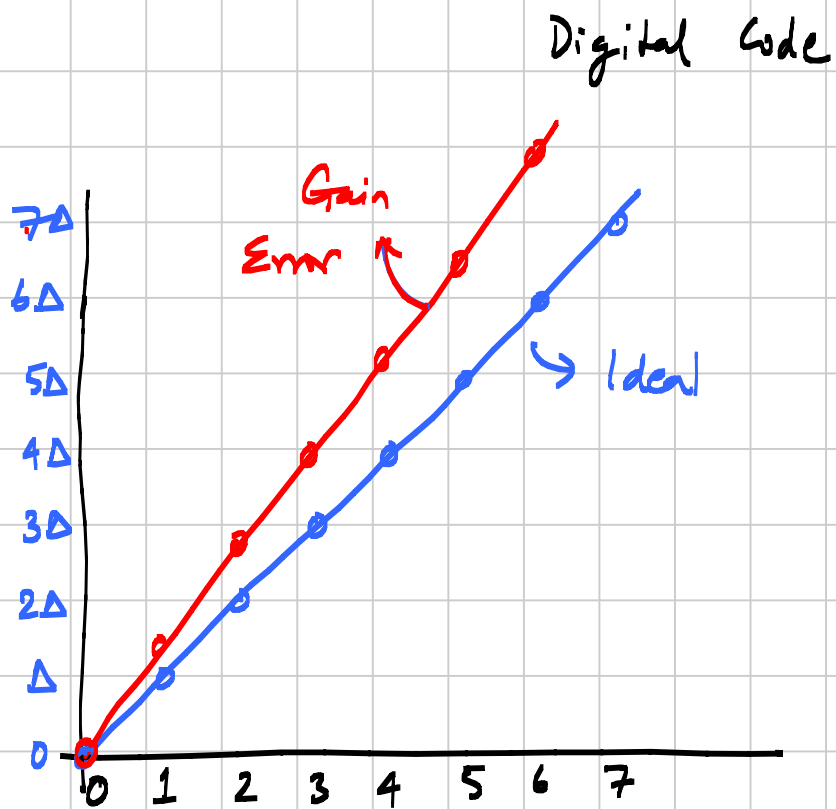
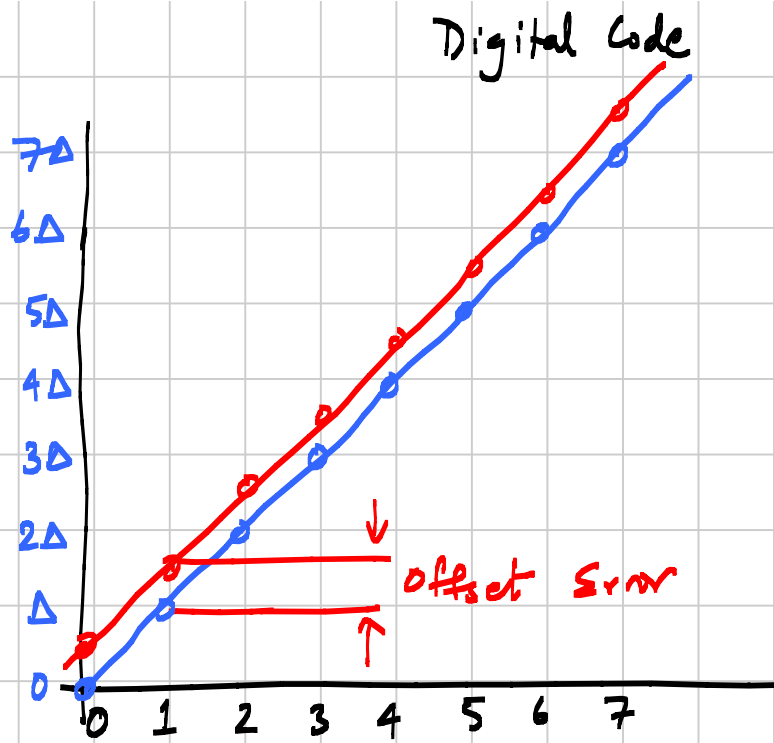
VLSI Data Conversion Circuits : Lecture 50

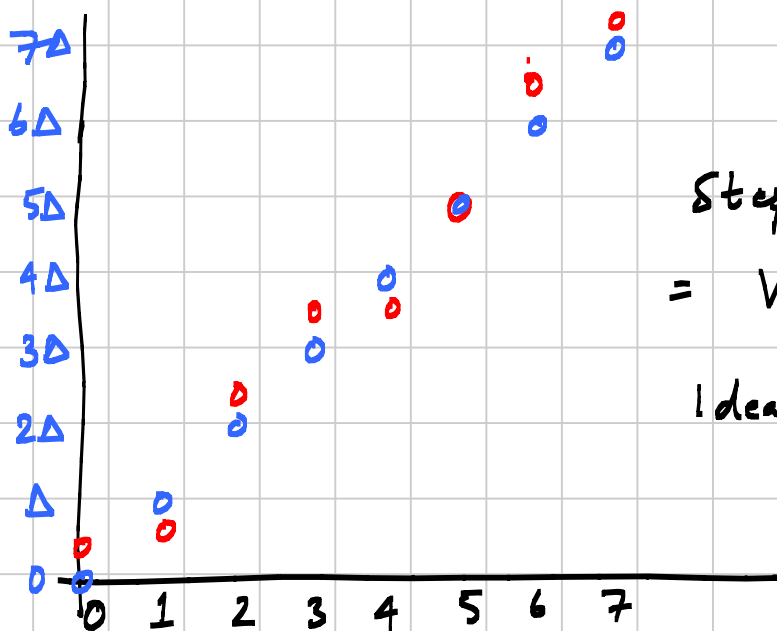


Input is a digital code.



← 3 bit
D/A converter
 Δ is the LSB,
or step size





Step Size (n)

$$= V_{n+1} - V_n$$

Ideally should be Δ .

$$DNL(n) = \frac{V_{n+1} - V_n - \Delta}{\Delta} \quad \left[\begin{array}{l} \text{Normalized to} \\ \text{the step size} \end{array} \right]$$

in LSB

Normalized Absolute Deviation from the ideal output level

$$= \frac{V_n - n\Delta}{\Delta} = \text{Integral Non Linearity (n)} = INL(n)$$

$$\sum DNL = INL, \text{ like in ADCs}$$

In practice

$$\Rightarrow \text{Offset} + \text{Gain Error} + \text{Nonlinearity}$$

To find DNL/INL

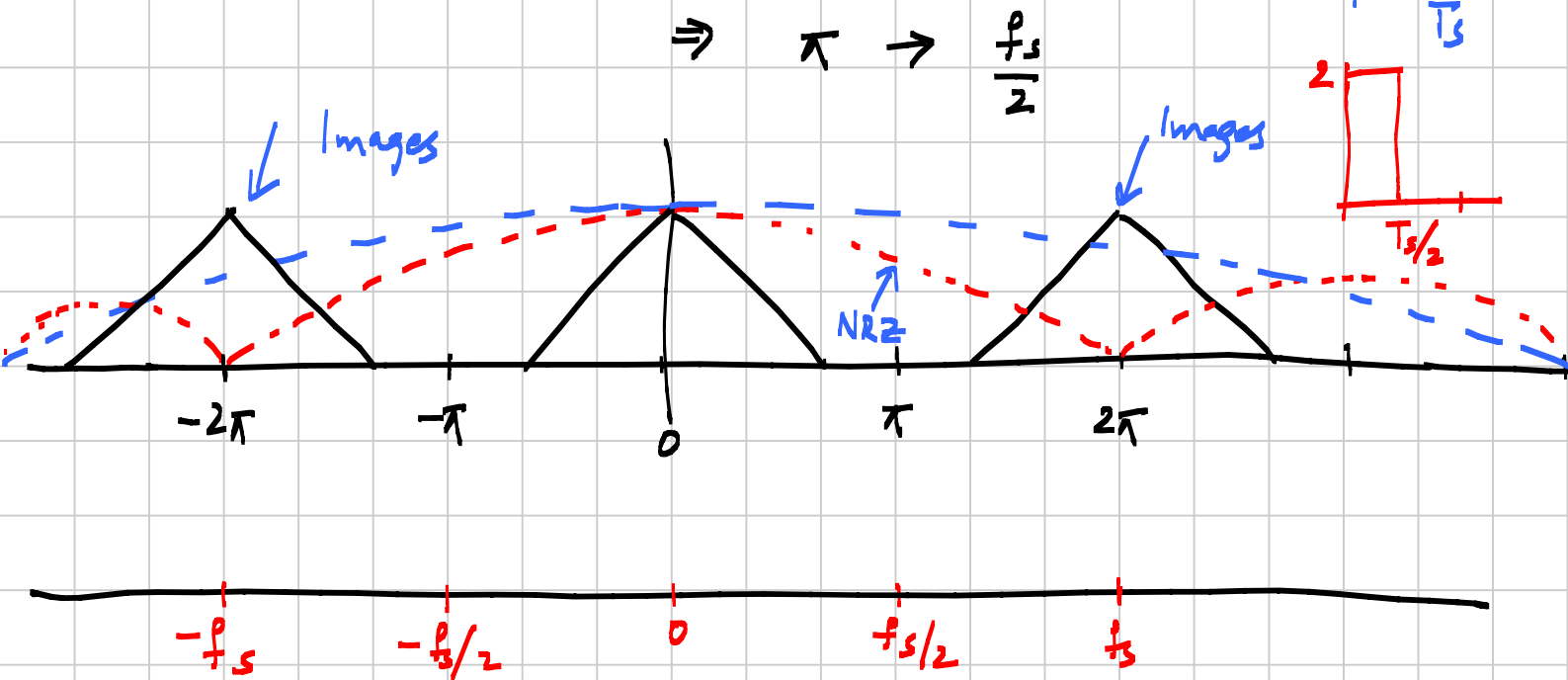
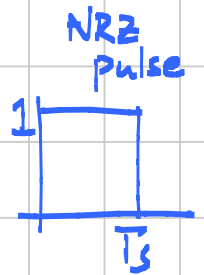
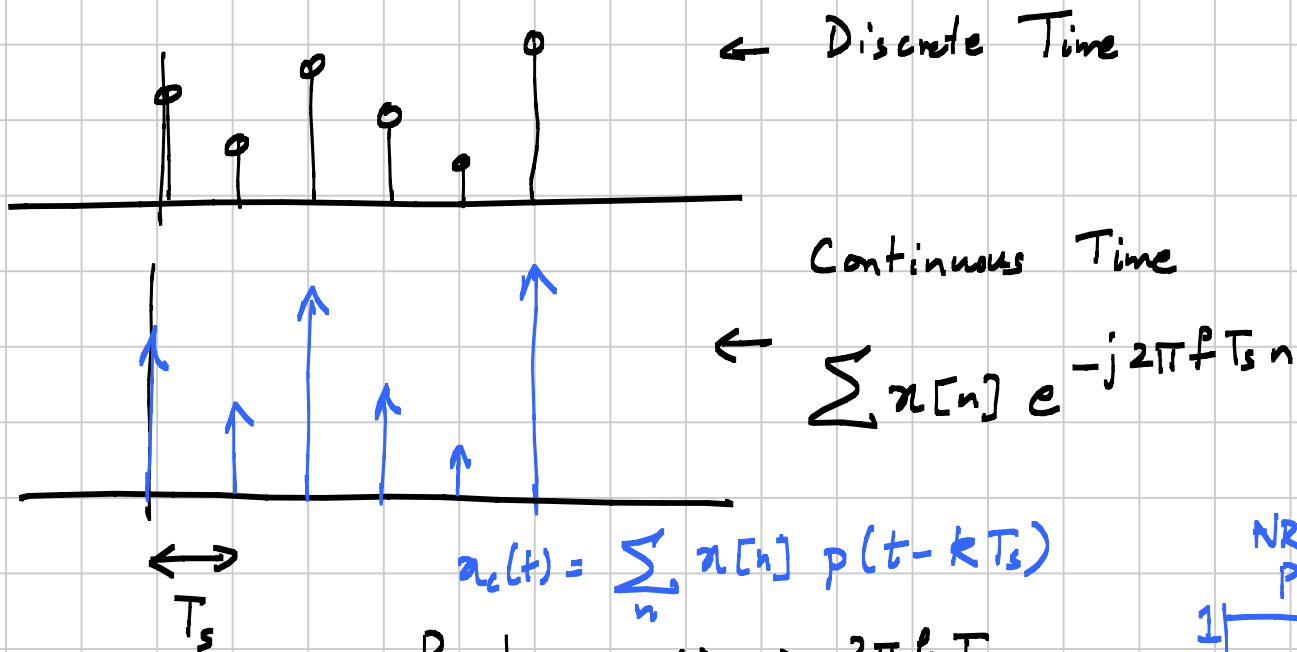
Step 1 $\Rightarrow$ Remove offset & gain error [by least squares fitting]

Step 2 $\Rightarrow$ Find DNL & INL with the LSB obtained from

Step 1.

Dynamic performance :-

$$\sum_{n=-\infty}^{\infty} x[n] e^{-j\omega n} = X(e^{j\omega})$$

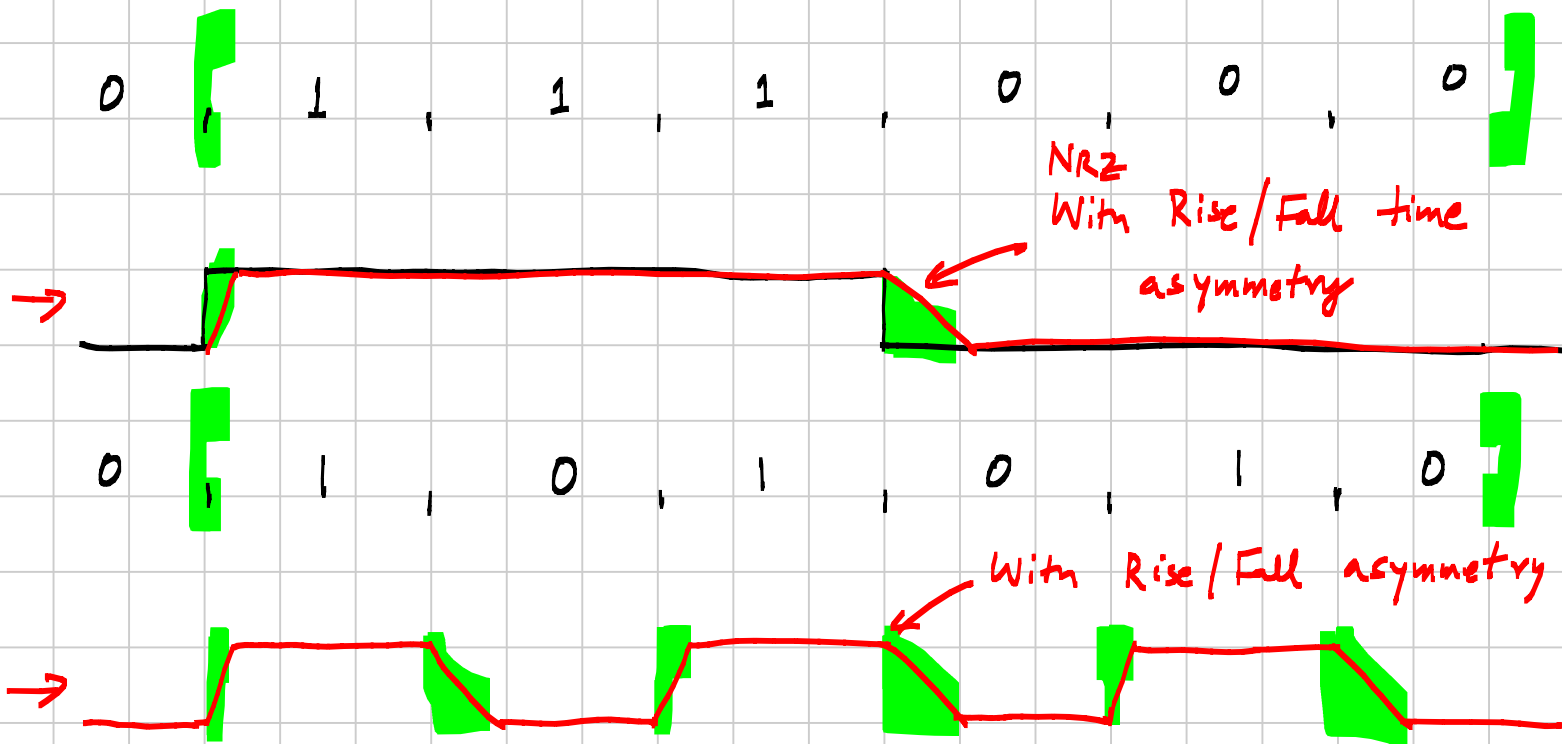


NRZ pulse $\rightarrow T_s \text{sinc}(fT_s)$

nulls @ multiples of $\frac{1}{T_s}$

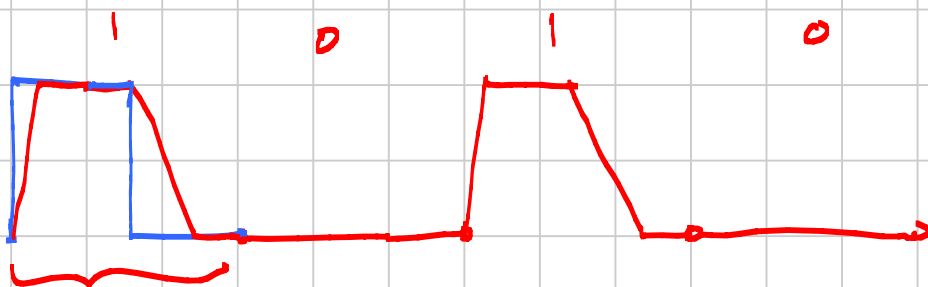
$$\text{RZ pulse} \rightarrow \frac{2T_s}{2} \text{sinc}\left(f \frac{T_s}{2}\right) = T_s \text{sinc}\left(f \frac{T_s}{2}\right)$$

nulls @ even multiples of $\frac{1}{T_s}$

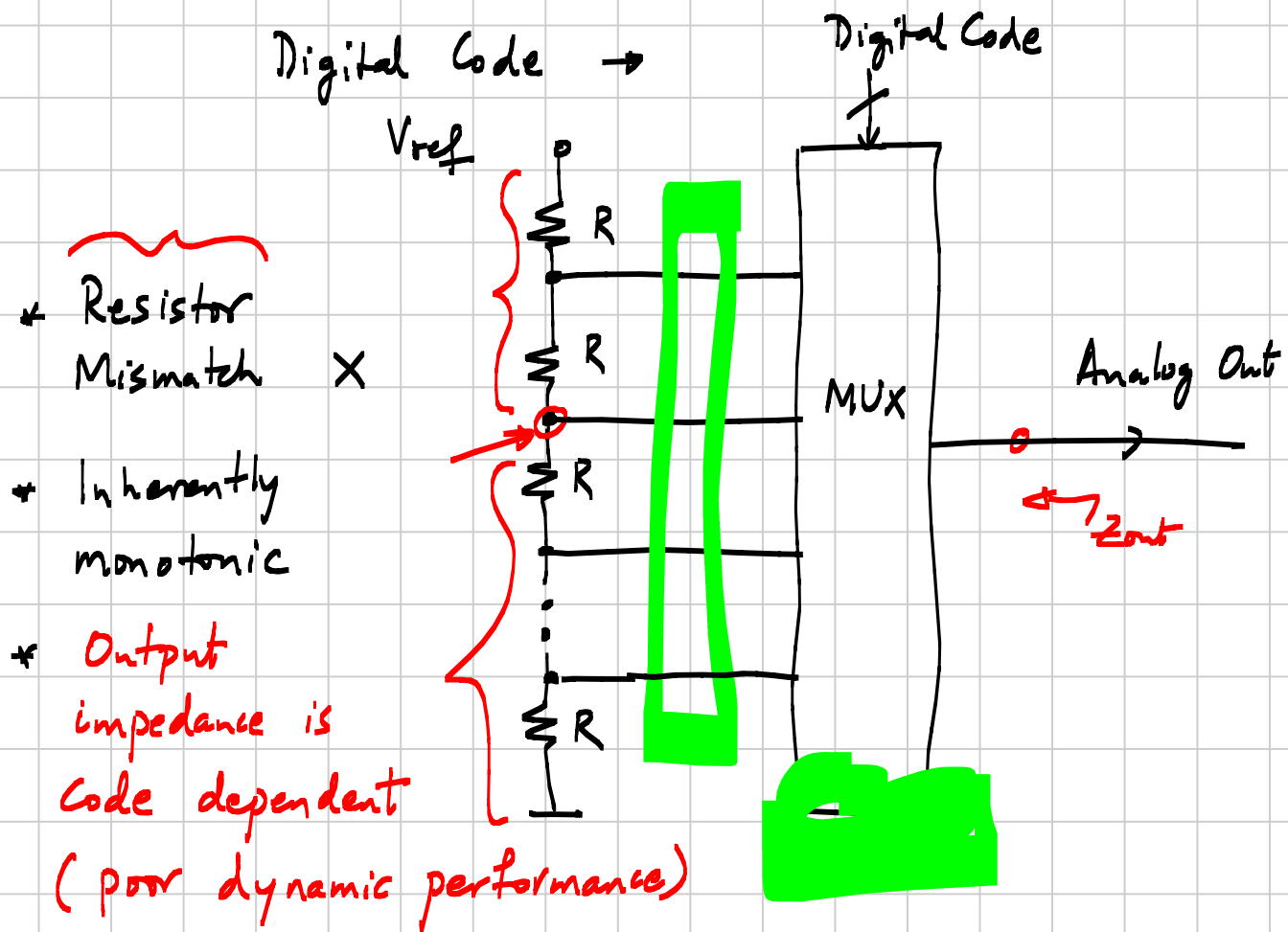


Two sequences with the same average value result in waveforms with different averages.

⇒ Nonlinearity



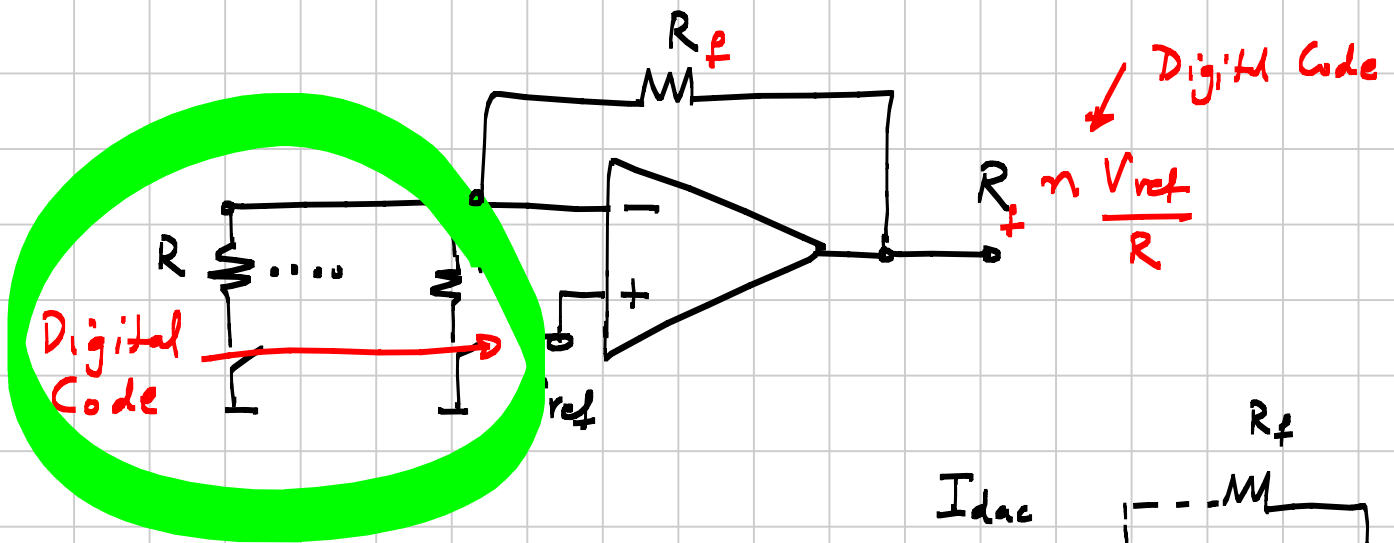
RZ DAC is immune to rise time - fall time asymmetry.



* Messy decoding logic / band limiting at the output node.

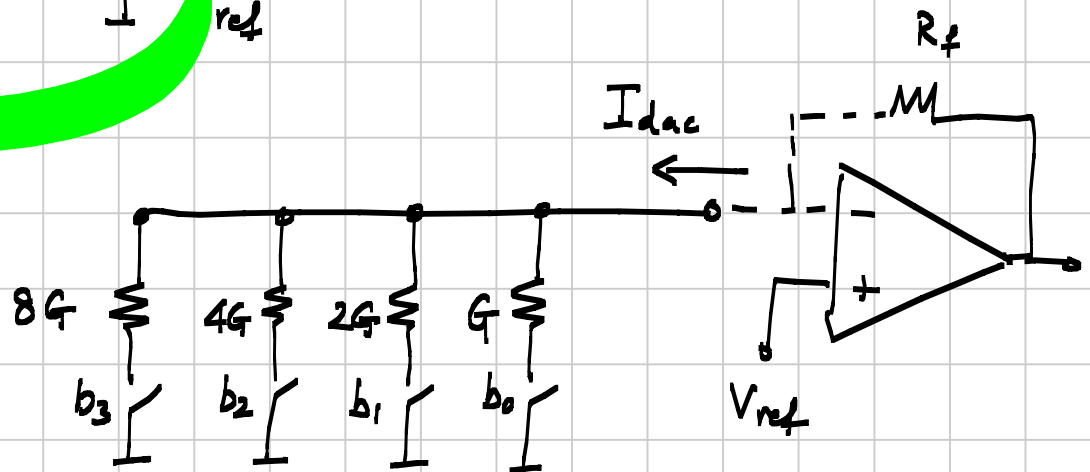
VLSI Data Conversion Circuits: Lecture 51

Note Title



$$\frac{1}{R} = G$$

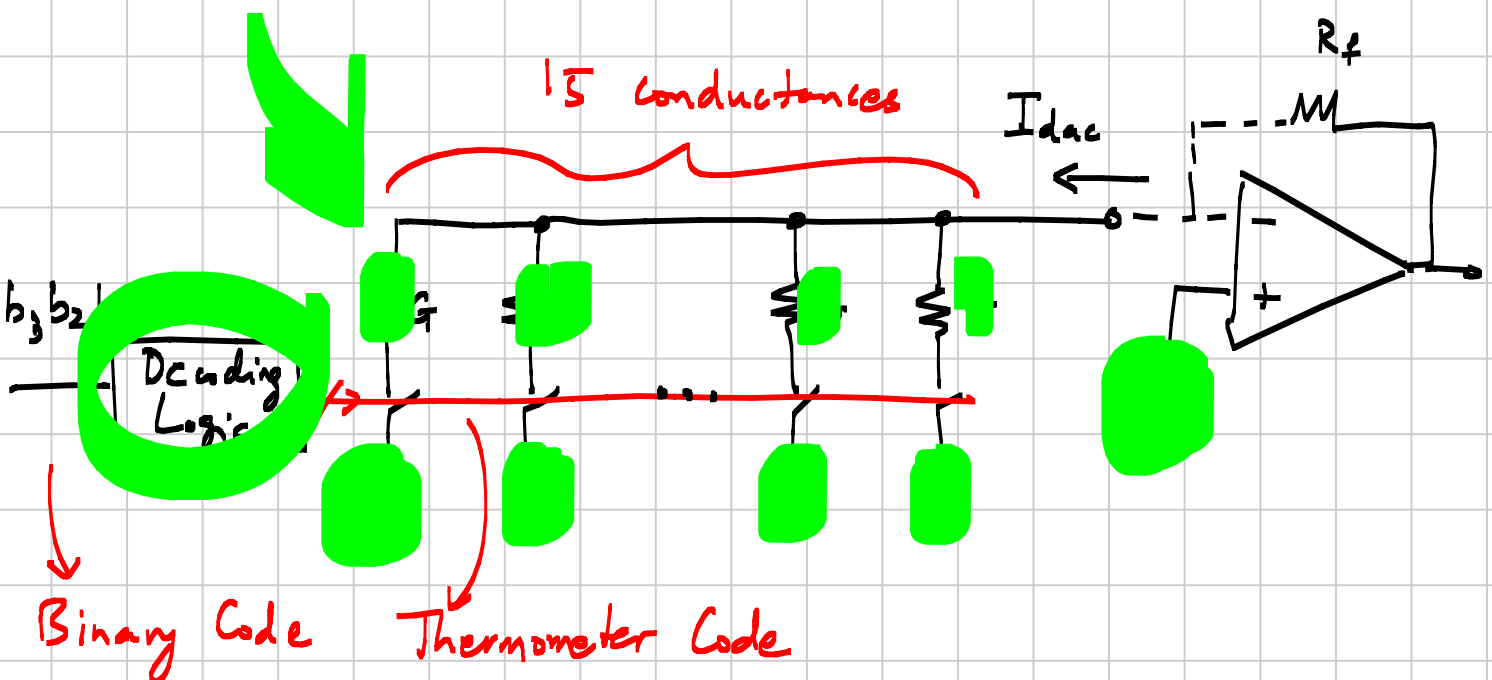
4-bit Example
(b_3, b_2, b_1, b_0)



BINARY DECODED DAC

$$I_{dac} = G V_{ref} \{ 8b_3 + 4b_2 + 2b_1 + b_0 \}$$

"Decoding" Logic is trivial



With mismatch :-

$$\begin{aligned} & \text{[redacted]} + \text{[redacted]} \\ & \text{[redacted]} + \text{[redacted]} \\ & \text{[redacted]} + \text{[redacted]} \\ & 8G + \text{[redacted]} \end{aligned}$$

$$\Delta G = N(0, \sigma_G)$$

$$\Delta G_2 = N(0, \sqrt{2} \sigma_G)$$

$$\Delta G_4 = N(0, \sqrt{4} \sigma_G)$$

$$\Delta G_8 = N(0, \sqrt{8} \sigma_G)$$

$b_3 \ b_2 \ b_1 \ b_0$
0 1 1 1

Major
Code
Transition

1 0 0 0

Idac

$$V_{ref} G \cdot \left\{ 7 + \frac{\text{[redacted]} + \text{[redacted]} + \text{[redacted]}}{G} \right\}$$

$$V_{ref} G \left\{ 7 + \frac{\sigma_G}{G} \sqrt{1 + 2 + 4} \right\}$$

$$= V_{ref} G \left\{ 7 + N\left(0, \sqrt{7} \frac{\sigma_G}{G}\right) \right\}$$

Ideal

$$\begin{aligned} & V_{ref} G \cdot \left\{ 8 + \frac{\Delta G_8}{G} \right\} \\ & = V_{ref} G \left\{ 8 + N\left(0, \frac{\text{[redacted]}}{G}\right) \right\} \end{aligned}$$

$$\text{Step Size} = G V_{ref} \left\{ 1 + N\left(0, \sqrt{15} \frac{\sigma_G}{G}\right) \right\}$$

$\left. \begin{array}{cc} 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 0 \end{array} \right\}$

$$\text{Step Size} = G V_{ref} \left\{ 1 + N\left(0, \sqrt{7} \frac{\sigma_G}{G}\right) \right\}$$

$$\sigma_{DNL} \text{ @ major code transition} \\ = N\left(0, \sqrt{15} \frac{\sigma_G}{G}\right)$$

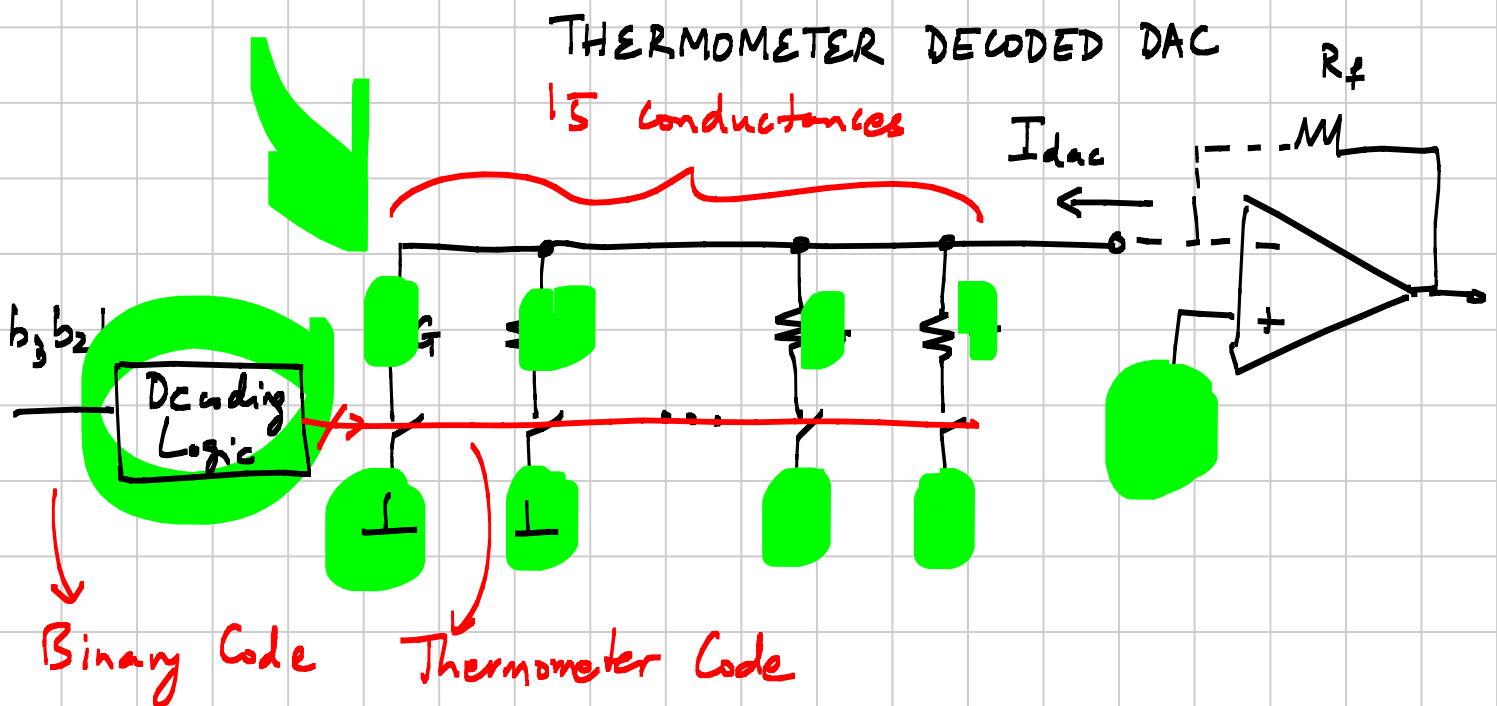
in general

$$\sigma_{DNL} = N\left(0, \sqrt{2^n - 1} \frac{\sigma_G}{G}\right)$$

@ Major code transition

$$\sigma_{INL} = N\left(0, \sqrt{2^{n-1}} \frac{\sigma_G}{G}\right)$$

@ $\underbrace{1000000}_{(n-1) \text{ zeros}}$



$$I_{DAC}[m] = V_{ref} [m G + \text{noise}]$$

$$= G V_{ref} \left[m + N\left(0, \frac{\sigma_G}{G}\right) \right]$$

$$I_{DAC}[m+1] = V_{ref} [(m+1) G + \text{noise}]$$

$$= G V_{ref} \left[m+1 + N\left(0, \frac{\sigma_G}{G}\right) \right]$$

$$I_{DAC}[m+1] - I_{DAC}[m] = G V_{ref} \left[1 + N\left(0, \frac{\sigma_q}{G}\right) \right]$$

Thermometer
DAC

$$\sigma_{DNL} = N\left(0, \frac{\sigma_q}{G}\right)$$

$$\sigma_{INL} = N\left(0, \sqrt{2^{N-1}} \frac{\sigma_q}{G}\right)$$

* INL same in both cases

* DNL

Binary

$$\sqrt{2^{N-1}} \frac{\sigma_q}{G}$$

Thermometer

$$\frac{\sigma_q}{G}$$

Ex: Want a $\sigma_{INL} = 0.1$ LSB

$$\frac{\sigma_q}{G} \approx \frac{0.1}{\sqrt{2^N}}$$

$$= 0.1$$

for a binary weighted DAC

for a thermometer
decoded DAC

Decoding logic is complex

VLSI Data Conversion Circuits : Lecture 52

* Binary Weighted

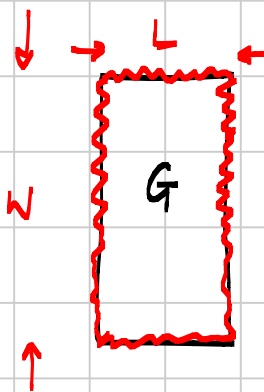
$$\sigma_{DNL} = \sqrt{2^N} \frac{\sigma_G}{G}$$

$$\sigma_{INL} = \sqrt{2^{N-1}} \frac{\sigma_G}{G}$$

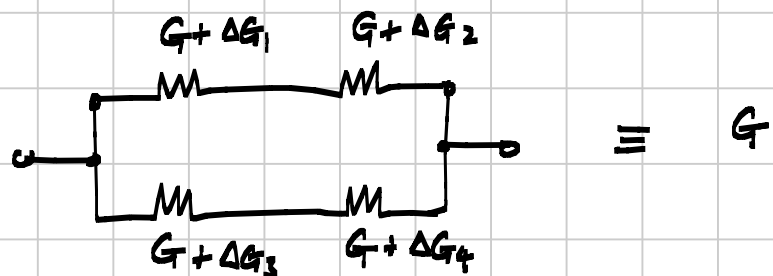
* Thermometric

$$\sigma_{DNL} = \frac{\sigma_G}{G}$$

$$\sigma_{INL} = \sqrt{2^{N-1}} \frac{\sigma_G}{G}$$



Matching $\propto \frac{1}{\sqrt{WL}}$



$$\frac{(G + \Delta G_1)(G + \Delta G_2)}{2G + \Delta G_1 + \Delta G_2}$$

$$= \frac{\frac{G}{2} \left(1 + \frac{\Delta G_1}{G}\right) \left(1 + \frac{\Delta G_2}{G}\right)}{\left(1 + \frac{\Delta G_1}{2G} + \frac{\Delta G_2}{2G}\right)} \approx \frac{G}{2} \left(1 + \frac{\Delta G_1}{2G} + \frac{\Delta G_2}{2G}\right)$$

$$\left. \begin{aligned} \frac{G}{2} + \frac{\Delta G_1}{4} + \frac{\Delta G_2}{4} \\ \frac{G}{2} + \frac{\Delta G_3}{4} + \frac{\Delta G_4}{4} \end{aligned} \right\} G \left[1 + N \left(0, \frac{1}{2} \frac{\sigma_G}{G} \right) \right]$$

Partly binary + Partly Thermometer decoding

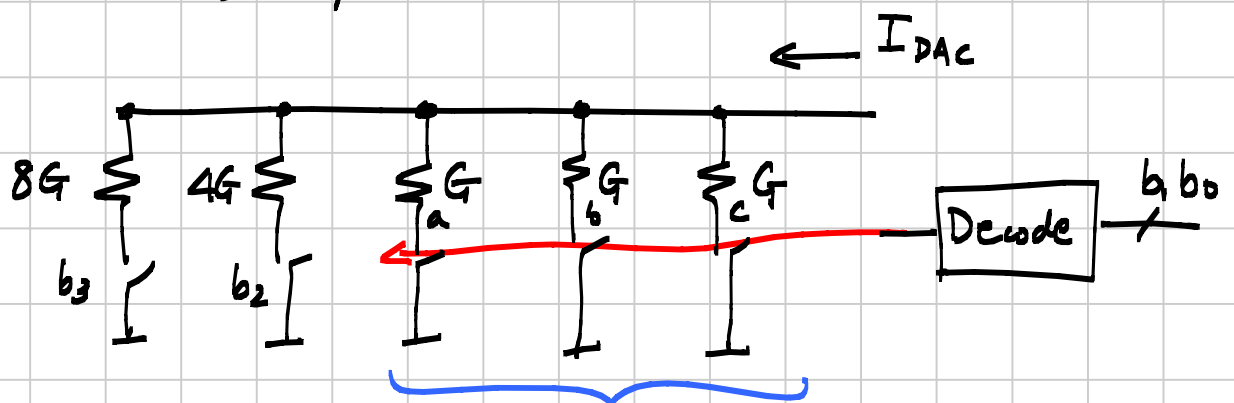
⇒ Segmentation

Example :- 4-bit example

2 bit + 2 bit segmentation

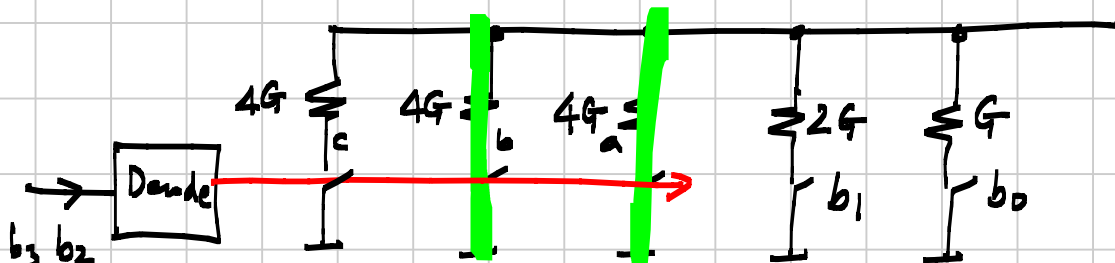
$b_3 \ b_2 \ b_1 \ b_0$
 $\underbrace{\hspace{1cm}} \quad \underbrace{\hspace{1cm}}$
 MSB LSB

BINARY Thermometer



$$0111 \rightarrow V_{ref} [7G + \Delta G_4 + \Delta G_{1a} + \Delta G_{1b} + \Delta G_{1c}]$$

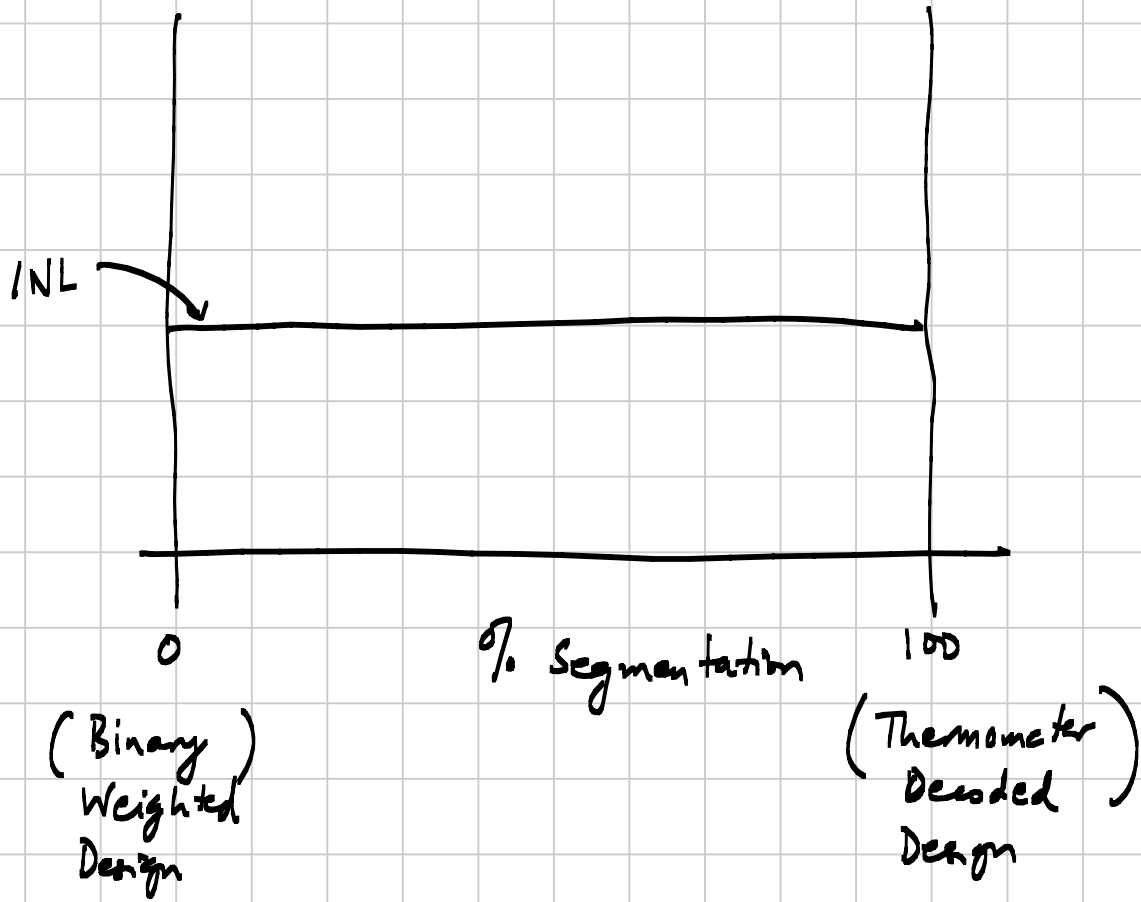
$$1000 \rightarrow V_{ref} [8G + \Delta G_2]$$



50% Segmentation
 $\frac{G}{4} \sqrt{2^{N/2}}$

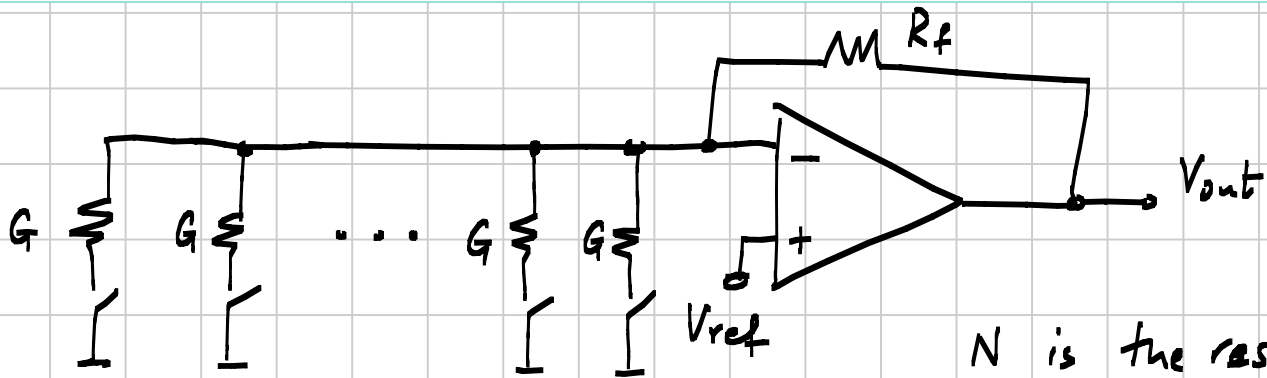
$$\left. \begin{array}{l} 0111 \quad V_{ref} [7G + \Delta G_2 + \Delta G + \cancel{\Delta G_{4a}}] \\ 1000 \quad V_{ref} [8G + \cancel{\Delta G_{4a}} + \Delta G_{4b}] \end{array} \right\} V_{ref} [G + \Delta G_{4b} + \Delta G_2 + \Delta G]$$

$$\sigma_{DNL} = \frac{\sigma_q}{q} \cdot \sqrt{7}$$



VLSI Data Conversion Circuits: Lecture 53

Note Title



N is the resolution in bits

Thermometer decoded DAC $\rightarrow 2^N - 1$ elements
 $\approx 2^N$ elements

$b_N \dots b_{M+1} \quad b_M \dots b_1 b_0$

Thermometer
Decoded

Binary
Decoded

Each step = $V_{ref} G$

Step Size of Thermometer Coded part

$$= G V_{ref} 2^M$$

Worst Case DNL

$$\left[\underbrace{1 + 2 + \dots + 2^{M-1}}_{2^M - 1} \right] G V_{ref} + \{ +\epsilon_1 + \epsilon_2 + \dots + \epsilon_{2M-1} \}$$

$0 \dots 0$

$00 \dots 0$

Therm.
Decoded

Bin.
Decoded

$$G V_{ref} \{ 2^M + \dots \}$$

$$\text{Step Size} = G V_{ref} \{ 1 + \epsilon_{2M} - [\epsilon_1 + \dots + \epsilon_{2M-1}] \}$$

$$\sigma_{DNL}^2 = \sigma_{\varepsilon_{2^M}}^2 + \sigma_{\varepsilon_1}^2 + \dots + \sigma_{\varepsilon_{2^{M-1}}}^2$$

$$\sigma_{\varepsilon_2}^2 = 2 \sigma_{\varepsilon_1}^2, \dots, \sigma_{\varepsilon_{2^{M-1}}}^2 = 2^{M-1} \sigma_{\varepsilon_1}^2$$

$$\Rightarrow \sigma_{DNL}^2 = \sigma_{\varepsilon_1}^2 + 2 \sigma_{\varepsilon_1}^2 + 4 \sigma_{\varepsilon_1}^2 + \dots + 2^M \sigma_{\varepsilon_1}^2$$

$$\sigma_{DNL}^2 = (2^{M+1} - 1) \sigma_{\varepsilon_1}^2$$

$$\sigma_{\varepsilon_1}^2 \propto \frac{1}{\text{Area}}$$

$$\Rightarrow \sigma_{DNL}^2 \propto \frac{(2^{M+1} - 1)}{\text{Area}}$$

$$\sigma_{INL}^2 \propto \frac{1}{\text{Area}}$$

$M = N \Rightarrow$ Binary DAC

$M = 0 \Rightarrow$ Thermometer DAC

$$\text{Area} \propto \frac{(2^{M+1} - 1)}{\sigma_{DNL}^2} \approx \frac{2^{M+1}}{\sigma_{DNL}^2}$$

$$\text{Area} \propto \frac{1}{\sigma_{DNL}^2}$$

Total Area of the DAC

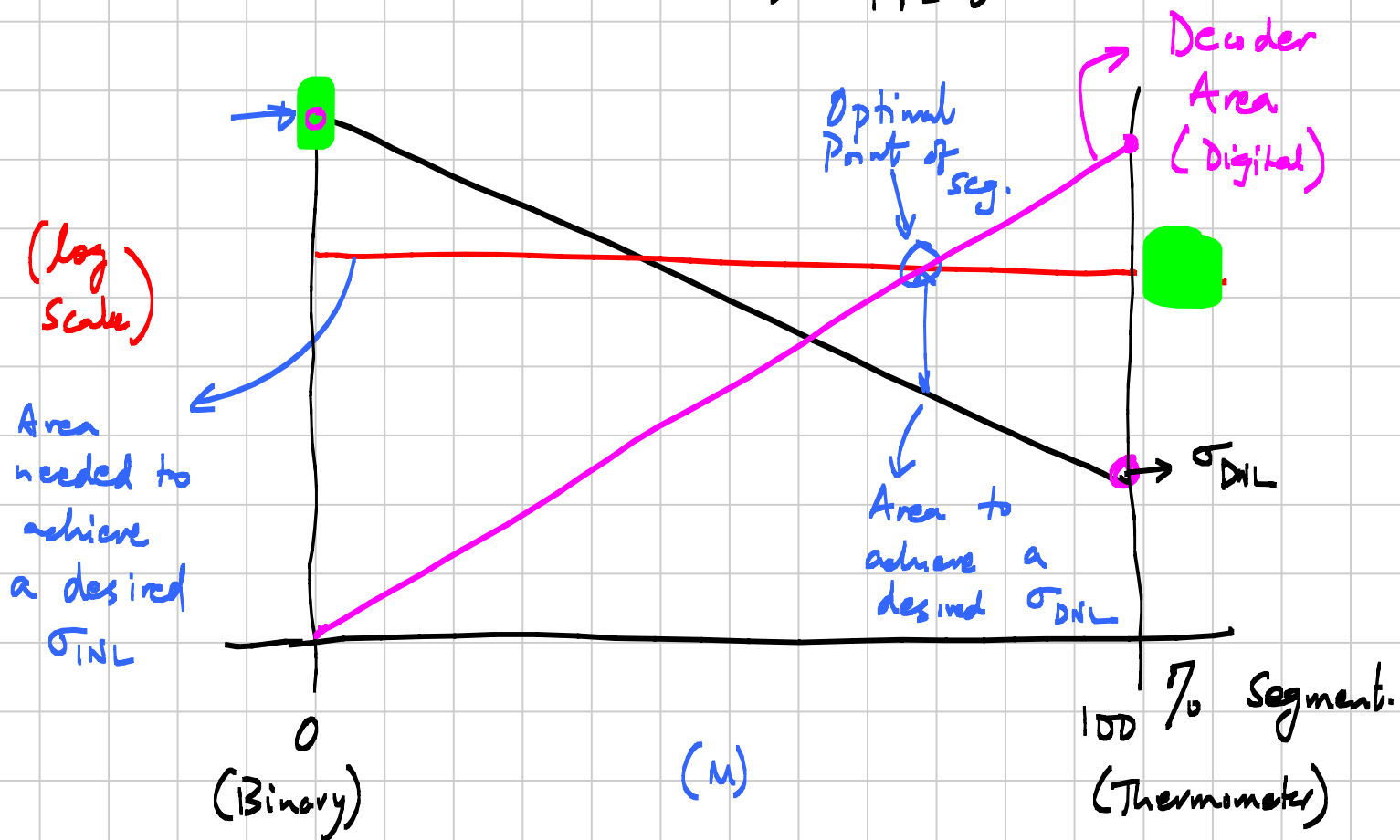
$$= \text{Area of unit elements} \rightarrow 2^N \cdot \text{Area} + \text{Area of decoder (digital)}$$

$\% \text{ Segmentation} \Rightarrow 100 \left(1 - \frac{M}{N} \right)$

No. of binarily decoded bits $\rightarrow$ (points to M)
 DAC resolution $\rightarrow$ (points to N)

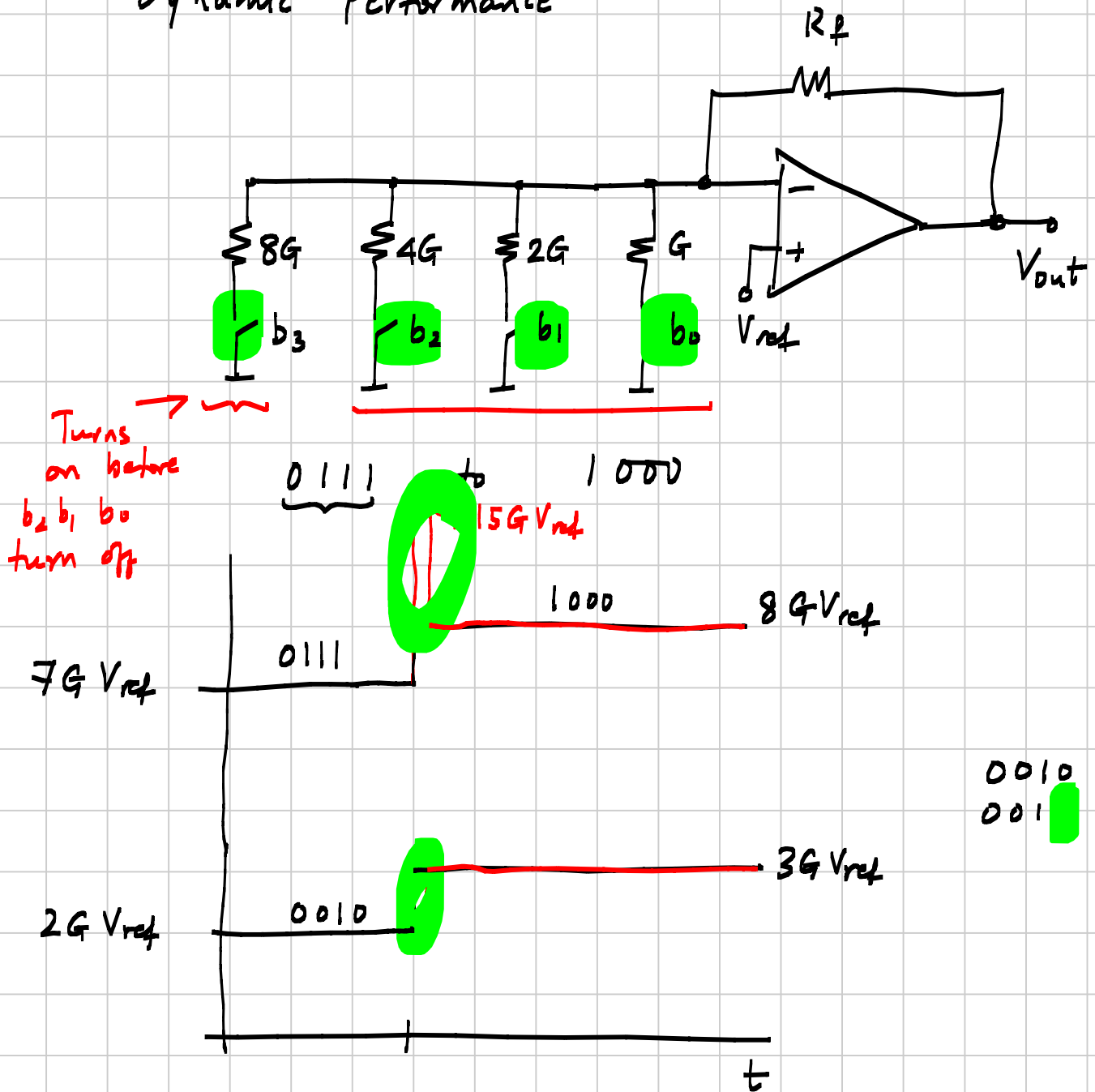
0% Segmented $\Rightarrow$ Fully binary
 $\Rightarrow M = N$

100% Segmented $\Rightarrow$ Fully thermometer
 $\Rightarrow M = 0$

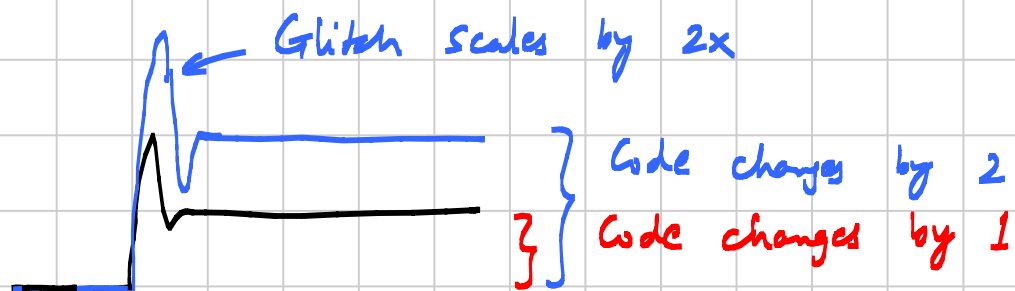
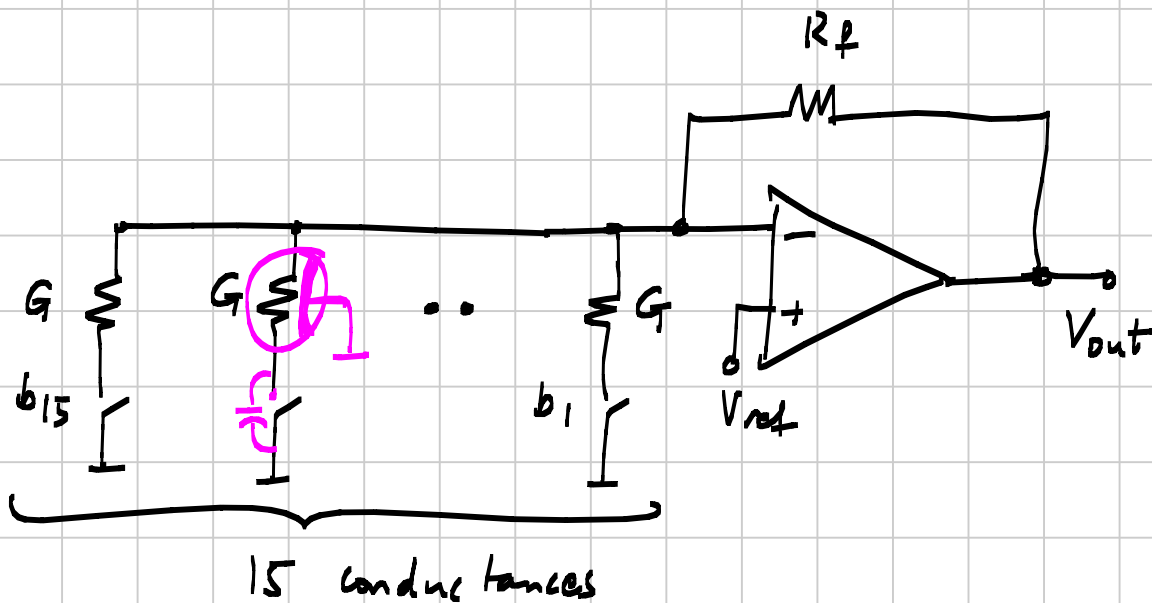


VLSI Data Conversion Circuits: Lecture 54

Dynamic Performance



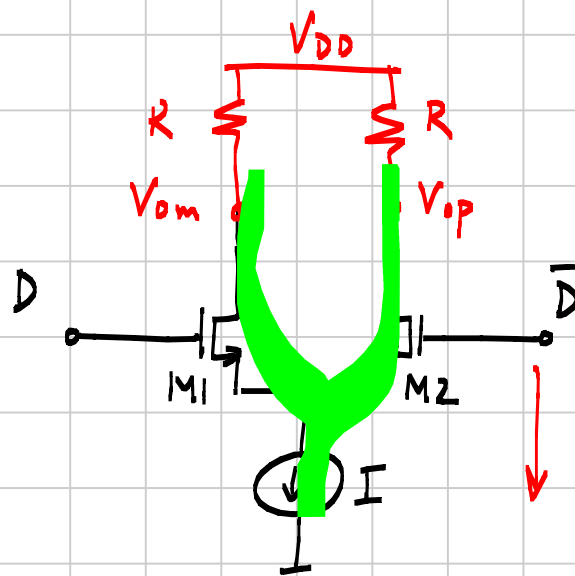
A Binary weighted DAC has significant
Dynamic nonlinearity



Dynamic performance of a thermometer decoded DAC is much better than that of a binary DAC.

All things being equal $\Rightarrow$ increased segmentation leads to better performance.

Current Steering DACs



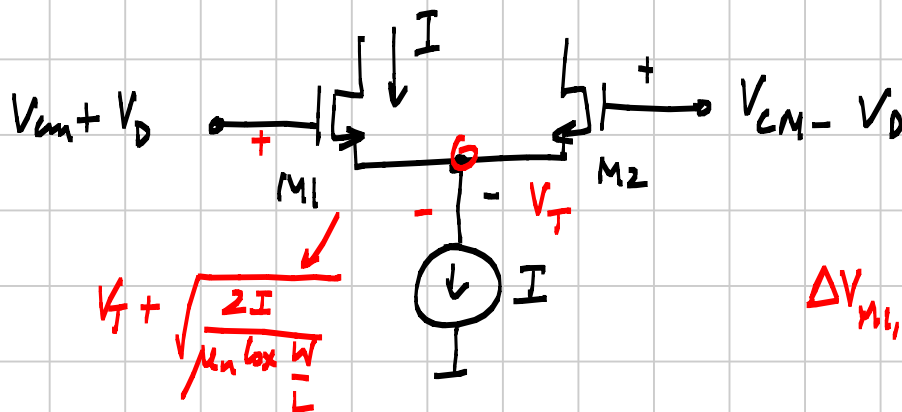
$$D = 1 \\ \bar{D} = 0$$

$$V_{om} = V_{DD} - IR \cdot D$$

$$V_{op} = V_{DD} - IR \cdot (1-D)$$

$$V_{op} - V_{om} = IR \underbrace{(2D-1)}_{\substack{\uparrow \\ -1}} = \pm IR$$

*



$$V_T + \sqrt{\frac{2I}{\mu_n C_{ox} \frac{W}{L}}}$$

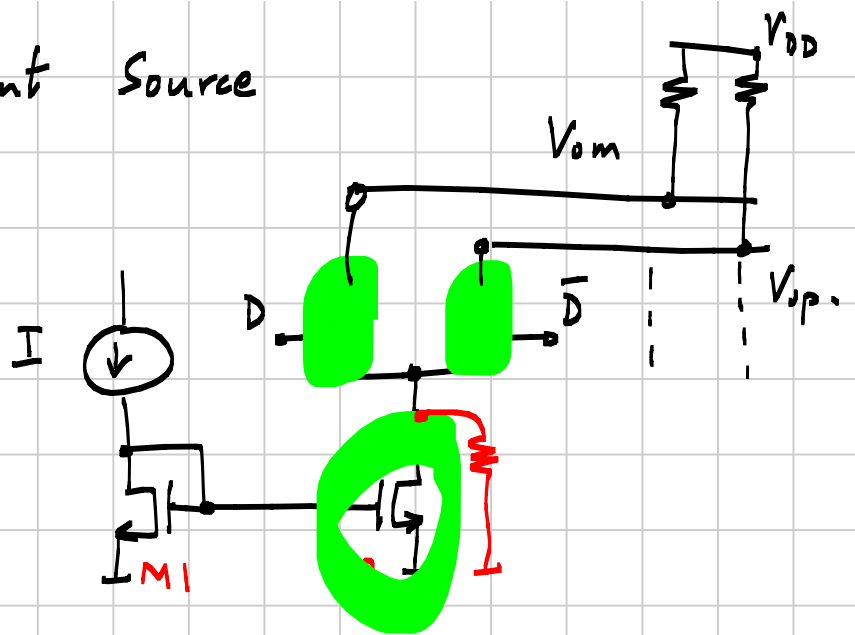
$$\Delta V_{M1, M2} = \sqrt{\frac{I}{\mu_n C_{ox} \frac{W}{L}}}$$

$$2V_D = \sqrt{\frac{2I}{\mu_n C_{ox} \frac{W}{L}}} = \sqrt{2} \cdot \Delta V_{M1, M2}$$

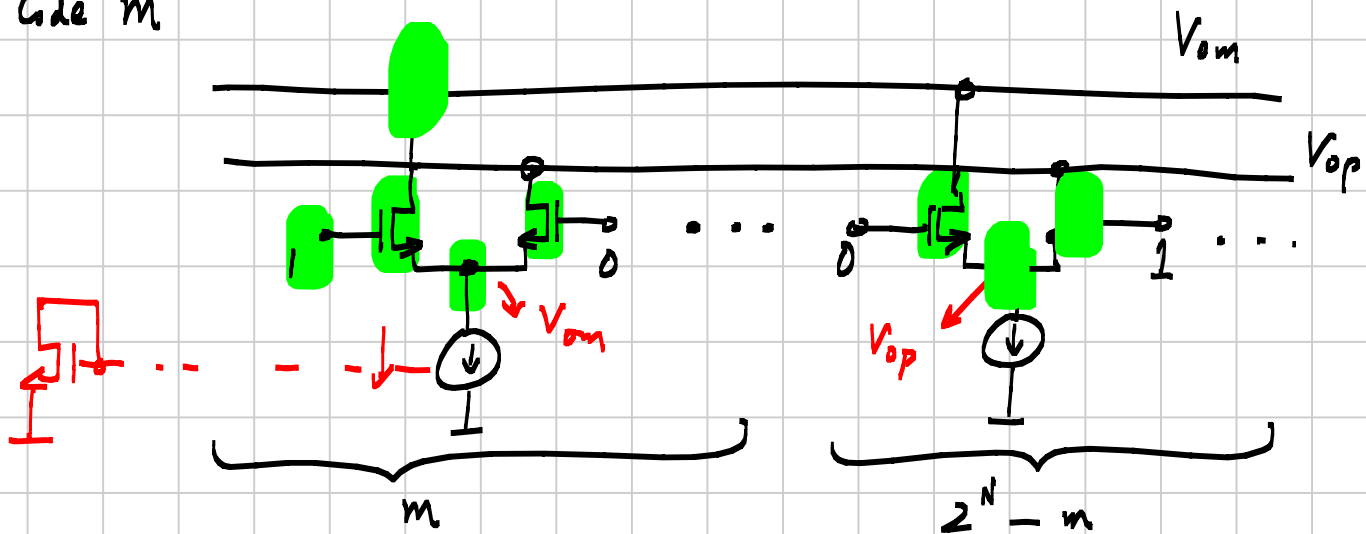
* Switching signals need not be full rail.

* Tail Current Source

Var. 0



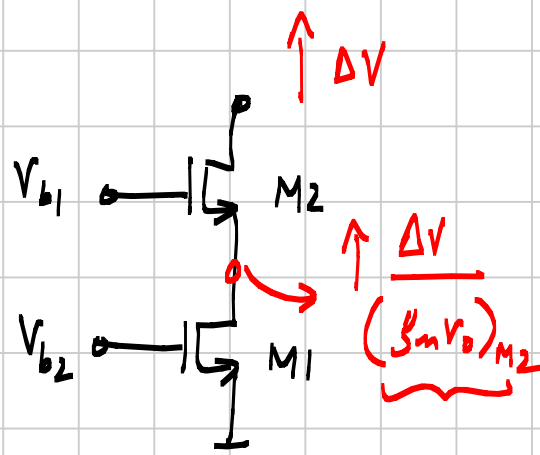
Digital Code m



$$m(I + (V_{om} - V_{gs})g_{ds}) \Rightarrow V_{om}$$

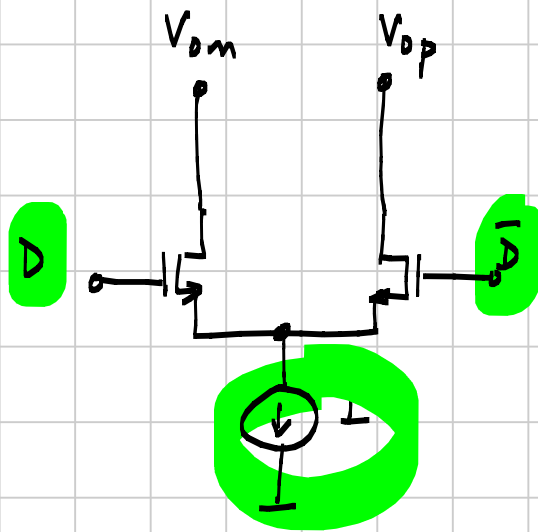
$$(2^N - m)(I + (V_{op} - V_{gs})g_{ds}) \Rightarrow V_{op}$$

$$V_{op} - V_{om} = \left[(2^N - 2m)I + V_{op}(2^N - m) - V_{om}(m) + (2m - 2^N)V_{gs} \right] R$$



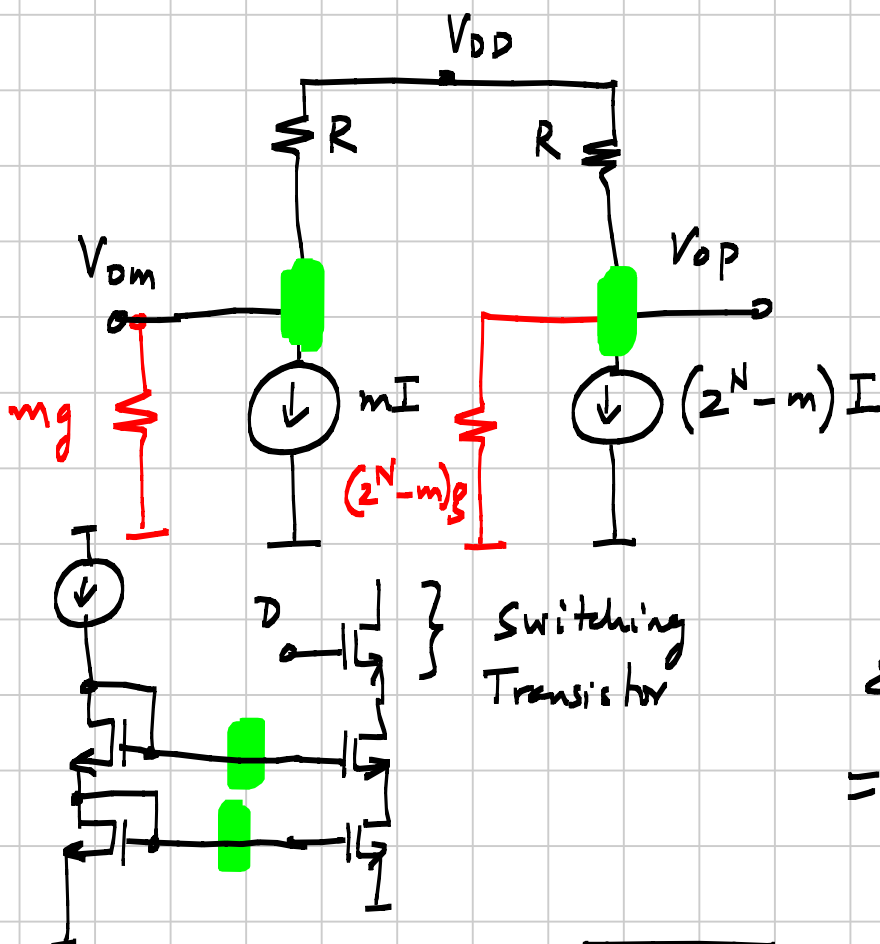
VLSI Data Conversion Circuits: Lecture 55

Note Title



For an N-bit DAC
 2^N current sources
 each current = I

Input code = m

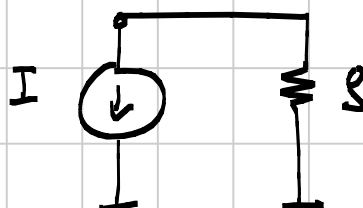


$$V_{op} = V_{DD} - (2^N - m)IR$$

$$V_{om} = V_{DD} - mIR$$

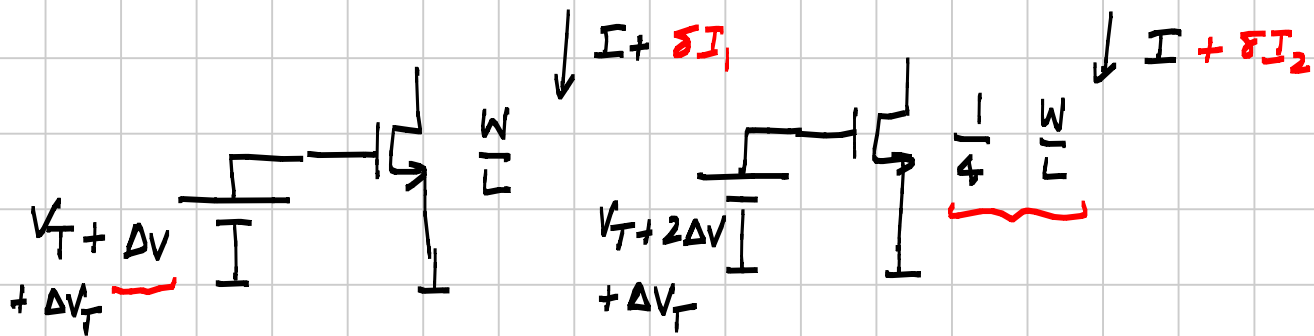
$$\begin{aligned} V_{op} - V_{om} &= 2mIR - 2^N IR \\ &= IR (2^m - 2^N) \end{aligned}$$

$$\begin{aligned} \text{Effective o/p resistance} &= O[r_o (g_m r_f)^2] \end{aligned}$$



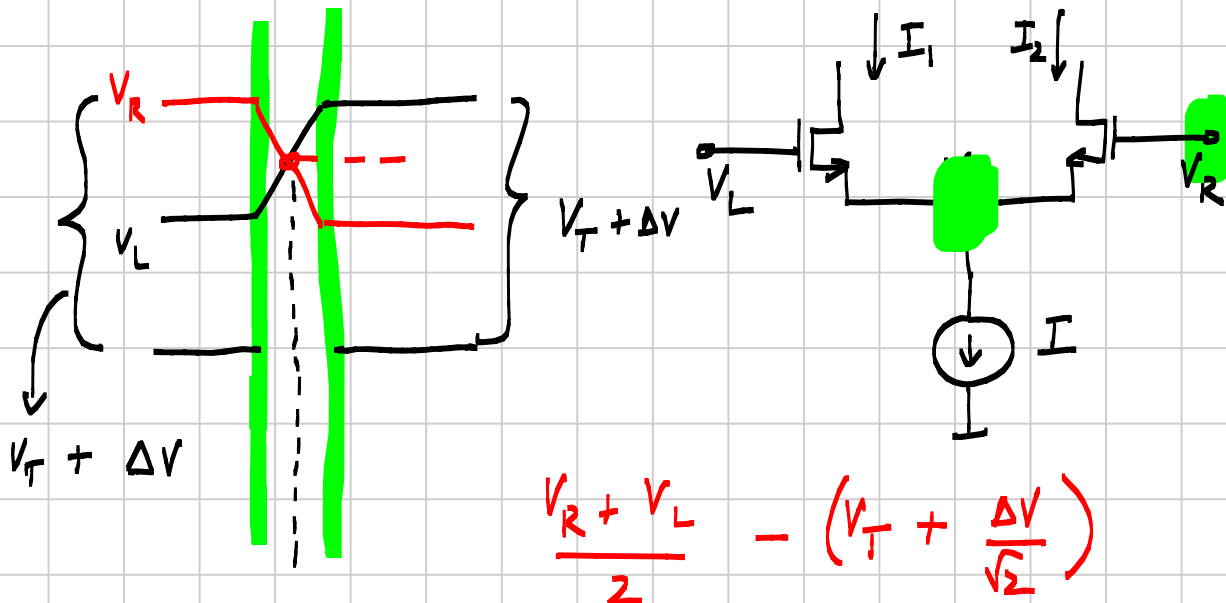
$$\frac{\Delta I_D}{I_D} = \frac{\frac{1}{2} (V_{GS} - V_T)^2 \cdot \Delta \beta}{\frac{1}{2} \beta (V_{GS} - V_T)^2} - \frac{2 I_D}{(V_{GS} - V_T)} \frac{\Delta V_T}{I_D}$$

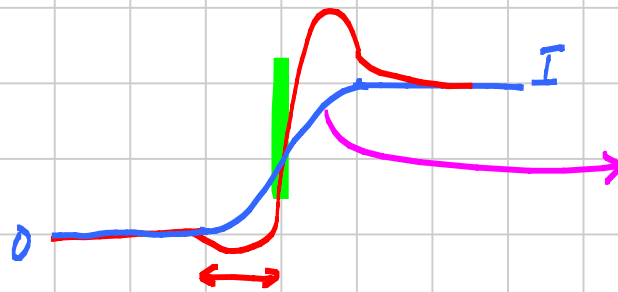
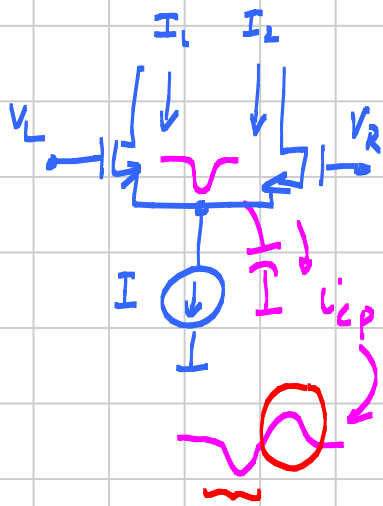
$$\frac{\Delta I_D}{I_D} = \frac{\Delta \beta}{\beta} - \frac{2 \Delta V_T}{(V_{GS} - V_T)}$$



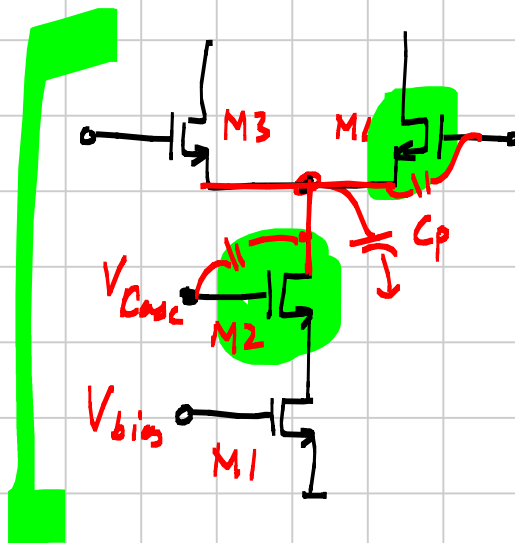
$$\sigma_{\frac{\Delta I_D}{I_D}}^2 = \frac{A_\beta^2}{WL} + \frac{4 A_{V_T}^2}{(V_{GS} - V_T)^2 WL}$$

$$\sigma_{\Delta V_T} = \frac{A_{V_T}}{\sqrt{WL}} \quad A_{V_T} \Rightarrow m V_\mu$$





Assuming no parasitic capacitances



* Keep C_p as small as possible

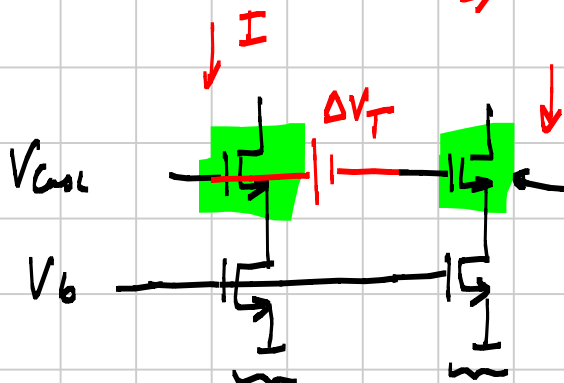
$$C_{db,M2} + C_{gs,M2}$$

$$C_{sb,M3} + C_{gs,M3}$$

+ Routing capacitance

$\Rightarrow$ M3, M4, M2 as small as possible

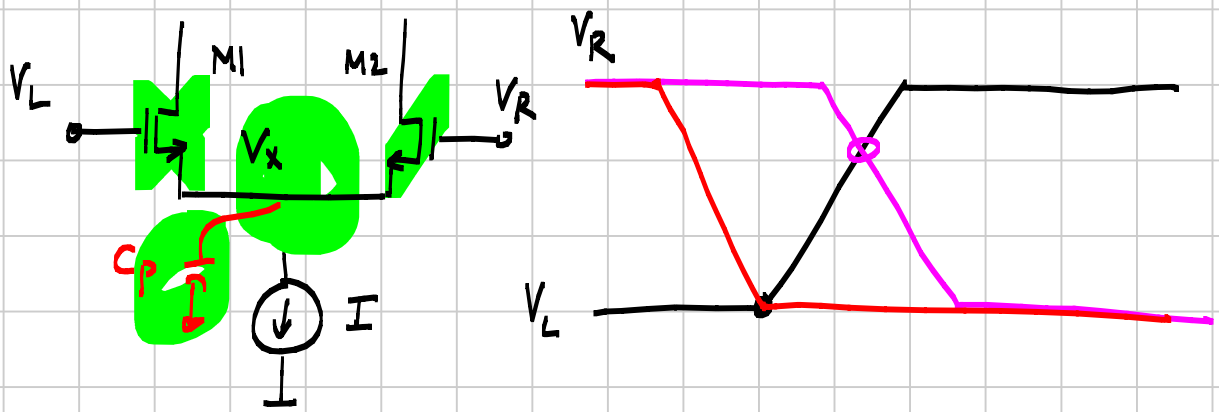
$\Rightarrow$ Smallest L for M2, 3, 4



$$\delta I \approx \frac{\Delta V_T}{r_o}$$

$$\Delta V_T \approx \Delta V_T \cdot g_m$$

$$\frac{\Delta V_T}{r_o}$$



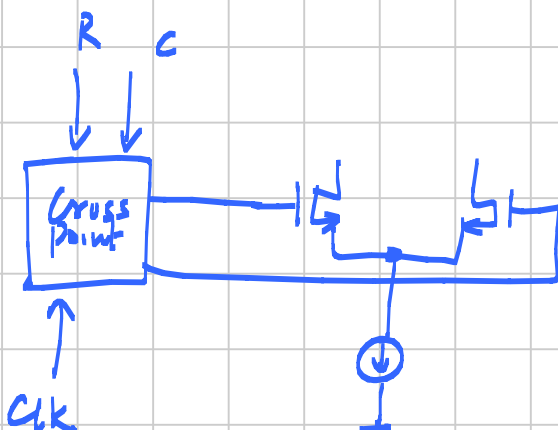
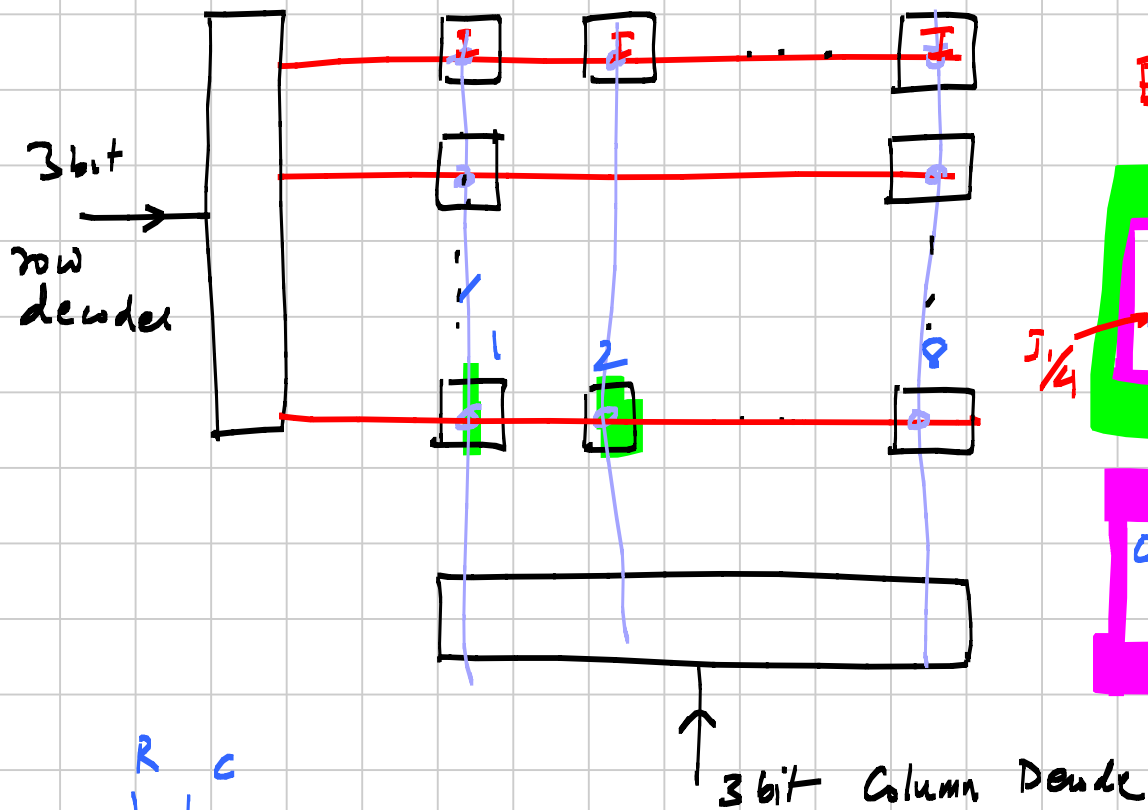
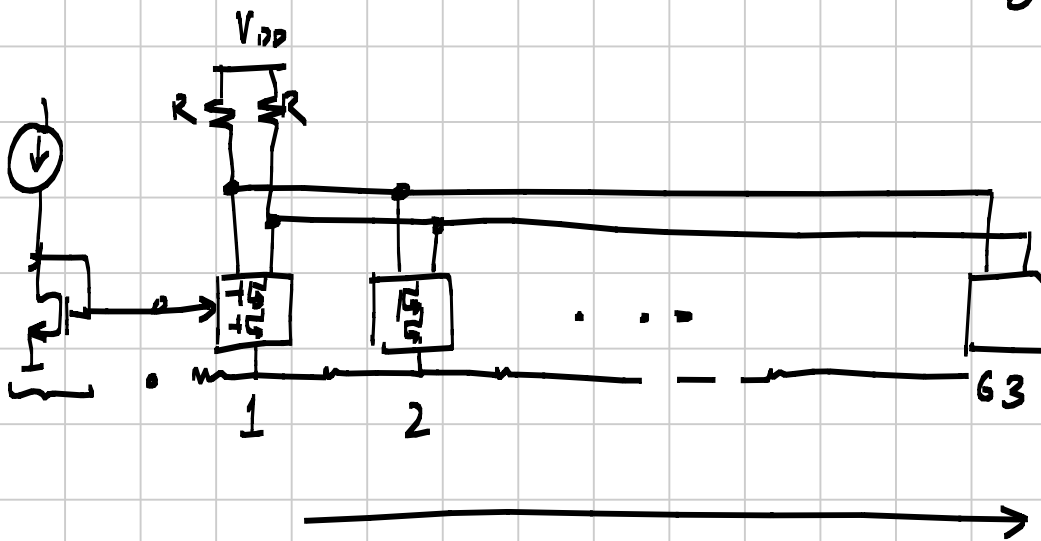
- * If M_1 & M_2 are OFF Simultaneously,
leads to large glitches $\rightarrow$ poor dynamic linearity
- * For good dynamic nonlinearity,
keep M_1 & M_2 on during the transition
so that the voltage swing at V_x is as small
as possible.

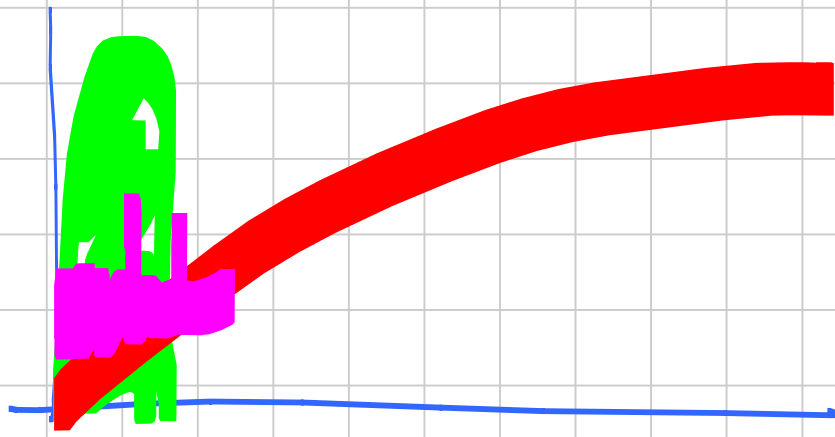
Systematic DAC Design

- * Choose $\frac{\sigma_{\Delta I}}{I}$ based on DNL/INL specs,
and segmentation strategy.
- * Choose cascode & switch devices to be
as small as possible.

Eg. 10 bit DAC

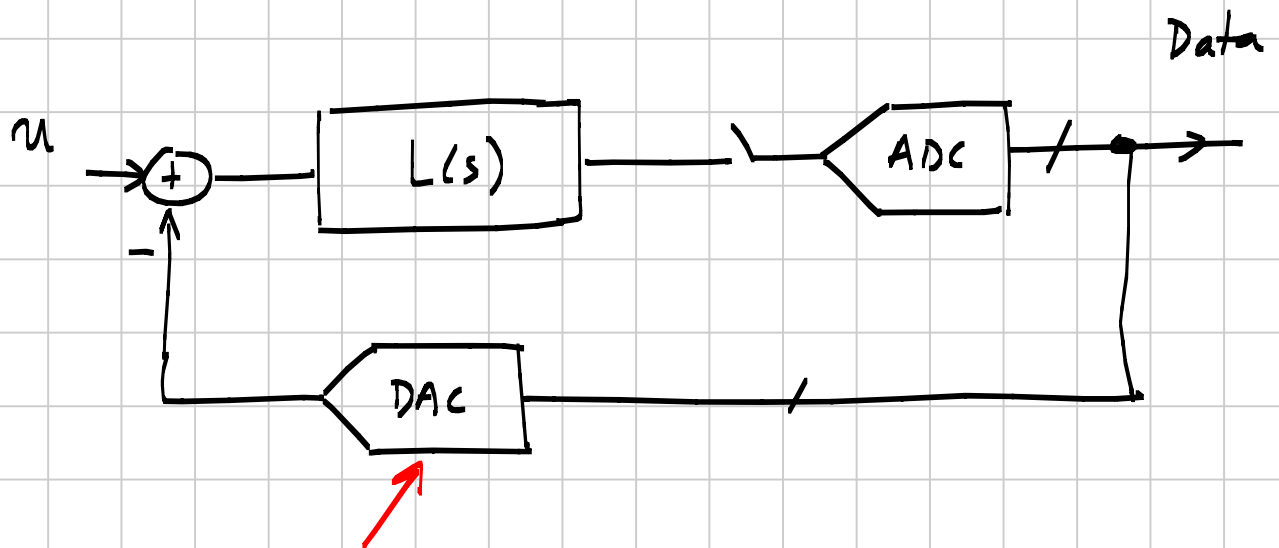
6 thermometers + 4 binary





VLSI Data Conversion Circuits : Lecture 57

Note Title



Mismatch in the DAC elements

in multibit $\Sigma\Delta$ modulators

- * For the same NTF,
 - $\rightarrow$ SNR $\uparrow$
 - $\rightarrow$ MSA $\uparrow$
 - * In a CTDSM, Jitter Noise $\downarrow$
 - * Reduced effect of loop filter nonlinearity
- } Multi-bit operation enables more aggressive NTFs

VLSI Data Conversion Circuits

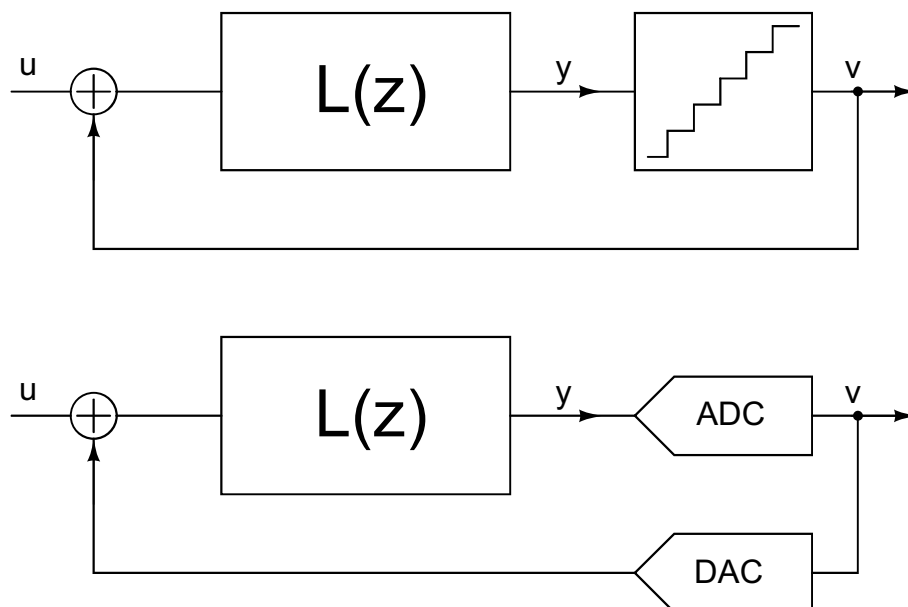
Shanthi Pavan

Department of Electrical Engineering
Indian Institute of Technology, Madras

April 18, 2011

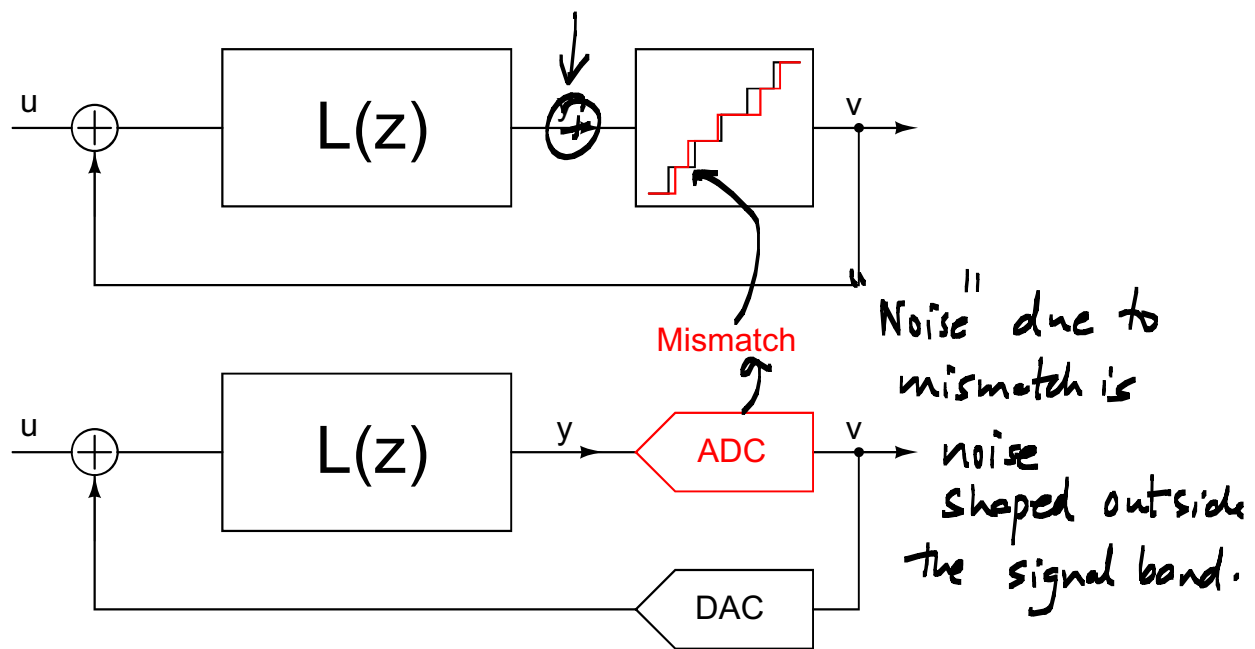
Outline

DAC Nonlinearity in $\Delta\Sigma$ Modulators



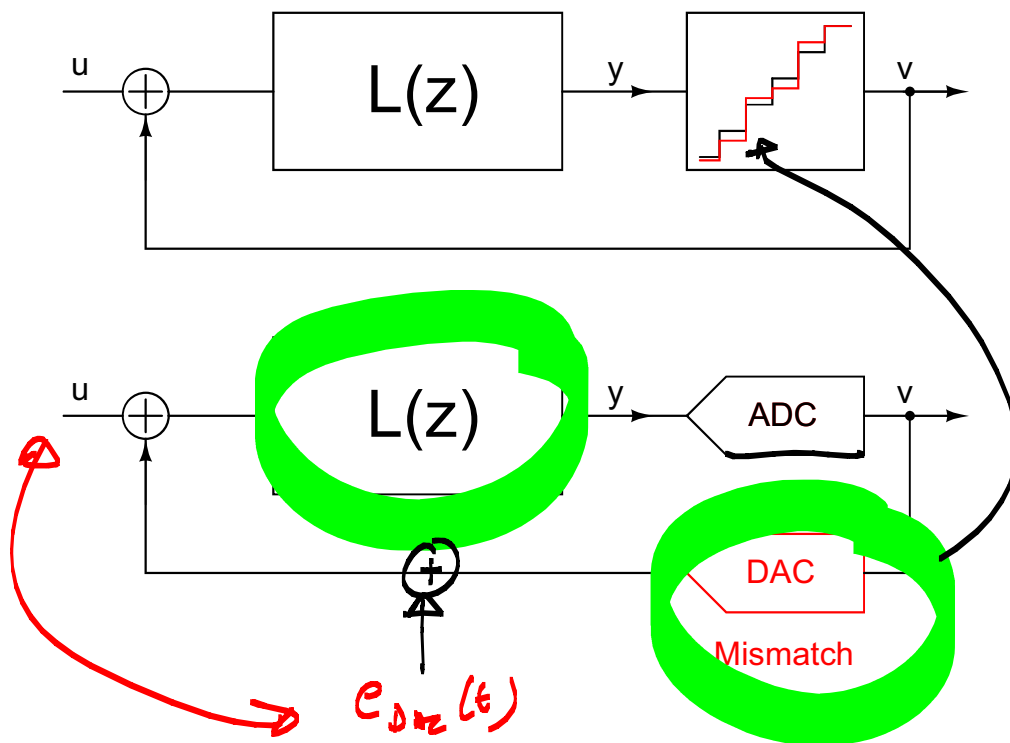
- Quantizer = ADC & DAC in cascade

DAC Nonlinearity in $\Delta\Sigma$ Modulators



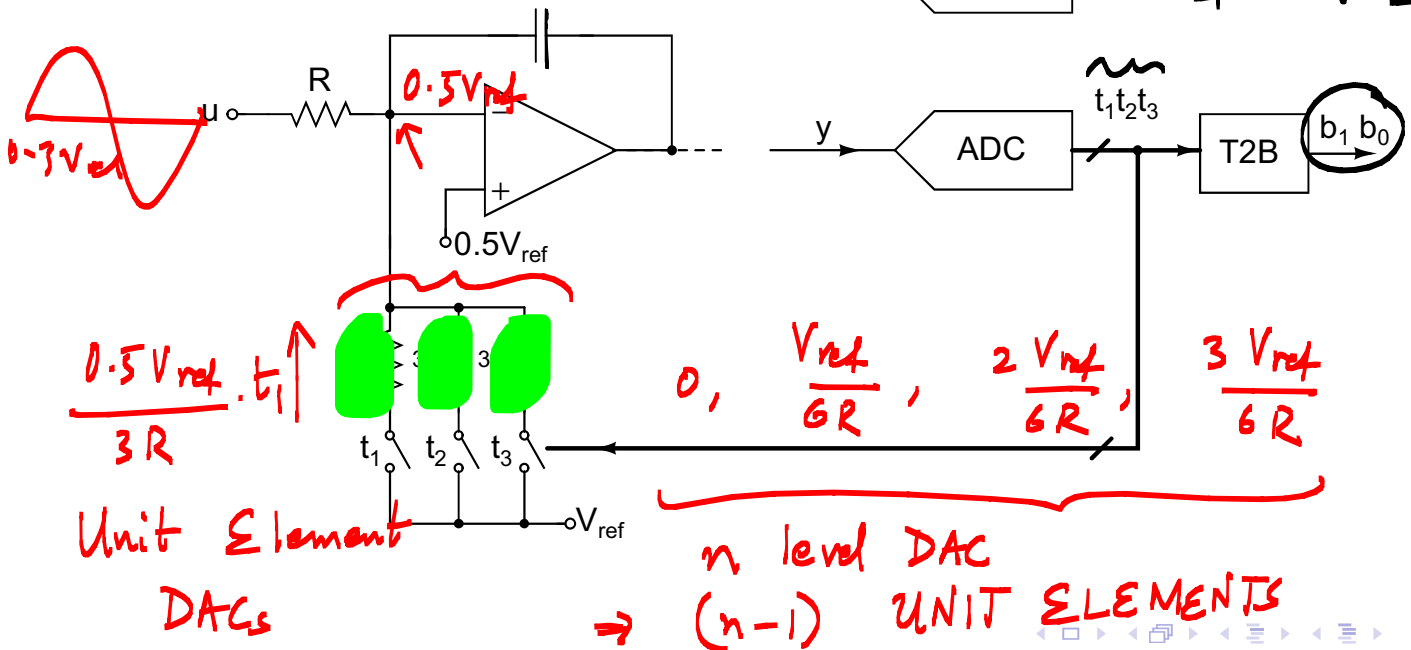
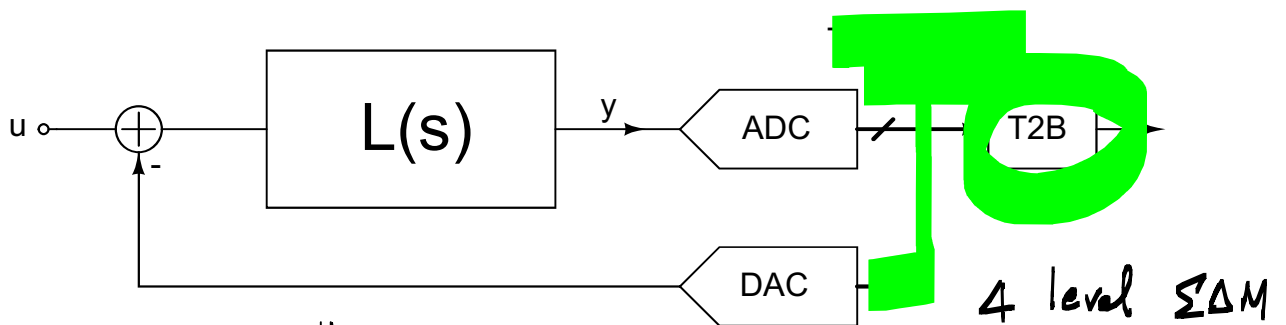
- Device mismatch in the (flash) ADC causes thresholds to move from their ideal values
- Equivalent to injecting an error at the quantizer input - shaped by the loop

DAC Nonlinearity in $\Delta\Sigma$ Modulators

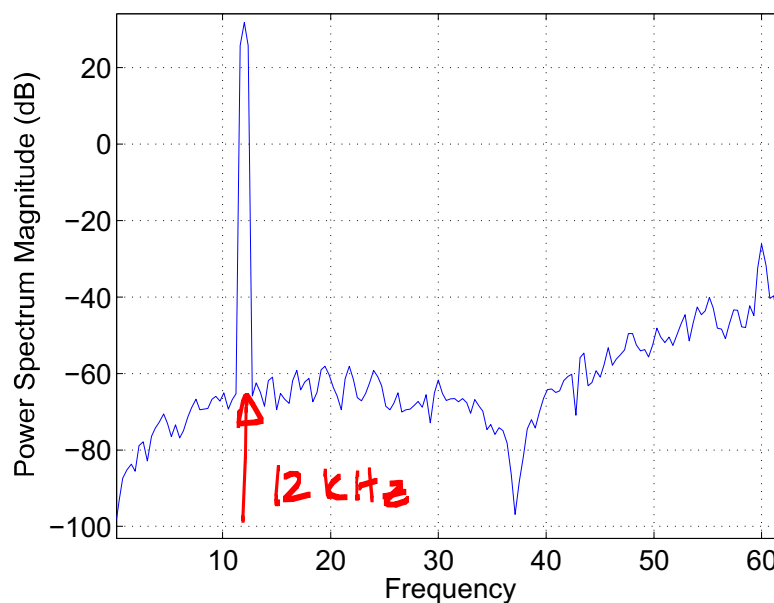


- Device mismatch in the DAC causes levels to move from their ideal values
- Equivalent to injecting an error at the modulator input

DAC Nonlinearity in $\Delta\Sigma$ Modulators



Example Modulator : without mismatch

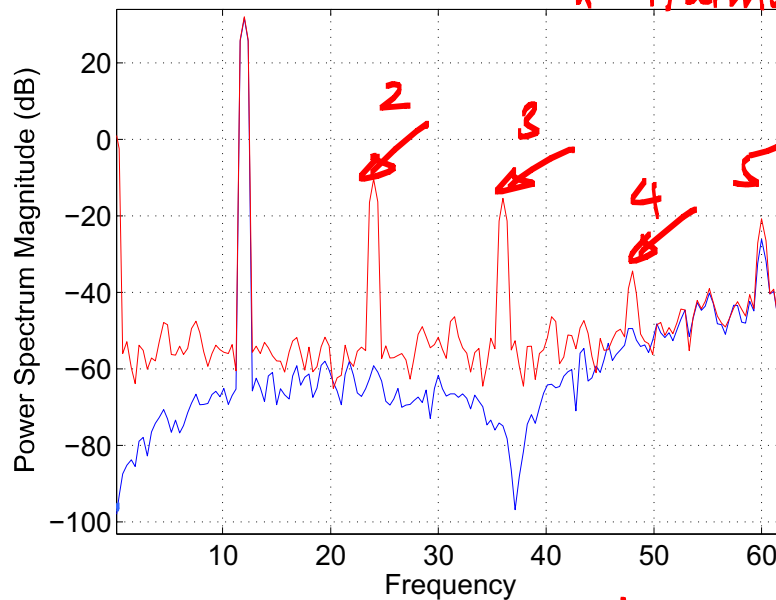


$$f_s = 3.072 \text{ MHz}$$

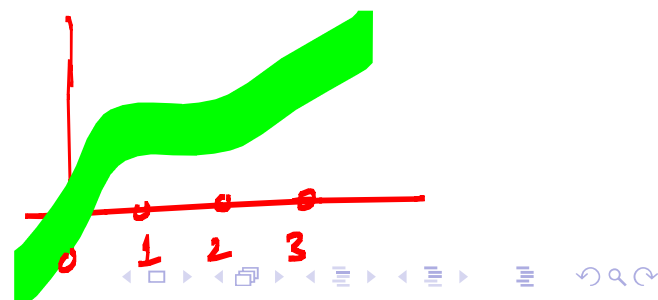
- Third Order NTF, Optimized zeros
- 4-level quantizer, OSR = 32
- -3 dBFS input

Modulator with 5% random mismatch in DAC elements

* Noise floor increases
* Harmonic distortion

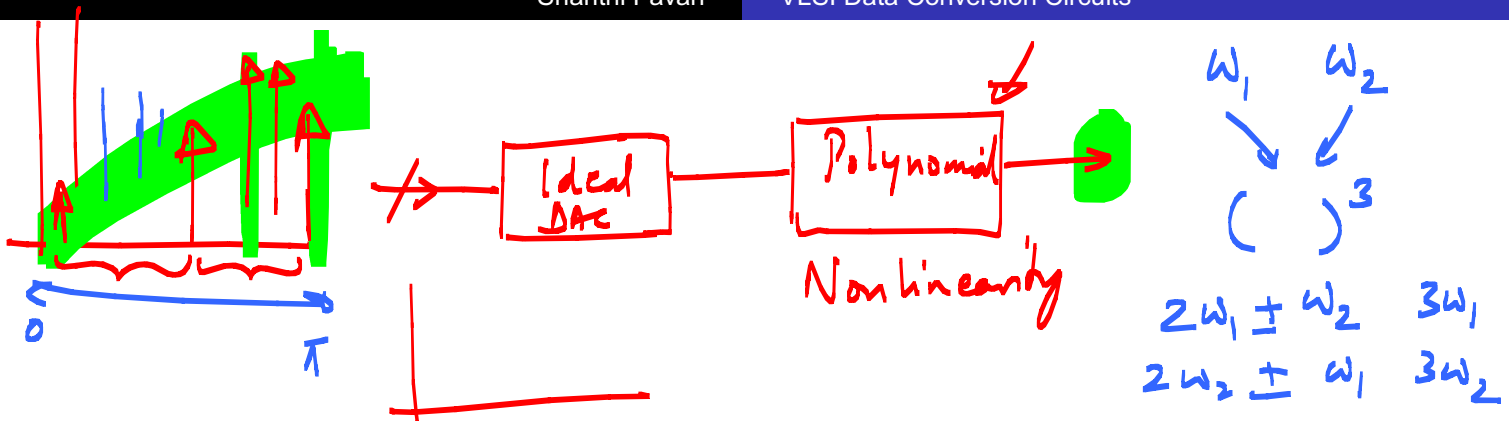


• Oops ! What happened ?

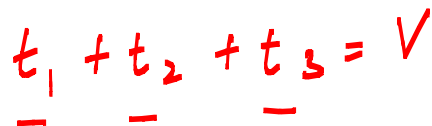


Shanthi Pavan

VLSI Data Conversion Circuits

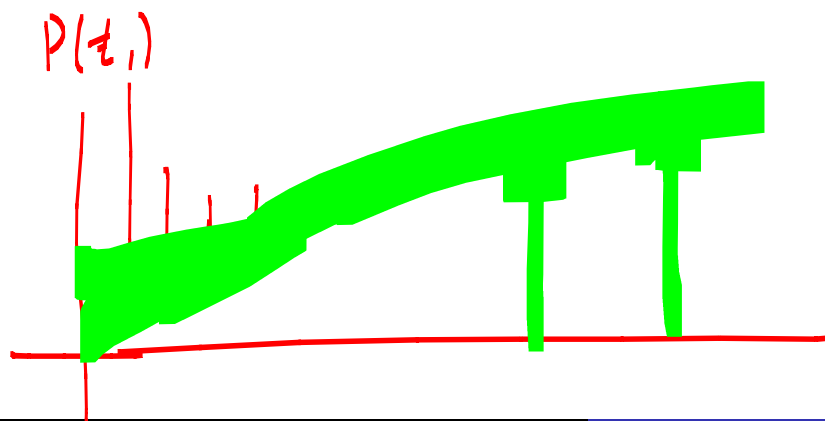
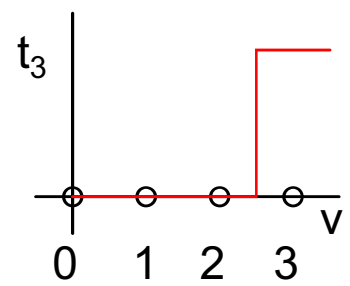
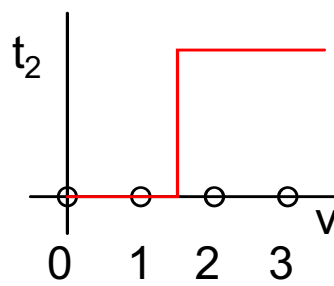
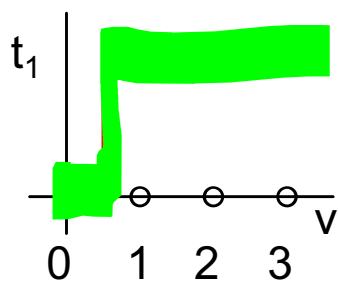


DAC Nonlinearity in $\Delta\Sigma$ Modulators

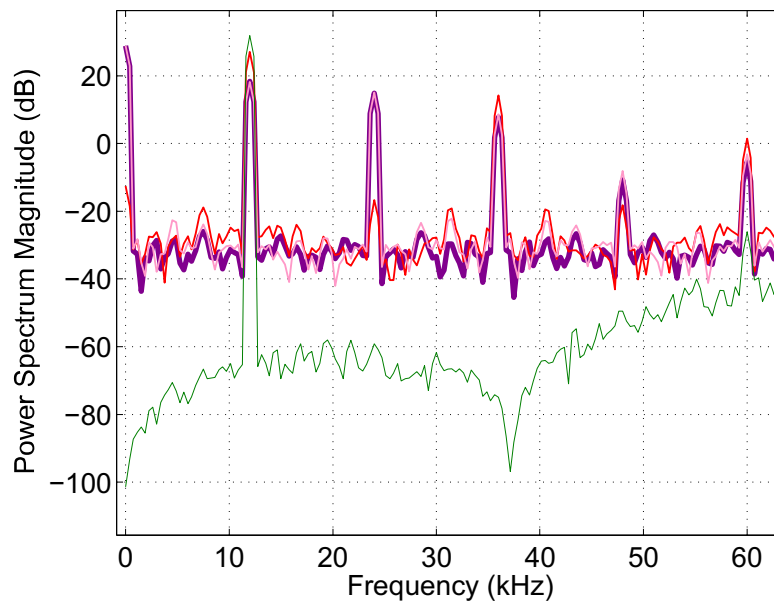


- $I_{DAC} = \frac{V_{ref}}{6R} (t_1 + t_2 + t_3)$

How are t_1 , t_2 and t_3 related to v ?



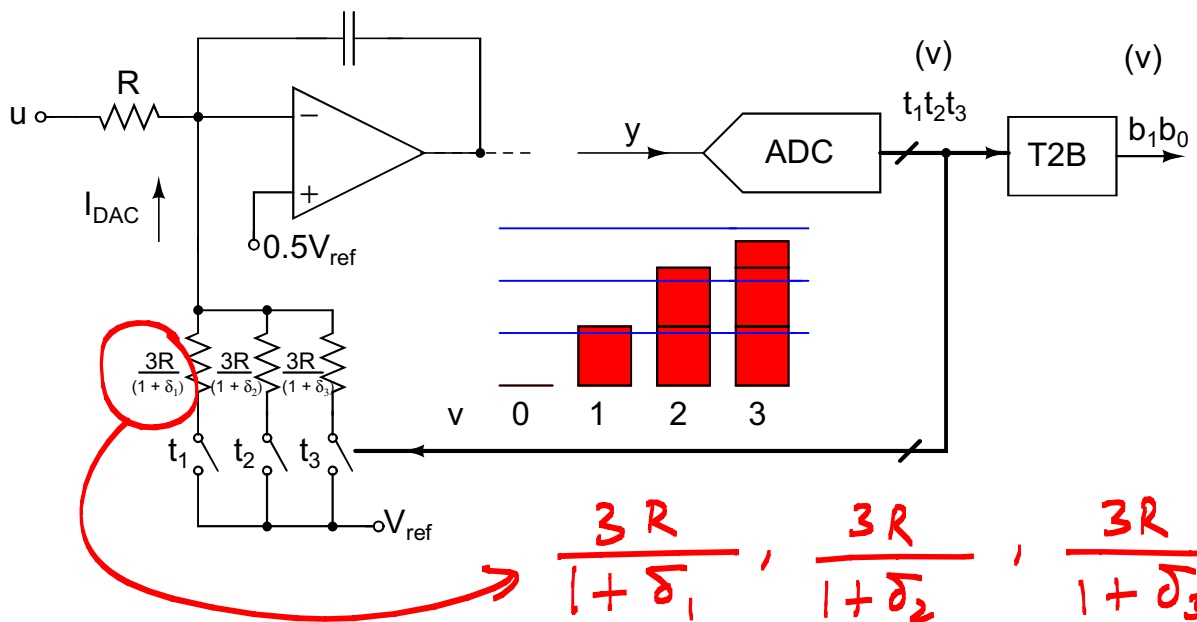
PSDs of t_1, t_2, t_3 and v



$$V = \text{[redacted]} + \alpha t_1 + \beta t_2 + \gamma t_3$$

Recall - $v = t_1 + t_2 + t_3$
 $\Rightarrow \underbrace{PSD(v)} = \underbrace{PSD(t_1 + t_2 + t_3)}$

With mismatch



- $$I_{DAC} = \frac{V_{ref}}{6R} [t_1(1+\delta_1) + t_2(1+\delta_2) + t_3(1+\delta_3)]$$

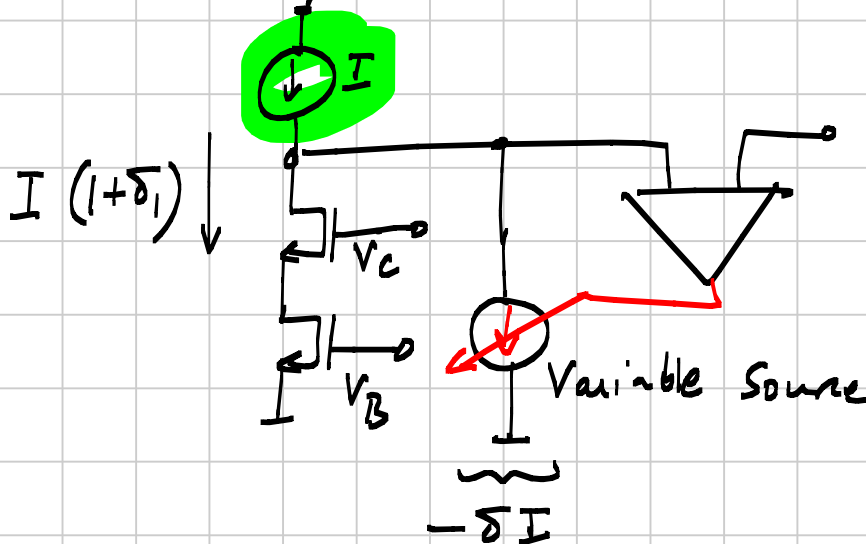
Not known

$$\delta_1, \delta_2, \delta_3$$

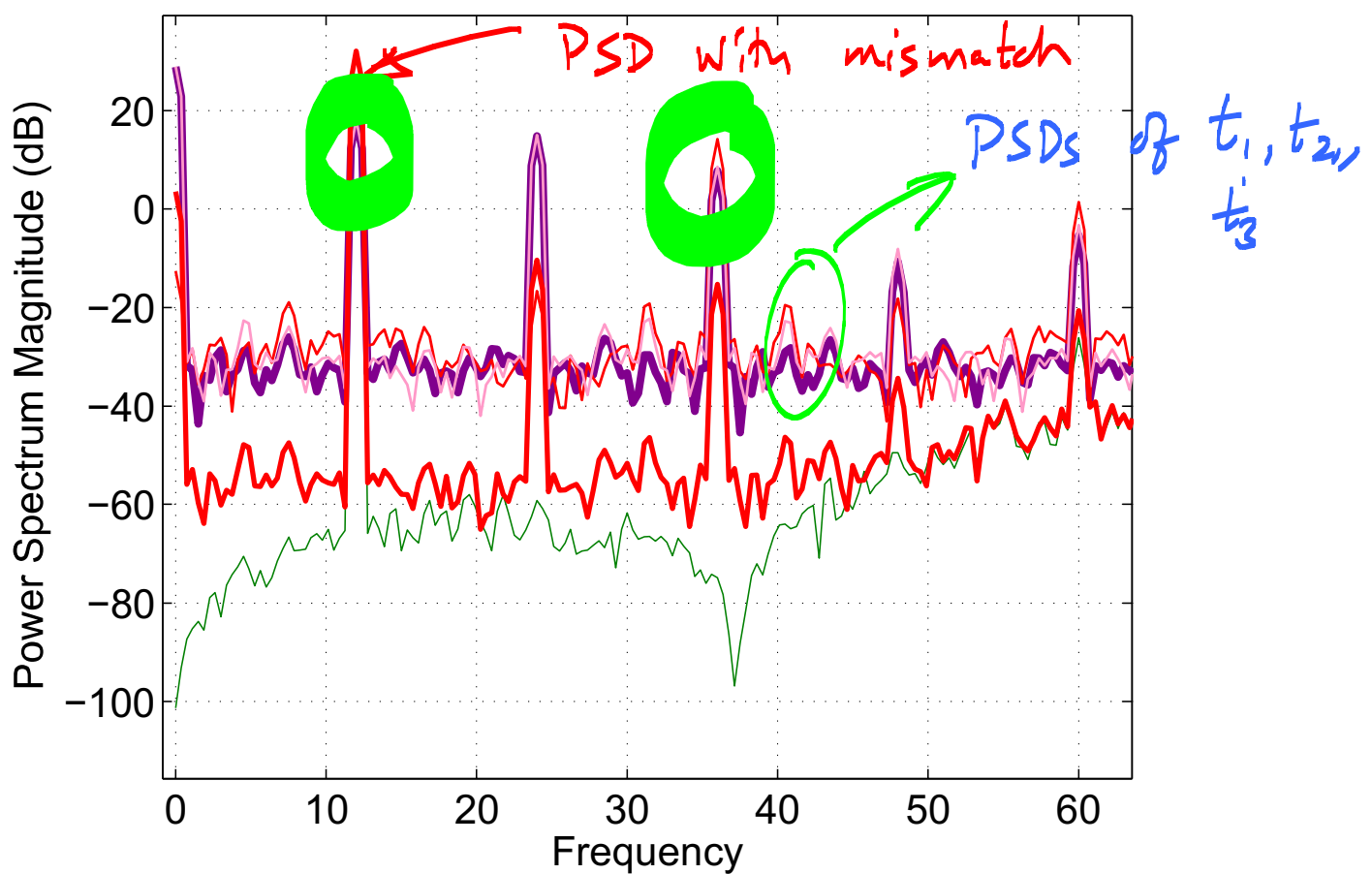
* Calibration

→ Measure the mismatch between unit elements (UE)

→ Vary the UE so that they are all equal



PSDs of I_{DAC} with and without mismatch



Mismatch “Fixing”

Basic Idea

- Conventionally, each t_i is nonlinearly dependent on v
- Each t_i waveform has lots of inband noise and harmonic distortion
- Without mismatch, all these noise and distortion components **precisely** cancel
- With mismatch - imperfect cancellation leading to distortion and inband noise
- Solution : Make each “drive sequence” a linear function of v
 t_1, t_2, t_3

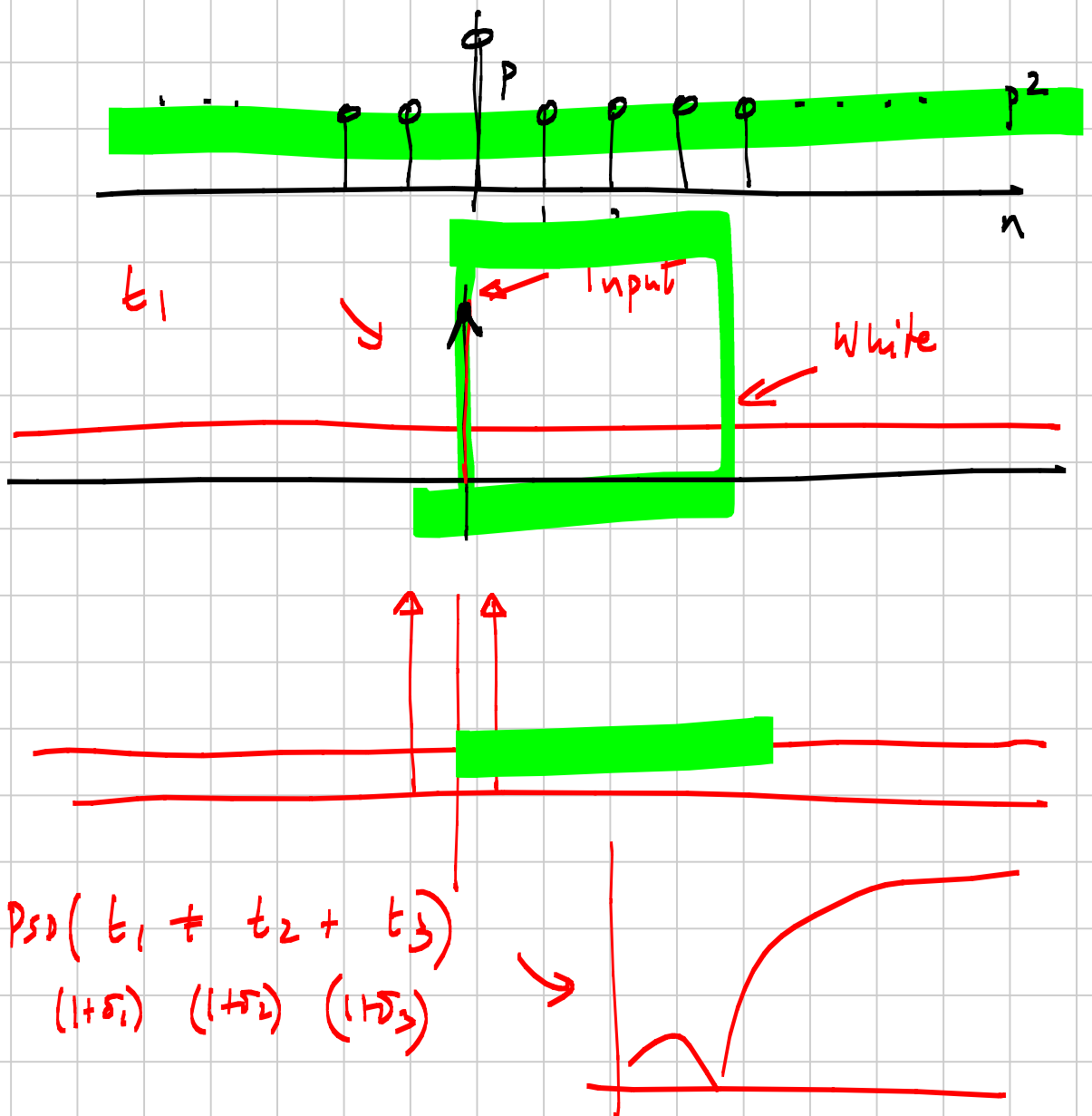
$$E(t_i) = p$$

$$p = \frac{V}{(n_{lev} - 1)}$$

$$\begin{aligned} t_m t_n &= 1 \quad \text{with prob. } p^2 \\ &= 0 \quad \text{with prob. } (1-p^2) \end{aligned}$$

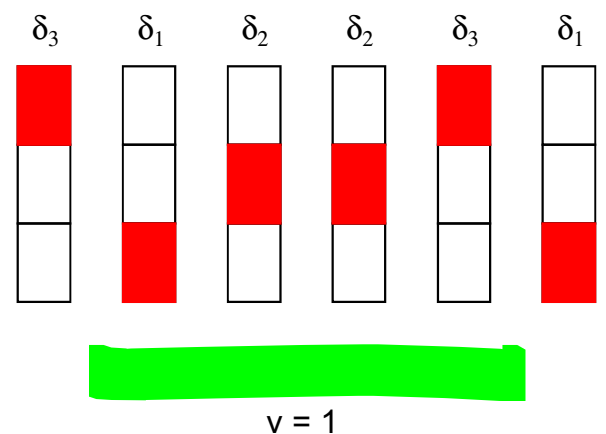
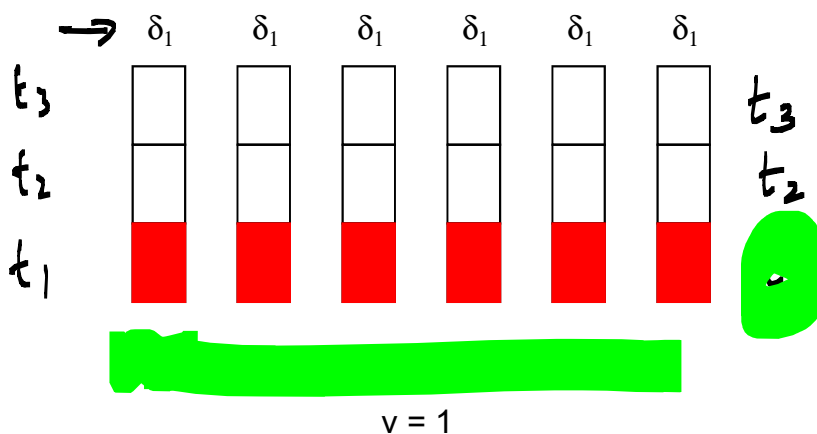
$$R_{tt}(m, n) = p^2, \quad m \neq n$$

$$R_{tt}(m, n) = p, \quad m = n$$



Dynamic Element Randomization

$$\overline{t_1}, \overline{t_2}, \overline{t_3} \propto V$$



$$t_1 + t_2 + t_3 = V$$

$$t_1 + t_2 + t_3 = V$$

- Randomly choose v elements out of $(nlev - 1)$.

-

$$t_1 = 1$$

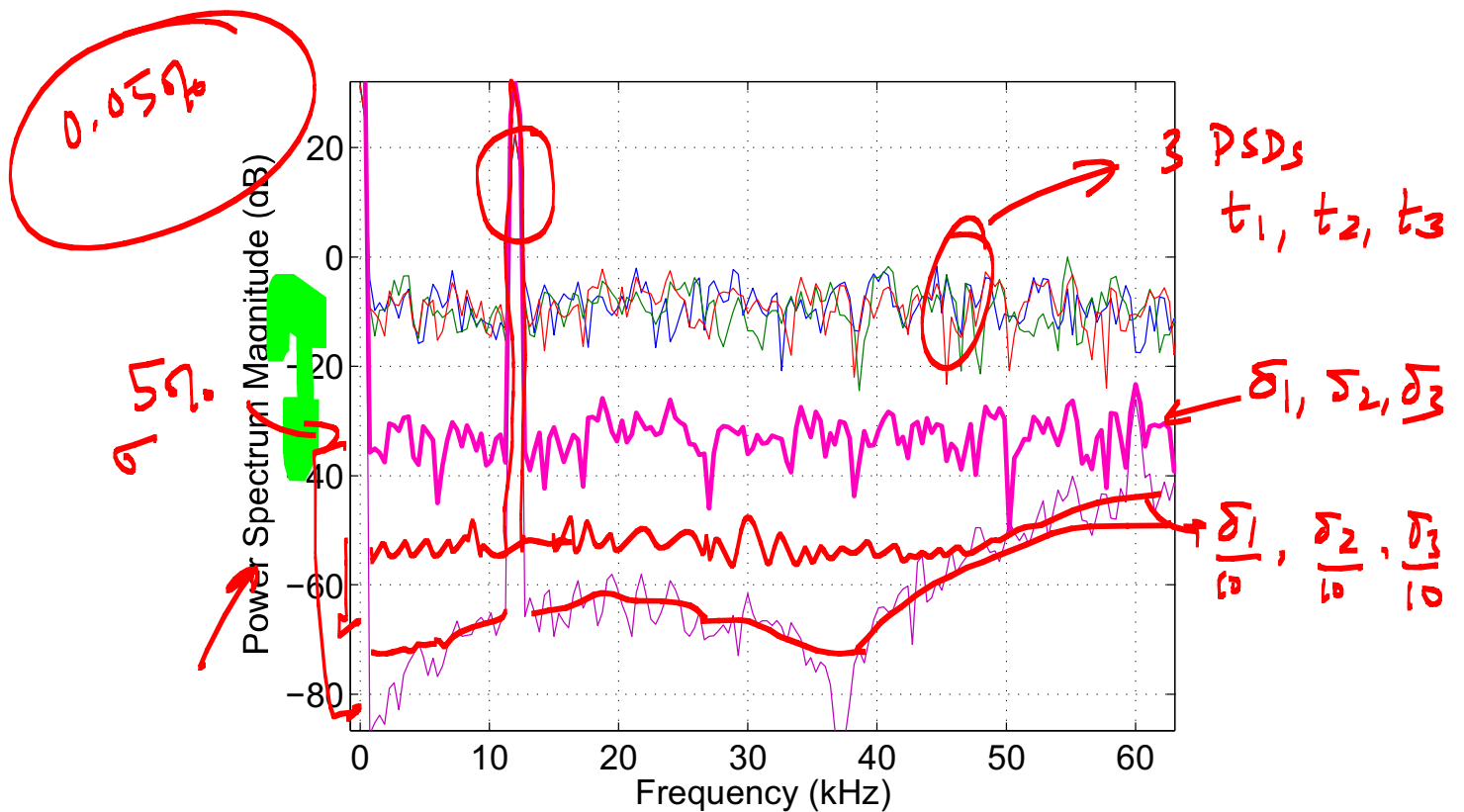
$$= 0$$

$$\text{with prob. } p \Rightarrow \frac{V}{nlev-1}$$

$$(1-p)$$

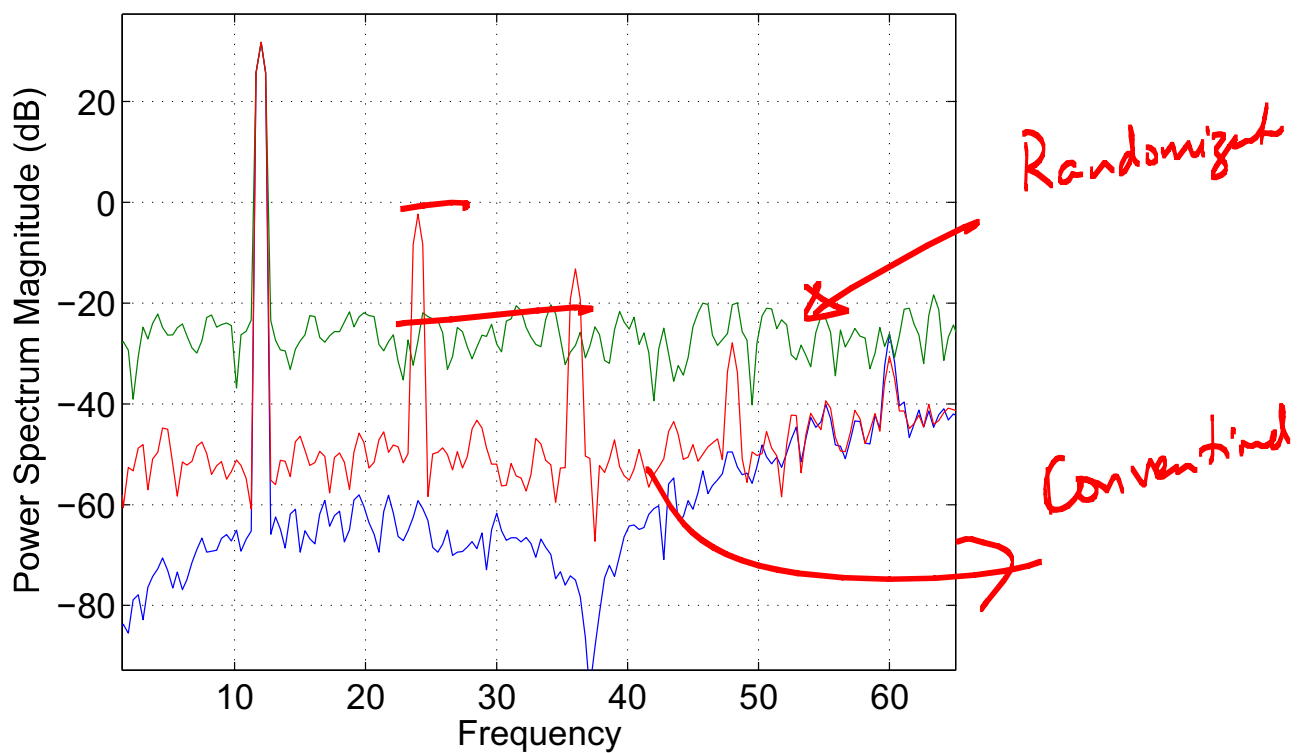
$$E(t_1) = p =$$

Dynamic Element Randomization



- Randomly choose v elements out of $(n/ev - 1)$.

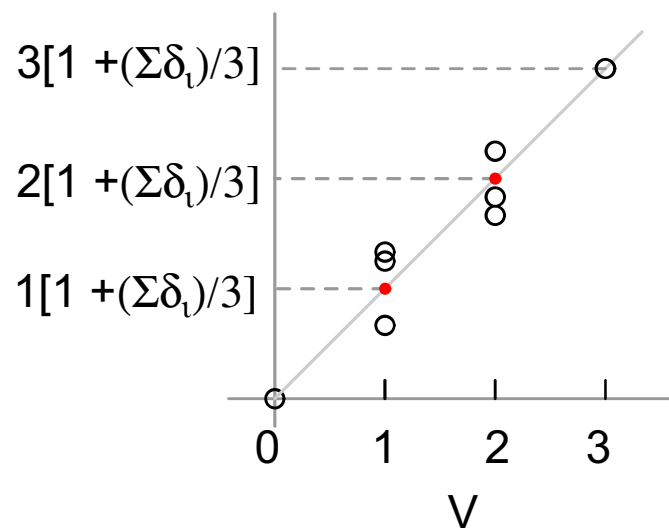
Dynamic Element Randomization



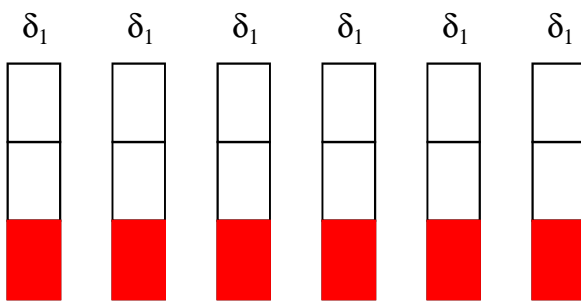
- Converts tones into white noise.

DAC levels with mismatch

v	0	1	2	3
	0	$(1 + \delta_1)$	$(2 + \delta_1 + \delta_2)$	$(3 + \delta_1 + \delta_2 + \delta_3)$
		$(1 + \delta_2)$	$(2 + \delta_2 + \delta_3)$	
		$(1 + \delta_3)$	$(2 + \delta_1 + \delta_3)$	

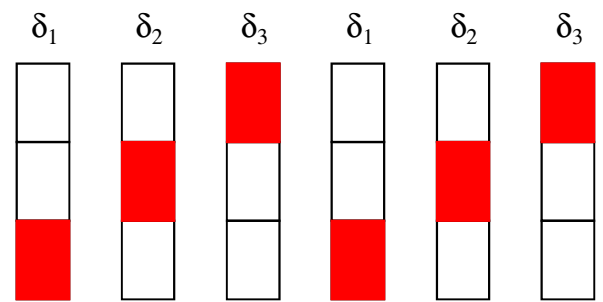


Individual Level Averaging



Conventional Element Selection

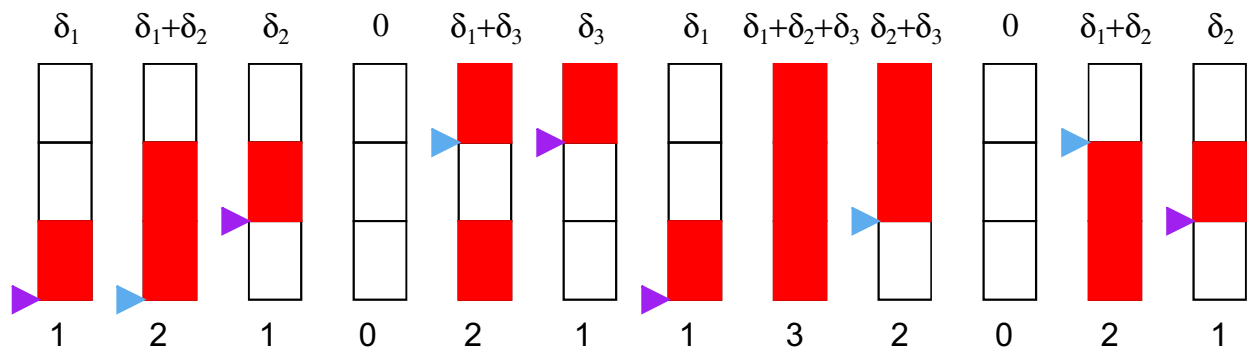
$v = 1$



Individual Level Averaging

$v = 1$

Individual Level Averaging



Individual Level Averaging With Varying Input