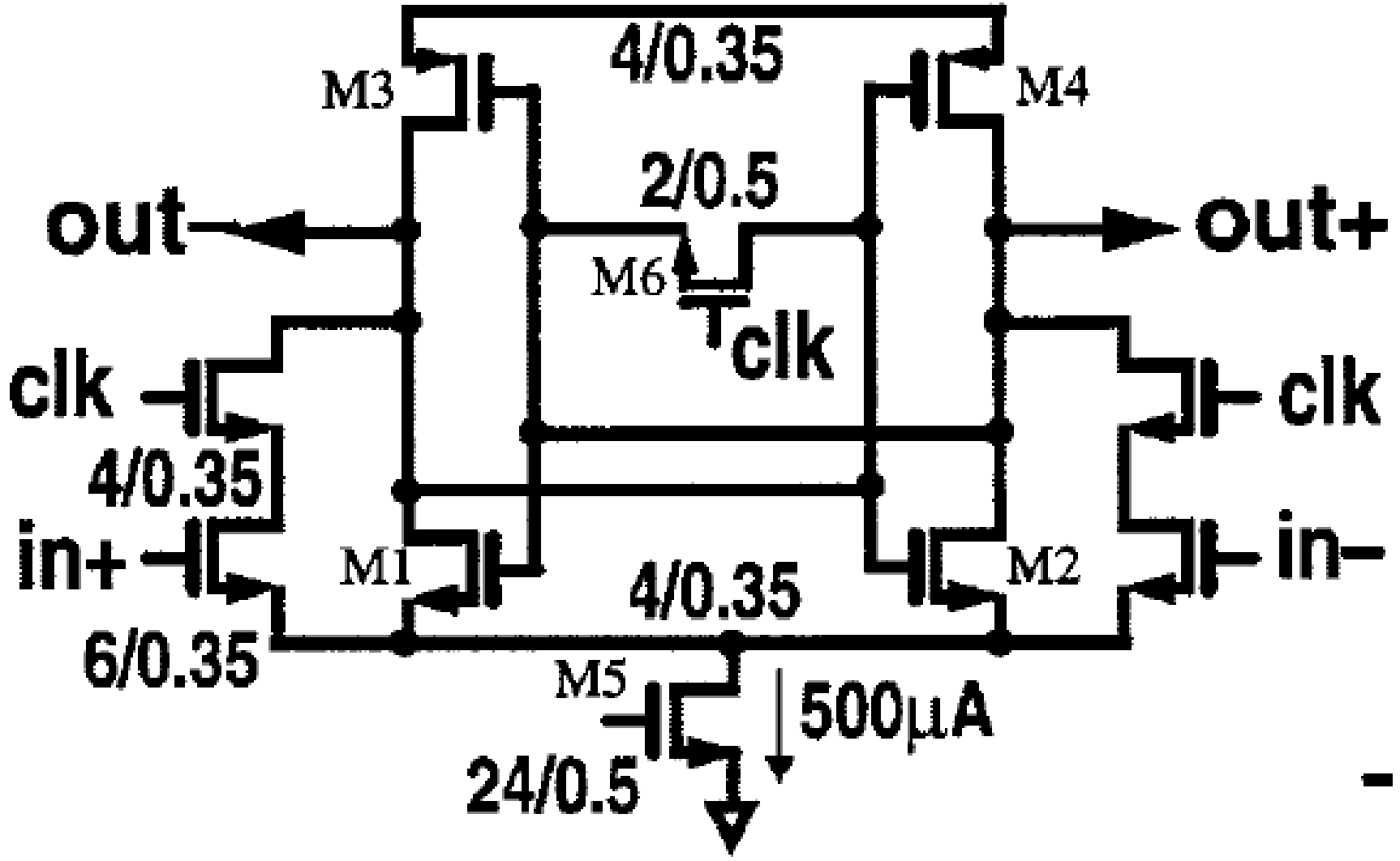
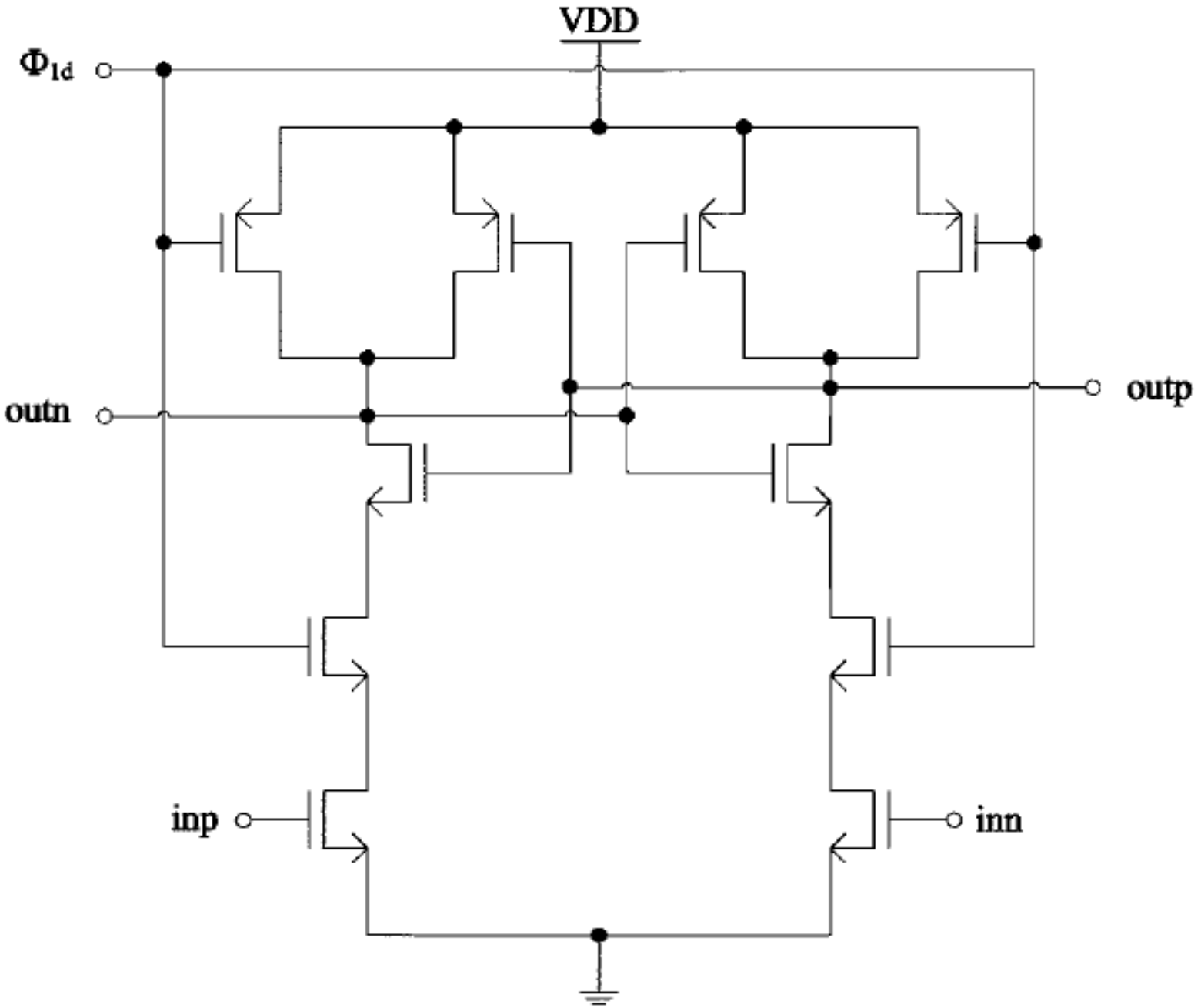


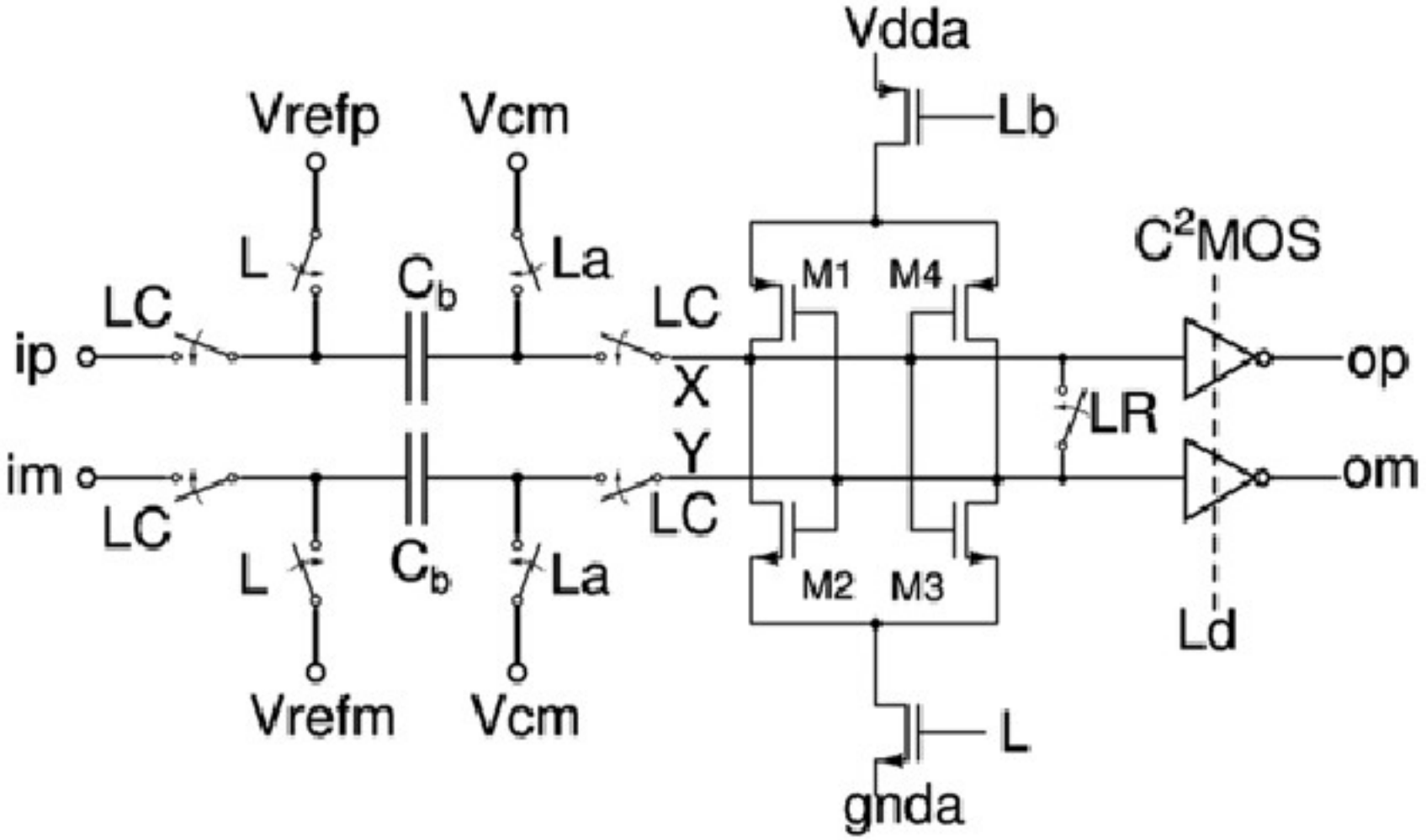
A 6-b 1.3-Gsample/s A/D Converter in 0.35-m CMOS

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 12, DECEMBER 2001



A 0.9-V 60-W 1-Bit Fourth-Order Delta-Sigma Modulator With 83-dB Dynamic Range

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 2, FEBRUARY 2008



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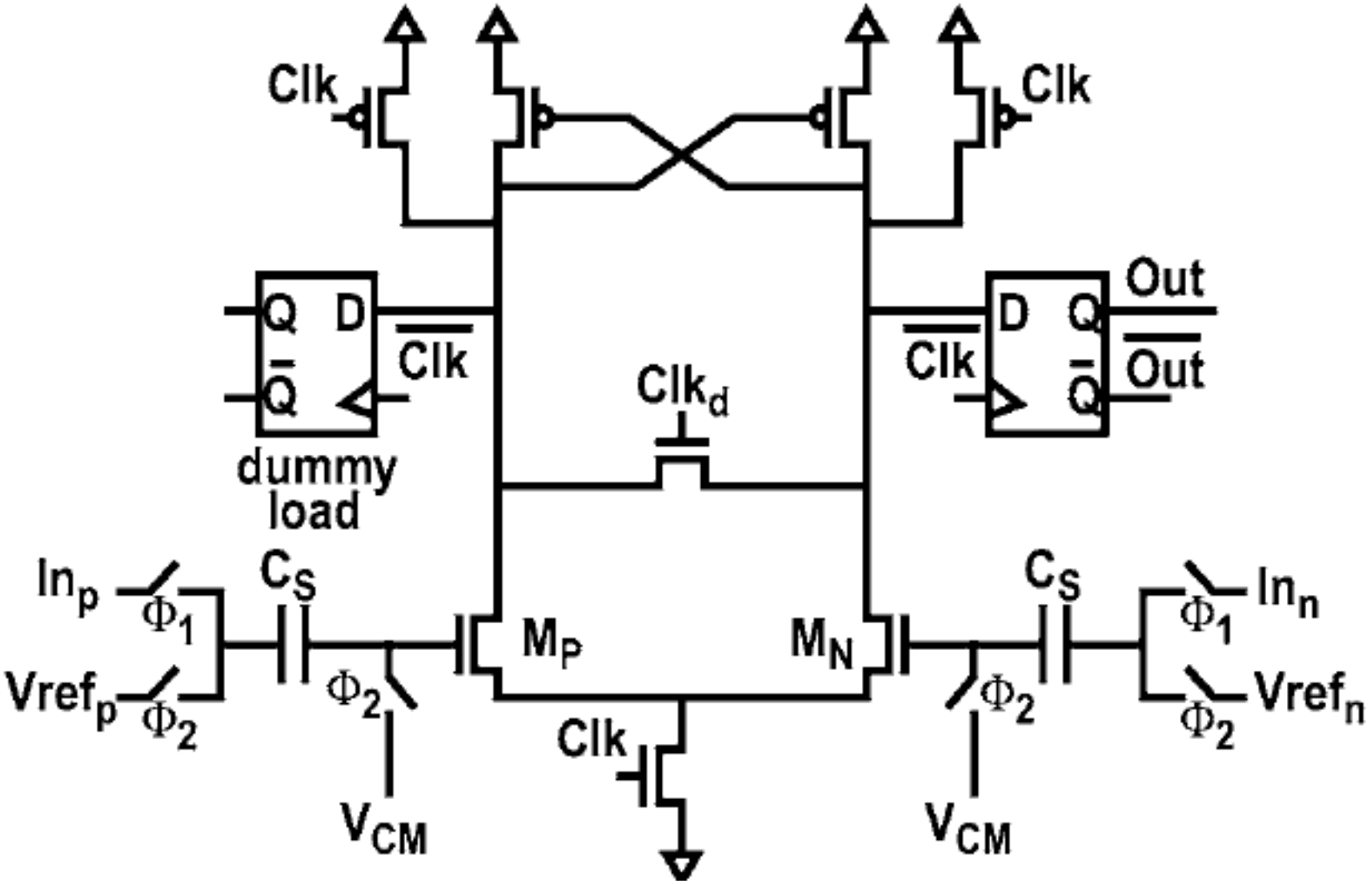
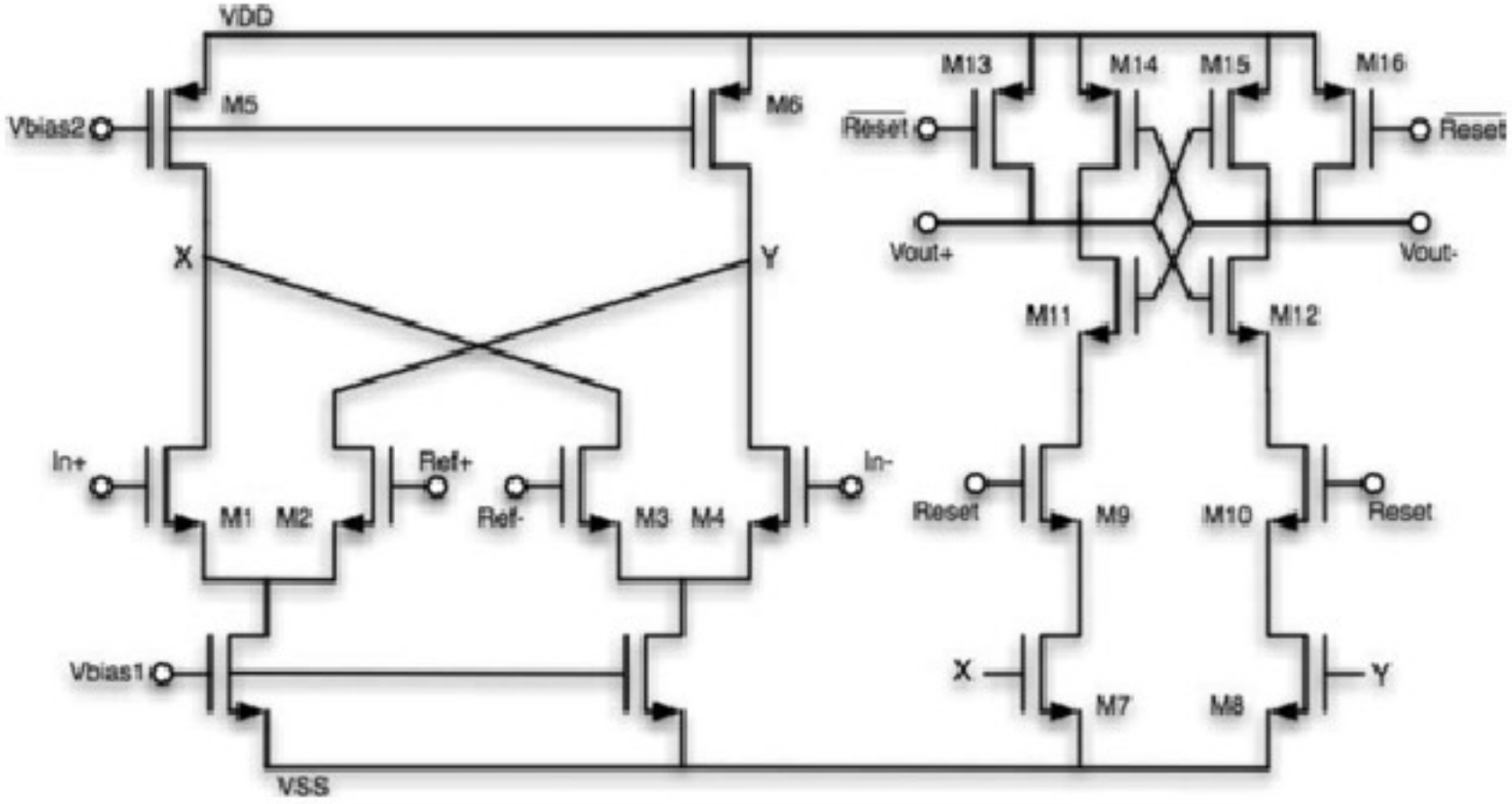


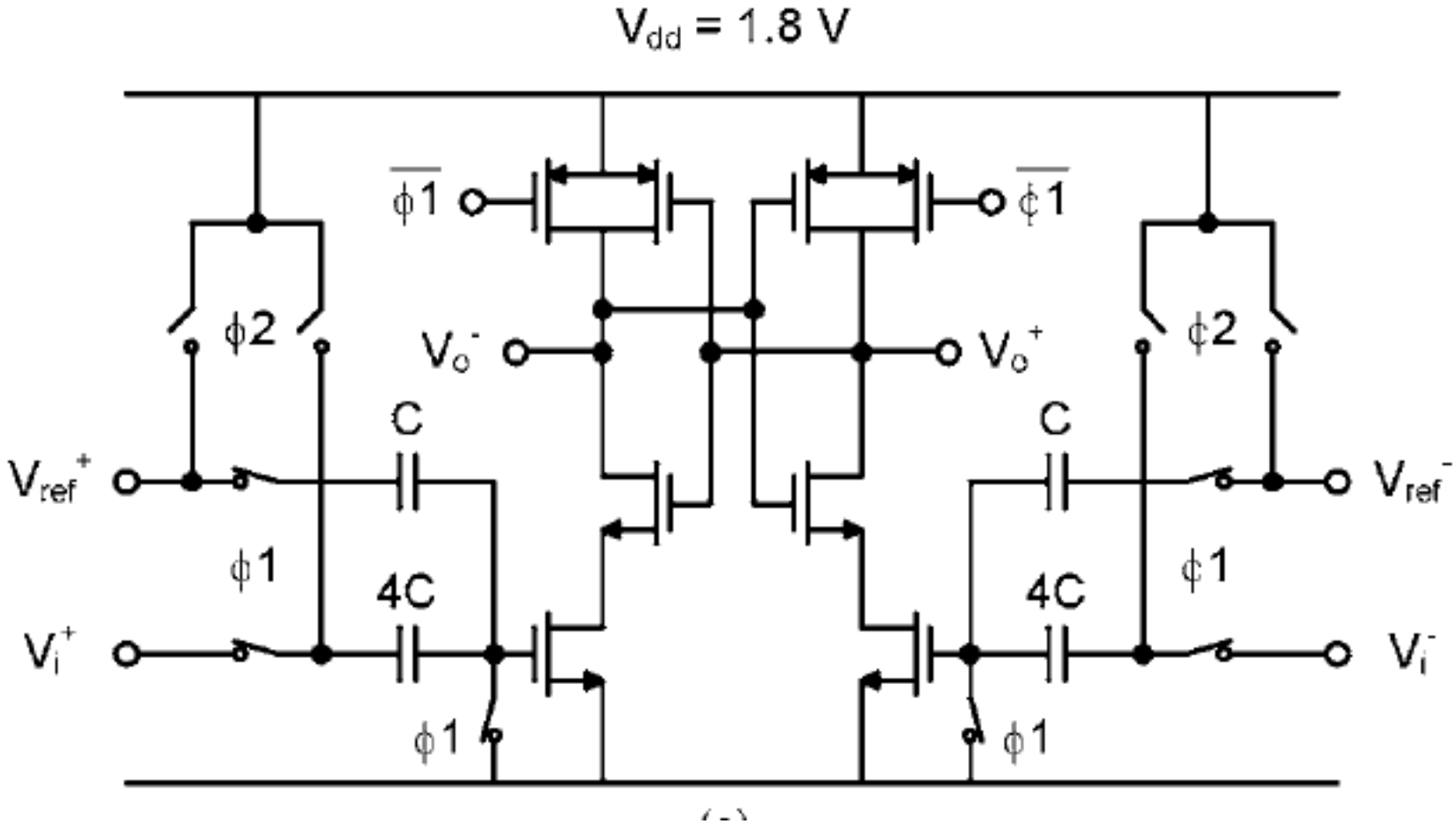
A 77-dB Dynamic Range, 7.5-MHz Hybrid Continuous-Time/Discrete-Time Cascaded 61 Modulator

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 4, APRIL 2008



40 MHz IF 1 MHz Bandwidth Two-Path Bandpass 61 Modulator With 72 dB DR Consuming 16 mW

GALDI et al.: 40 MHz IF 1 MHz BANDWIDTH TWO-PATH BANDPASS MODULATOR WITH 72 dB DR CONSUMING 16 mW



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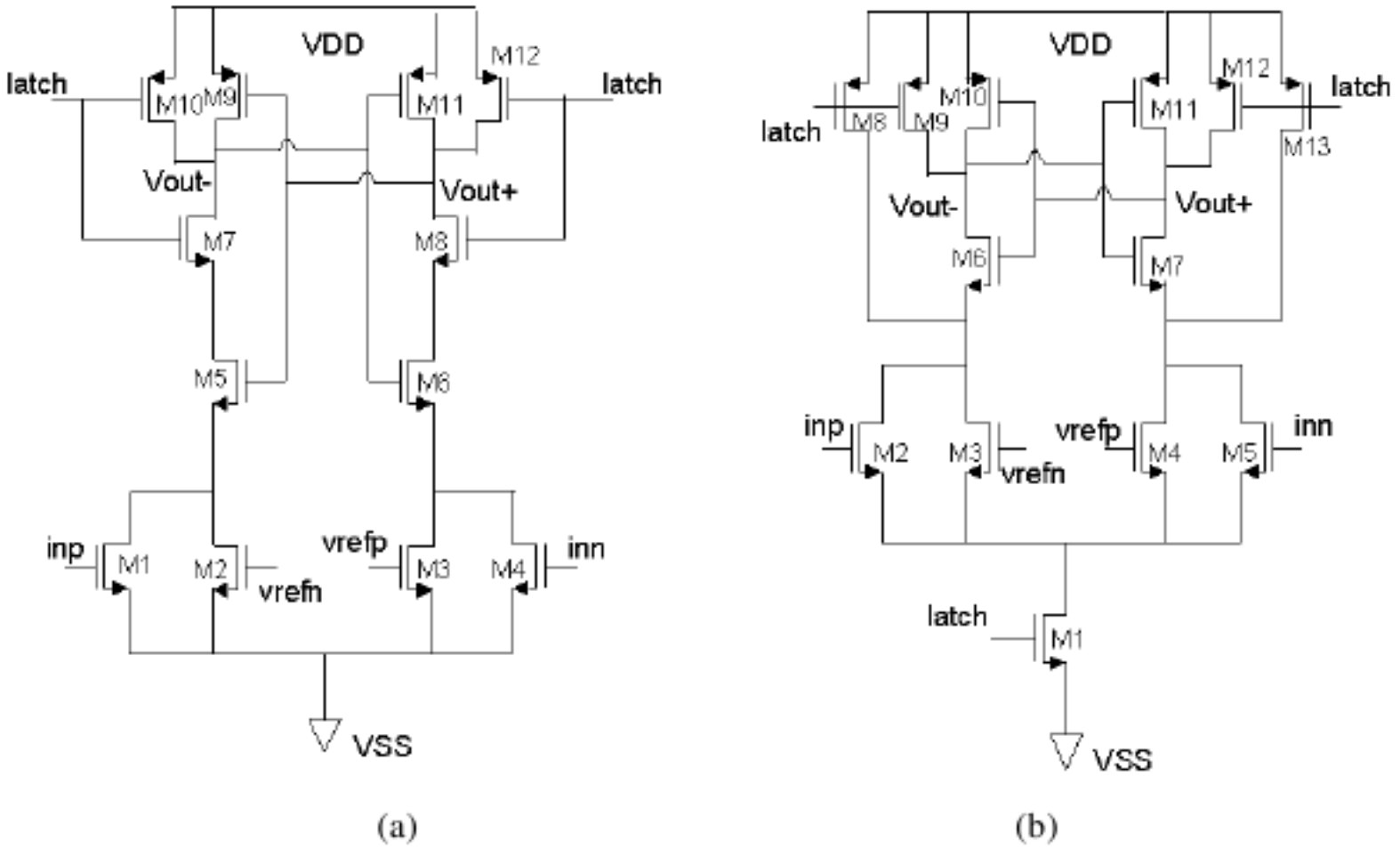

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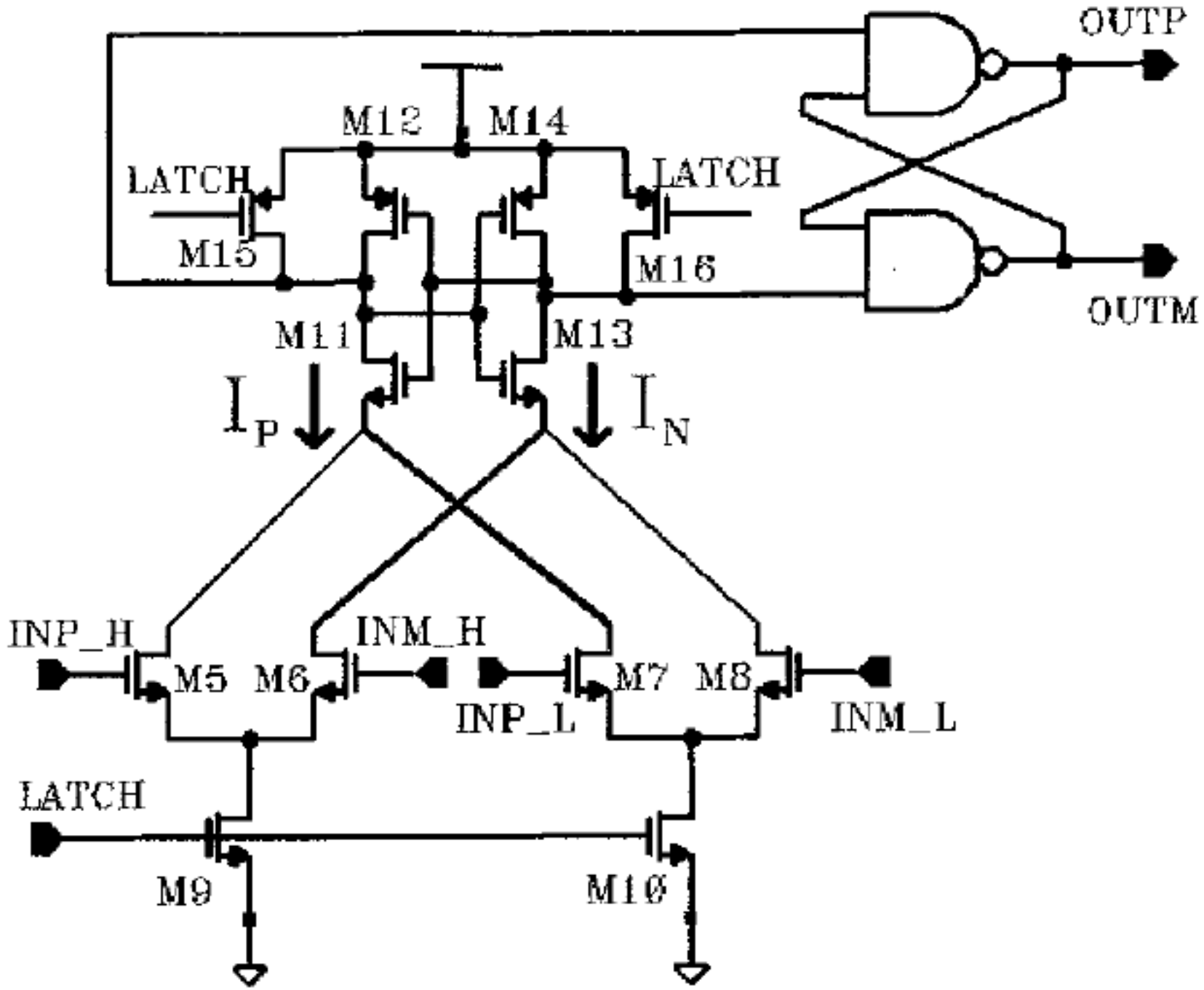

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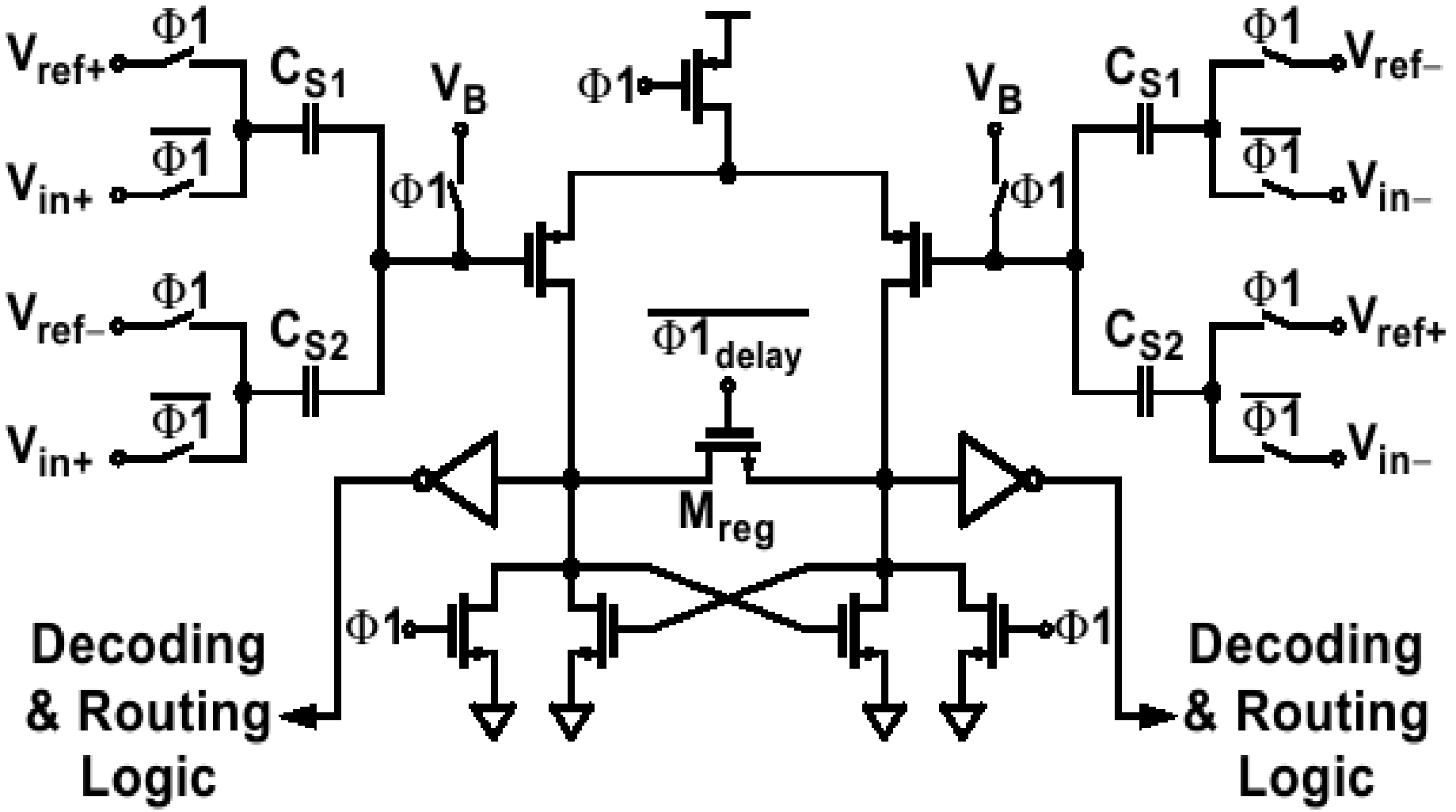

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Exercise

- Compare the following latches wrt
  - Static power dissipation
  - Dynamic offset
  - Speed
  - Number of clock phases