EE6320 Project 3: VCO + Divider Design – due Tuesday 14/04/2026 (11:59pm)

In this project, you are asked to design a fully-differential LC-VCO followed by a divide-by-two circuit that meets or exceeds the specifications given below. You can use one of the basic circuit topologies that was discussed in class. However, you can modify it with circuit techniques to improve its performance, supported by simulation results. Use the IBM 130 nm CMOS process parameters supplied to you through the class website (Vdd = 1.2 V, Wmin = 0.16 µm, Lmin = 0.12 µm). Design the VCO for the following specs:

- VCO frequency f_{VCO} = 6.90 to 7.10 GHz; Divider output frequency f_{LO} = 3.45 to 3.55 GHz.
- VCO Tuning range = 200 MHz; LO tuning range = 100 MHz
- Minimum VCO output differential amplitude = 1.2 V
- Phase noise specification: -122dBc/Hz @ 1MHz offset and -154dBc/Hz @ 20MHz offset
- Maximum number of inductors = 2. In the case of a NMOS-only or PMOS-only VCO, the two sections of a symmetrical centre-tap inductor is considered as 1 inductor, with the centre tap connected to VDD/ground. The second inductor can be used in various ways.
- Tuning can be done purely using a MOS-transistor-based varactor, or through a combination of MOS-transistor-based varactors for fine-tuning and a binary weighted switched-capacitor bank for coarse-tuning. The fine-tuning circuit should exhibit a nominal KVCO of 70MHz/V over the usable tuning range.
- In case coarse + fine tuning is implemented, there should be about 33% frequency overlap between fine tuning curves of adjacent coarse tuning bits.
- Design the divide by two circuit to produce 0, 90, 180 and 270 degree signals to drive the IQ receiver mixer from project 2.
- Minimise overall power consumption

Notes:

1) No ideal inductors are allowed! Add a resistor in parallel with each of the inductors in your circuit so that it has a Q of 20 at 3.5 GHz). All capacitors can be assumed to be ideal.
2) Include and discuss your VCO design procedure and architecture choice in your report. Remember to include the KVCO plot as well as VCO transient simulation output to show startup behaviour.
3) Discuss the divider topology and operation.