EE6320 Project 4: Power Amplifier Design – due Tuesday 28/04/2026 (11:59pm)

In this project, you are asked to design a differential power amplifier (PA) that meets or exceeds the specifications given below. Use the IBM 130 nm CMOS process parameters supplied to you (Vdd = 1.2 V, Wmin = 0.16 µm, Lmin = 0.12 µm). Design the PA for the following specs:

- F_{RF} = 3.45 to 3.55 GHz
- Minimum output P1dB = 20 mW (+13 dBm)
- Maximum AM-PM deviation at P1dB = 3 degrees
- Minimum PA voltage gain = 2 V/V
- Maximum number of inductors = 2.
- There is no specification on S22 (output matching is not required).
- You may use a matching network to transform the 50Ω load to a lower impedance so that PA drives a smaller impedance and can therefore deliver more power. However, you should design the PA to deliver the appropriate power to the 50Ω load after accounting for matching network loss (based on the Q below).
- Minimise overall power consumption

Notes:

1) No ideal inductors are allowed! Add a resistor in parallel with each of the inductors in your circuit so that it has a Q of 20 at 3.5 GHz). All capacitors can be assumed to be ideal.