EE6320 Project 3: VCO Design

In this project, you are asked to design a fully-differential LC-VCO that meets or exceeds the specifications given below. Use the TSMC 0.180 μm CMOS process parameters used by you earlier. Design the VCO for the following specs:

- f_0 = 1850 to 1920 MHz (70 MHz tuning range)
- V_{DD} = 1.8V
- Minimum VCO output single-ended amplitude = 1.2V
- Phase noise specification: -125dBc/Hz @ 1MHz offset and -157dBc/Hz @ 20MHz offset
- Maximum number of inductors = 2. In the case of a nmos-only or pmos-only VCO, the two sections of a symmetrical centre-tap inductor is considered as 1 inductor, with the centre tap connected to V_{DD}/ground. The second inductor can be used in various ways.
- Tuning can be done purely using a MOS-transistor-based varactor, or through a combination of MOS-transistor-based varactors for fine-tuning and a binary weighted switched-capacitor bank for coarse-tuning. The fine-tuning circuit should exhibit a nominal K_{VCO} of 70MHz/V over the usable tuning range.
- In case coarse + fine tuning is implemented, there should be about 33% frequency overlap between fine tuning curves of adjacent coarse tuning bits.
- Minimise overall power consumption
- Design a divide by two circuit to produce 0, 90, 180 and 270 degree signals to drive an IQ receiver mixer from 925 to 960 MHz

Notes:

1. No ideal inductors are allowed! Add a resistor in parallel with each of the inductors in your circuit so that it has a Q of 15 at 942.5 MHz. All capacitors can be assumed to be ideal.
2. Include and discuss your VCO design procedure and architecture choice in your report. Remember to include the K_{VCO} plot as well as VCO transient simulation output to show startup behaviour.
3. Discuss the divider topology and operation.