# EE6320 RFIC Project 1: LNA Design

In this project, you are asked to design a differential cascoded common source Low-Noise Amplifier (CS-LNA) for the specifications given below. The application will be 5GHz WLAN (802.11a) in the frequency band 5.170-5.320 GHz (for this and succeeding projects). The basic LNA circuit topology should be that discussed in class. However, you can modify it with circuit techniques to improve its performance, as long as you support it with analytical and simulation results. Use the IBM 0.130 μm CMOS process parameters supplied to you through the class website ($V_{dd}$=1.2V, $W_{min}$=0.16μm, $L_{min}$=0.12μm). Design for the following specs:

- Frequency of operation $f_0$ = 5170 to 5320 MHz (centre frequency of 5245 MHz)
- Differential $R_{in}$ = 100Ω; S11 < –10dB between 5170 to 5320 MHz. For all your simulations, place an ideal balun between single-ended input port with impedance of 50Ω and differential output ports each with 50Ω impedance to drive the LNA input.
- Voltage gain ≥ 20 dB over the complete band (differential voltage gain from balun output nodes to LNA outputs). Assume the LNA drives a load capacitance of 100 fF differential or 200 fF single-ended at the output port. This will represent the mixer input capacitance as well as any tuning required for process variations in tank resonance frequency. You can update this capacitance once the mixer is designed in the next project. Gain flatness over the above band should be ≤ 2dB.
- NF ≤ 3dB.
- $IIP_3$ ≥ –10dBm {Use two tones separated by 1MHz; choose the extrapolation point carefully}
- Minimise power consumption (i.e. total DC current drawn from supply)

Note 1: No ideal inductors are allowed! Add a resistor in parallel with each of the inductors in your circuit so that it has a Q of 20 at 5245 MHz). All capacitors can be assumed to be ideal.