EE6320 Design Project 4: PA Design – due 11:59pm Sunday 17/04/2022

In this project, you are asked to design a single ended power amplifier (PA) that meets or exceeds the specifications given below. Use the TSMC 0.18 μm CMOS process parameters used by you earlier. Design the PA for the following specs:

- f_{RF} = 0.9 to 1GHz
- V_{DD} = 1.8V
- Minimum output P_{1dB} = 14 mW (+11.5 dBm)
- Maximum AM-PM deviation at P_{1dB} = 5 degrees
- Minimum PA voltage gain from gate to drain = 2 V/V
- Maximum number of inductors = 2.
- There is no specification on S22 (output matching is not required).
- You may use a matching network to transform the 50Ω load to a lower impedance so that PA drives a smaller impedance and can therefore deliver more power. However, you should design the PA to deliver the appropriate power to the 50 Ohm load after accounting for matching network loss (based on the Q below).
- Minimise overall power consumption

Note 1: No ideal inductors are allowed! Add a resistor in parallel with each of the inductors in your circuit so that it has a Q of 15 at 1 GHz. All capacitors can be assumed to be ideal.