EE6320 Project 1: LNA Design – due Sunday 27/02/2022 (11:59pm)

In this project, you are asked to design a differential cascoded common source Low-Noise Amplifier (CS-LNA) for the specifications given below. The basic circuit topology should be that discussed in class. However, you can modify it with circuit techniques to improve its performance, as long as you support it with analytical and simulation results. Use the TMSC 0.180 μm CMOS process parameters supplied to you through the class website. Design for the following specs:

- Frequency of operation f_0 = 0.9 to 1 GHz
- Differential R_{in} = 100Ω; S11 < –10dB between 0.9GHz to 1GHz. For all your simulations, place an ideal balun from ahdlLib library between single-ended input port with impedance of 50Ω and differential output ports each with 50Ω impedance to drive the LNA input.
- Voltage gain ≥ 20 dB over the complete band (differential voltage gain from balun output nodes to LNA outputs). Assume the LNA drives a load capacitance of 250fF differential. This will represent the mixer input capacitance as well as any tuning required for process variations in tank resonance frequency. Gain flatness over the above band should be ≤ 3dB.
- NF ≤ 2dB.
- IIP_3 ≥ –10dBm {Use two tones separated by 1MHz; choose the extrapolation point carefully}
- Minimise power consumption (i.e. total DC current drawn from supply); V_{DD} = 1.8V

Note 1: No ideal inductors are allowed! Add a resistor in parallel with each of the inductors in your circuit so that it has a Q of 15 at 1GHz). All capacitors can be assumed to be ideal.

Note 2: If the gate inductor becomes too large (>7nH), its Q will limit your noise figure. For this project, assume that the gate inductor will be implemented using a high-Q off-chip inductor. Therefore, add a resistance in parallel with the gate inductor such that its Q = 50 at 1GHz.