EC5190/EE5390 Analog Integrated Circuit Design
Assignment 5
(Wednesday, April 30, 2014)

0.18μm technology parameters: V_{Tn} = 0.5V; V_{Tp} = 0.5V; K_n = 300 μA/V^2 ; K_p = 75 μA/V^2 ; A_{VT} = 3.5mV μm; A_β = 0; V_{dd} = 1.8V; L_{min} = 0.18μm, W_{min} = 0.24μm; Ignore body effect unless mentioned otherwise. For all MOS transistors, use $A_d = A_s = 2WL_{min}$; and $P_d = P_s = 2(W + 2L_{min})$ in simulations.

1. **Fully differential two stage opamp design**: The fully differential opamp shown in Fig. 1 should be used to make an amplifier of gain 2 and a closed loop -3dB bandwidth of f_b = 10MHz with R_L and C_L given below. The phase margin of all loops should be 60°. Minimize the value of miller capacitors in all loops. Use zero cancelling resistors in series with miller capacitors. A minimum open loop gain of 40dB is required.

Roll No.	Input pair	C_L (pF)	R_L (kΩ)
4N	pMOS	6pF	2.5
4N+1	pMOS	3pF	5
4N+2	nMOS	6pF	2.5
4N+3	nMOS	3pF	5

Tabulate the following:
(a) W, L and operating points(g_m, g_{ds}, V_{GS}-V_T, I_D) of all transistors. Use transistor names given in Fig. 1).
(b) Values of other components in the opamp.
(c) DC gain of the opamp.
(d) DC loop gain of the two common mode feedback loops.
(e) Input referred offset (For this, ignore current factor mismatch; Calculate σ_{VT} from the sizes, and use g_m values from the operating point; You can assume $g_m \gg g_{ds}$).
(f) Power consumption.

Plot the following: (choose appropriate axes limits and font sizes for plotting. Illegible plots do not get any credit).
(a) Differential loop gain-magnitude and phase; Indicate the phase margin.
(b) Differential closed loop gain-magnitude and phase; Indicate the -3dB bandwidth.
(c) First stage common mode loop gain-magnitude and phase; Indicate the phase margin.
(d) Second stage common mode loop gain-magnitude and phase; Indicate the phase margin.
(e) Transient response of the unity gain inverting amplifier with a 0.2V differential step (use 0.1ns rise/fall times).
(f) Transient response of the unity gain inverting amplifier with a 0.1V common mode step (use 0.1ns rise/fall times).
(g) Input referred noise spectral density-identify 1/f noise corner. Show relative contributions from different devices at 10MHz.

Do not use ideal current sources in the tail. You can use one ideal reference current source of 1/10th the tail current of the input differential pair for bias generation. Design the bias generator block that generates bias currents and voltages required in the opamp.
Try to determine as many parameters as possible from the specifications and choose sensible starting points for the others. You can assume a gate overdrive of 200mV in your initial calculations. Make sure to use replicas correctly (i.e. same transistor length) wherever applicable.

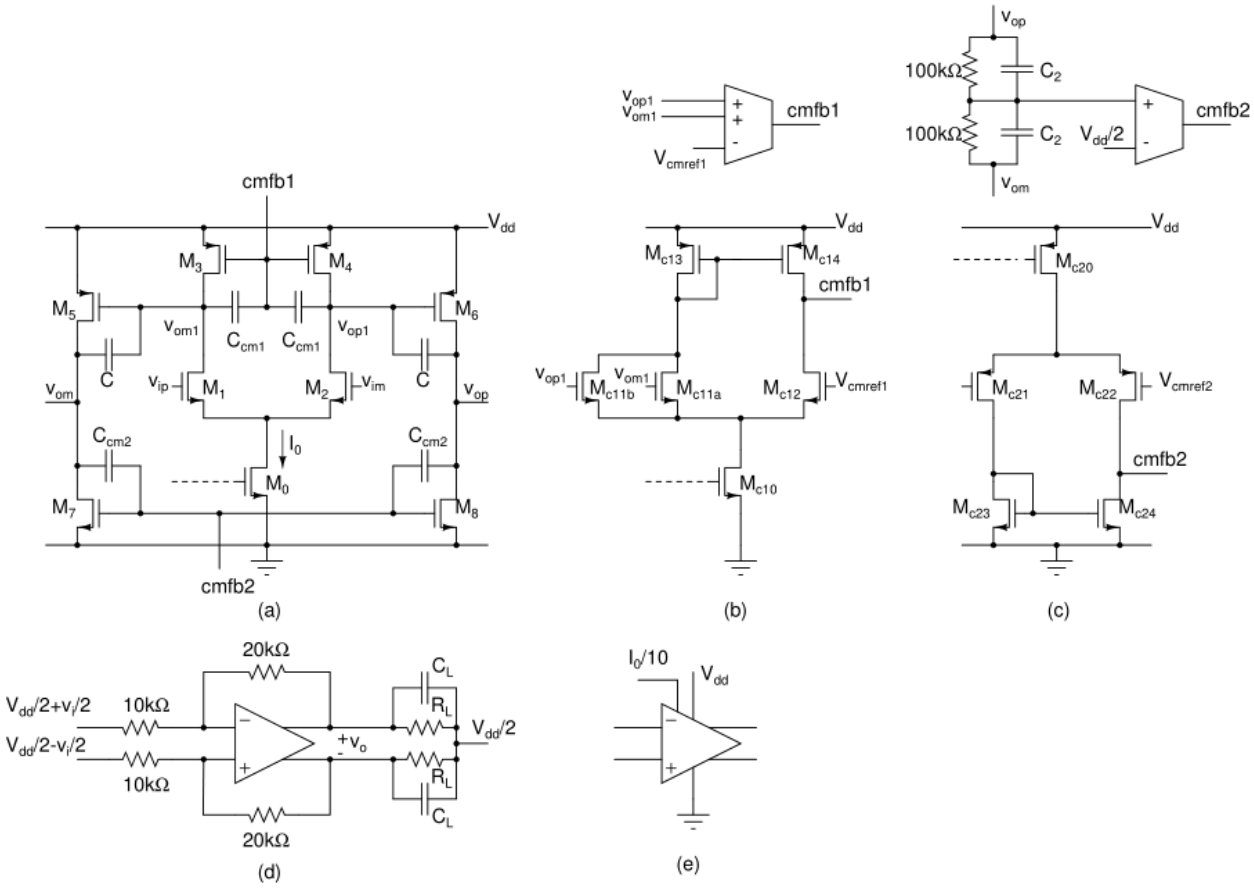

Figure 1: (a) Fully differential two stage opamp(Zero cancelling resistors not shown), (b) First stage common mode feedback, (b) Second stage common mode feedback, (d) Closed loop amplifier, (e) External connections to the opamp. ***With a pMOS input pair, all transistors will be of the opposite polarity***