ACTIVE FILTER DESIGN : PROBLEM SET 5

Problem 1 : Distortion

In class, we derived the expression for the differential output current of a diff-pair as a function of differential input. Assume that for small signals, the characteristic is predominantly a third order one, i.e, $i_{out} = a\,v_i - b\,v_i^3$. Let $v_i = A\,\sin(\omega_{in}\mathrm{t})$.

a. Find a and b as a function of I and k. Find the 3^{rd} harmonic distortion as a function I, k and the amplitude of the input signal A.

b. Suppose the input has DC offset, i.e, $v_i = v_{off} + A\,\sin(\omega_{in}\mathrm{t})$. Find the harmonic components of the output current. How much offset can you tolerate before the second harmonic amplitude becomes a tenth of the thrid harmonic amplitude ?

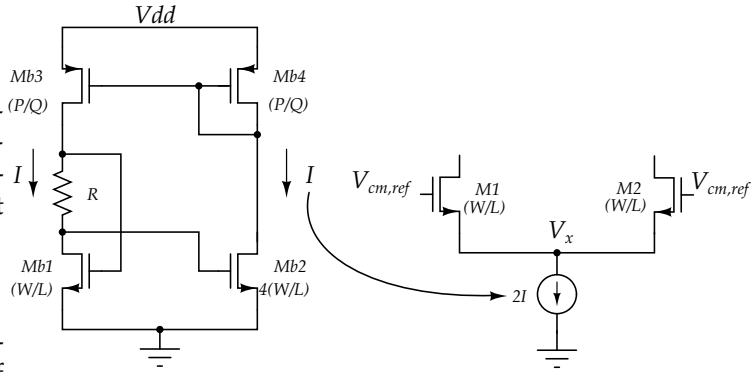

Figure 2: A partial fix for the body effect problem.

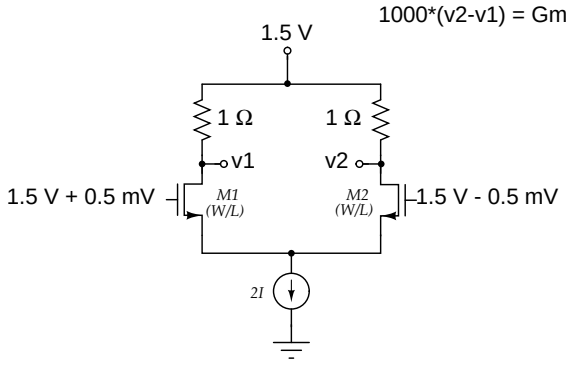

Figure 3: Measuring transconductance of M1.

Problem 2 : Stabilizing Transconductance of a Differential Pair

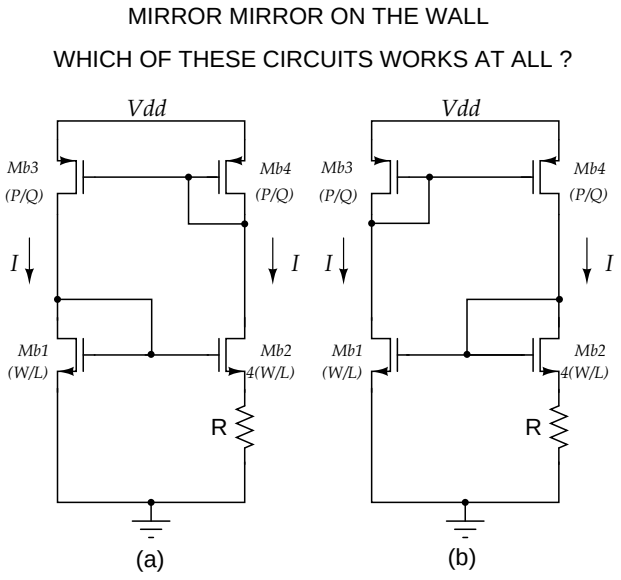

Figure 1: Basic fixed G_m bias circuits.

A time constant associated with a Gm-C filter is of the form G_m/C. One has to keep this time constant stable over process and temperature. In practice, C is fairly stable, so that one needs to take care of only the variation in G_m. Figure 1 shows a circuit that attempts to stabilize the transconductance of a transistor. It is one of many circuits that are called "fixed transconductance bias" circuits. The idea is to "servo" the G_m of a "master" device ($Mb1$ in the cases discussed below) to a stable external resistor R. Once this is done, all devices whose transconductance need stabilization are biased at the same operating point as the "master" device in the "servo" circuit as shown, for instance in Figure 2. Eventually, we are interested in the Gm of the "slave" devices (M1, M2 in Figure 2). Use the circuit of Figure 3, to do this.

a. First, analyze the circuit of Figure 1 (a). Assume that the bodies of all devices are tied to their sources and neglect output impedance of the devices. $\mathrm{V_{dd}}$ is such that all devices operate in saturation. Find the current I and the transconductance of $Mb1$.

b. Repeat for the circuit of Figure 1 (b). One of these circuits works and one doesn't. Which one works ? Why ?

c. Simulate the circuit in SPICE. Choose the lengths of all devices to be $1\,\mu\,\mathrm{m}$. $\mathrm{V_{dd}}$ is $1.8\,\mathrm{V}$. Choose R to be $1\,\mathrm{K\Omega}$, and the gate overdrive of $Mb1$ to be $V_{gs} - V_t = 250\,\mathrm{mV}$. Plot the $\mathrm{G_m}$ of $M1$ as temperature is varied from $0 - 70^o\,\mathrm{C}$.

d. Most CMOS technologies are n-well processes. That means that the bodies of the NFETs are connected to the lowest potential on the chip (ground, in this case.) Redo part (c) above with the NFET bodies grounded. How does the variation in G_m of $M1$ compare with that you found in part (c) ?

e. A partial fix for the body effect problem is shown in Figure 2. Analyze this circuit and run a temperature sweep as above. What do you notice ?

Problem 4 : Precision Biasing

This problem compares various techniques one might use to bias a differential pair at a desired current Iin per transistor. Use that value of Iin that results in a gate overdrive of about $300\,\mathrm{mV}$ and $(W/L) = (10\mu/0.7\mu)$. Once you determine Iin keep it constant for the rest of the problem.

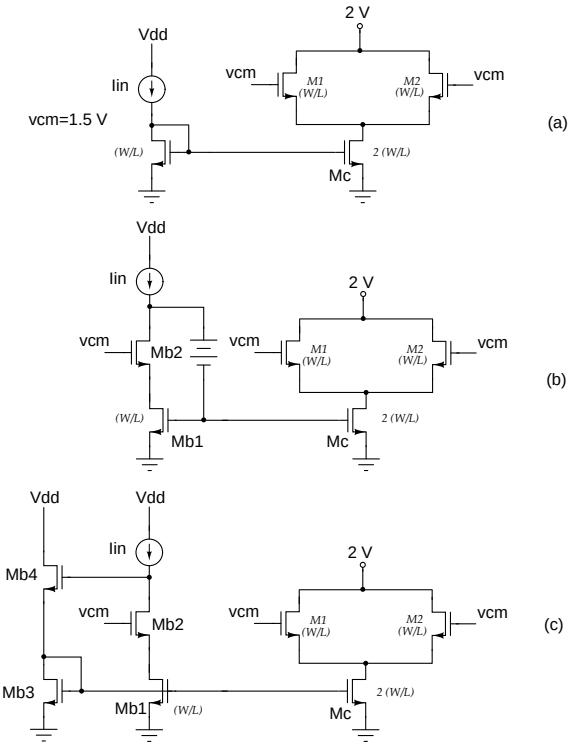

Figure 4: Evolution of precision biasing.

a. The first thing that comes to mind is a mirror, as shown in Figure 4(a). Assume that $M1$ and Mc has a gate-source voltage $V_T + \Delta\,v$ and an output impedance r_{out}. $vcm = 1.5\,\mathrm{V}$. What is the error in the current of $M1$ as a percentage of Iin ? Sweep vcm from $0.5 - 2.0\,V$ and plot the current in $M1$ as a function of the common-mode voltage.

b. Consider now the improved scheme shown in Figure 4(b) & (c). Explain why this is an improvement. What should the minimum value of the battery potential be to make the circuit operate as intended ? Which of the devices need to be operated at the same current density ? i.e. Mc and $Mb1$ should be of the same current density etc. Similary what can you say about $Mb2$, $Mb3$ and $Mb4$?

c. Now, sweep vcm from $0.5 - 2.0\,V$ and plot the current in $M1$ as a function of the common-mode voltage. What do you notice ?

Problem 5 : Common Mode Feedback

Figure 5 shows a fully differential transconductor with common-mode feedback through the triode-operated MOSFETs M7 & M8. Design the sizes of the transconductor under the following constraints

a. M1, M2 & M3 are to be identical.

b. Under no signal conditions, $g_{m|M4}$ must be $1/(10\,\mathrm{K\Omega})$. The distortion in differential output current for an input differential voltage of $100\,\mathrm{mV_{pp}}$ should be less than $2\,\%$.

c. Output common-mode voltage must be $1.7\,\mathrm{V}$ and must be compatible with the input common-mode level.

d. The power supply voltage is $3.3\,\mathrm{V}$. Design the circuit for room temperature (300 K).

e. Use a channel length of $L = 1\,\mu\mathrm{m}$ for all devices.

How does one generate V_{bias} ? Find all device sizes. I am interested in your line of thought and how you went about designing rather than the final answer. So, do not skip steps, and carefully write down your design procedure. It is OK if you get stuck in the middle. Do not collaborate (a.k.a copy) from a fellow student. Both of you will get no credit. You may use a reference voltage of $1.7\,\mathrm{V}$, and an ideal current source of any value to please in your design. Sweep temperature from $0 - 70^o\,C$ and plot the output common-mode voltage as a function of temperature.

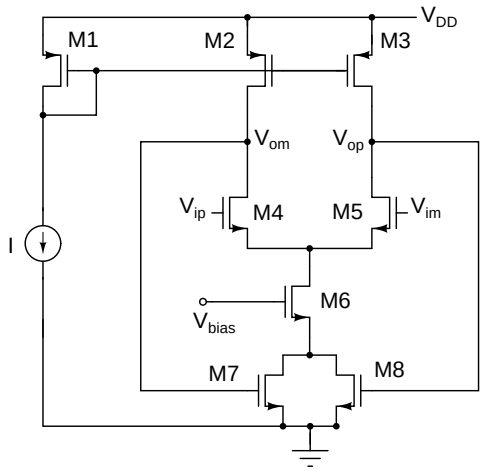

Figure 5: Common Mode Feedback Using Triode-operated MOSFETs.

Test the stability of your common-mode feedback using the circuit shown in Figure 6. The 1 pF capacitance represents the integrating capacitance of the transconductor. Observe the waveform at the node labeled vx. What can you infer about the common-mode impedance and bandwidth of the CM loop from the time domain waveform at vx ?

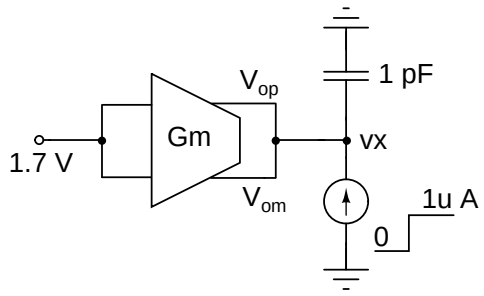

Figure 6: Common Mode Feedback Using Triode-operated MOSFETs.

Problem 6 : Circuit Noise Calculations

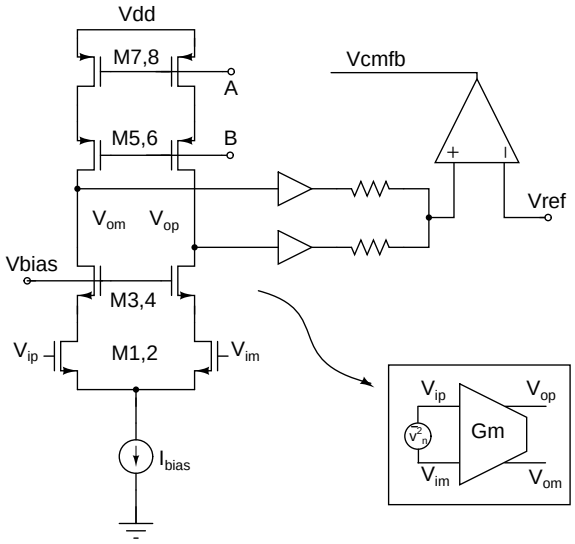

Figure 7: Noise calculations for a cascoded differential pair.

Figure 7 shows a cascoded differential pair transconductor. Assume that $Vref$ is high enough so that M1,2 & M3,4 are in saturation. One is faced with three choices:

a. Connect Vcmfb to A, appropriate bias at B.

b. Connect Vcmfb to B, appropriate bias at A.

c. Connect Vcmfb to A & B.

Assume that the servo amplifier has a low gain. Which is the best of the above strategies ? Explain clearly.

Now consider choice (a) above. Assume Vdd is high enough & node B is properly biased so that all devices are in saturation. Further, assume that all NFETs have a transconductance g_{mn} and all PFETs have a transconductance g_{mp}. Find the input referred voltage noise spectral density of the transconductor, as shown in the inset of the figure.

Problem 7 : Circuit Noise Calculations

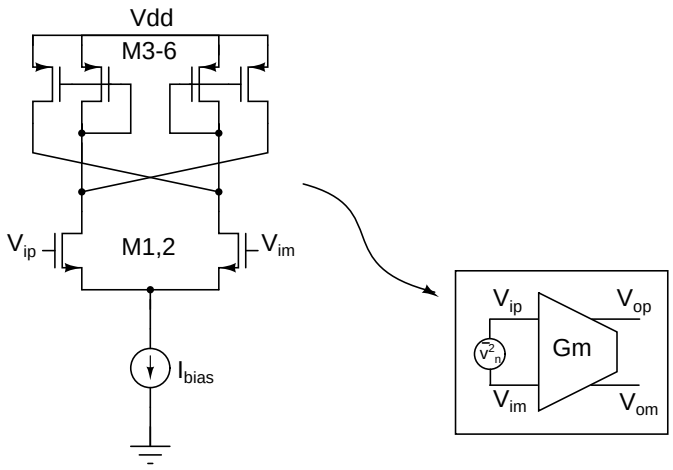

Figure 8: A transconductor employing a negative resistor load.

Figure 8 shows a transconductor with a negative resistor load. Assume that Vdd is high enough so that M1-6 are in saturation. Assume that all NFETs have a transconductance g_{mn} and all PFETs have a transconductance g_{mp}. Find the input referred voltage noise spectral density of the transconductor, as shown in the inset of the figure.

Problem 8 : Circuit Noise Calculations

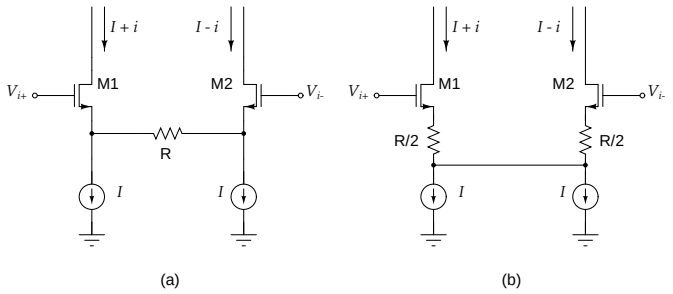

Figure 9: Denegenerated differential pairs.

Consider the input stages of the transconductors shown in Figure 9 (a)&(b). Assume that in both cases, M1 & M2 have a transconductance of g_m. Assume that each current source I is implemented using a MOS transistor with a transconductance of g_{mx}.

Find the transconductance (G_M) and the equivalent input voltage noise spectral density for both transconductors. Express the result as $\overline{v_n^2} = (8kT/3)(1/G_M)\eta$, where $(8kT/3)(1/G_M)$ is the noise for an ideal transconductor, and η is the so-called "excess noise factor". What should be the design considerations for both circuits to bring down the excess noise factor ?