DCM Operation and Zero Cross Detect

EE5325 Power Management Integrated Circuits

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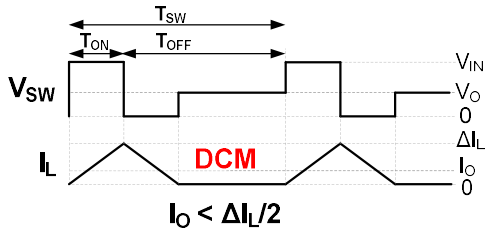
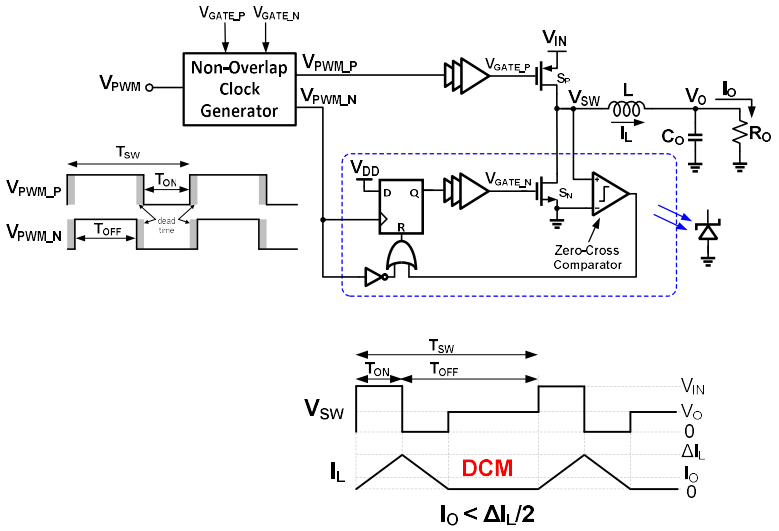
Detecting CCM-DCM Boundary

- Converter is operated in DCM by turning OFF low side FET (S_N) as soon as inductor current goes zero
- Zero current can be detected using zero-cross comparator as V_{SW} goes from negative to positive
- Can be used to switch from PWM to PFM mode
- Usually CCM-DCM detector output is de-bounced before entering/existing DCM mode to filter out any glitches



Implementing DCM Operation



Zero-Cross Comparator Requirement

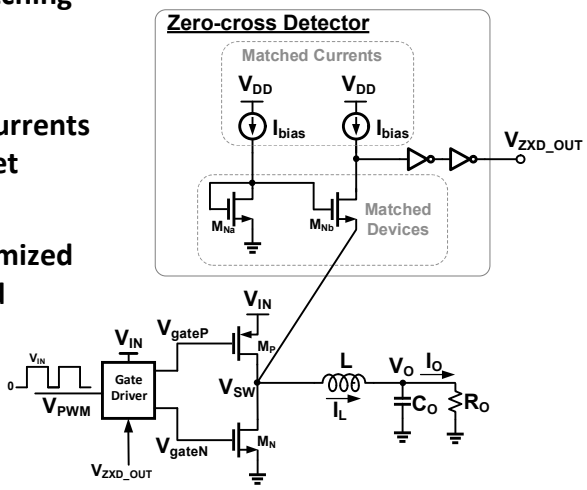
- **Since voltage drop across NFET is low (due to low R_{ds_on}), a very high gain and low offset comparator is required to detect the inductor reverse current**
  - **Assuming 100mOhm Rds_on, 1mV error may cause error of 10mA in zero current detection.**
- **Comparator delay should be minimized as it may also introduce error**
  - **Assuming 1MHz and 10% duty cycle, with Vout=1.2V, L=1uH, inductor current slope is 1.2A/µs → 10ns delay can cause an error of 12mA in the zero current detection**
  - **This becomes even more challenging when switching at higher frequencies (10MHz and above).**

Zero-Cross Comparator Topologies

- Conventional two stage comparator is not suitable of zero current detection mainly due to large delay
- High speed comparator with offset cancellation is usually required to minimize the error
- Current comparator can also be used to minimize the delay

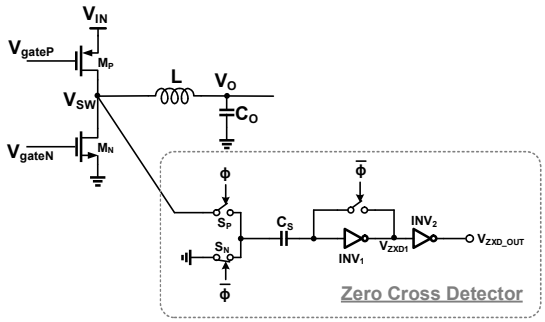
Current Based Zero-Cross Detector

- Requires good matching between devices
- Any mismatch in currents will introduce offset
- Offset can be minimized by good layout and cascaded devices



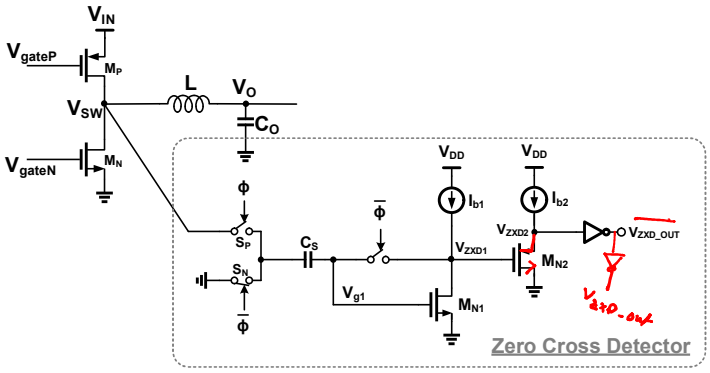
Inverter Based Auto-Zeroed Comparator

- ϕ and $\bar{\phi}$ are non overlapped clocks generated from V_{gateN}
- When V_{gateN}=0, C_S is pre-charged to V_{trip} of INV_1
- When V_{gateN}=1, C_S samples V_{SW} node
- V_{ZXD_OUT}=0 if V_{SW} < 0 and V_{ZXD_OUT}=1 if V_{SW} > 0
- Any static offset is automatically cancelled
- Any variation in V_{DD} of inverter INV_1 during V_{SW} sampling introduces error



Improved Inverter Based Auto-Zeroed Comparator

- Power supply rejection is improved by using current biased inverter (I_{b1} and M_{N1}).
- Any variation in V_{DD} during V_{SW} sampling is blocked by I_{b1} hence does not affect output → dynamic offset cancellation



Stephen W. Bryson , Using auto-zero comparator techniques to improve PWM performance, *eetimes article, 2008*