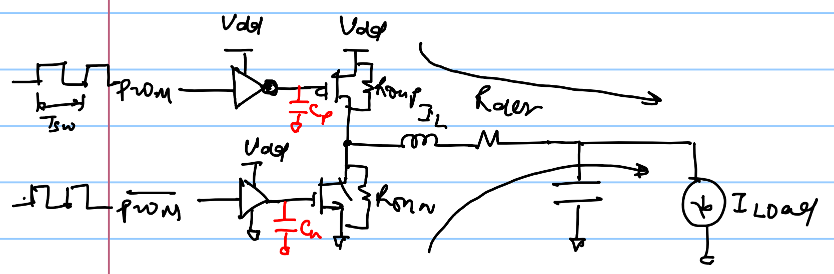
Losses in switching dc-dc converters



PWM & $\overline{PWM}$ are non-overlapped.

① Conduction Loss. → Resistive Loss

$$P_{cond} = I_{rms}^2 \cdot R$$

$$P_{cond} = I_L^2 \left(D \cdot R_{onp} + (1-D) R_{onn} + R_{dcr} \right)$$

② Gate switching Loss.

$$P_{gate\_sw} = C_p V_{dd}^2 F_{sw} + C_n V_{dd}^2 F_{sw} \qquad F_{sw} = \frac{1}{T_{sw}}$$

$$= (C_p + C_n) V_{dd}^2 F_{sw}$$

not a function of load current (Fixed loss for constant V_{dd} & F_{sw}

$C_p = C_n = 10\,pF$

$V_{dd} = 1.8\,V$

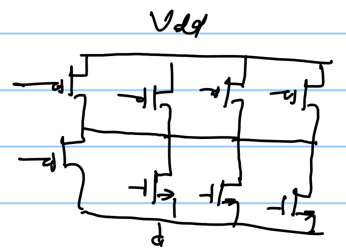
$F_{sw} = 1\,MHz$

$$P_{gate\_sw} = 20\,pF \times (1.8)^2 \times 10^6 = 64.8\,\mu W$$

if $F_{sw} = 10\,MHz$

$P_{gate\_sw} = 648\,\mu W$

[switching Frequency must be reduced at light load for high efficiency]



$P_{gate\_sw} = C V^2 f$ ↓ reduce f (PFM)

↓ reduce C (segmented FET)

Segmented FET

used smaller FETs in parallel instead of single large FET

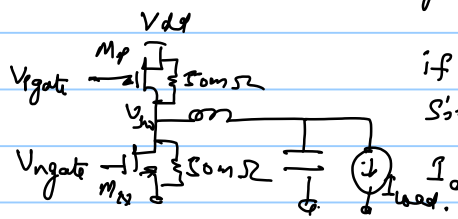
Turn OFF number of MOSFETs as load current reduces.

Let's say, we have 10 FETs.

10 in parallel = 10pF Cap.

1 FET → 1pF

③ Dead Time Switching Losses

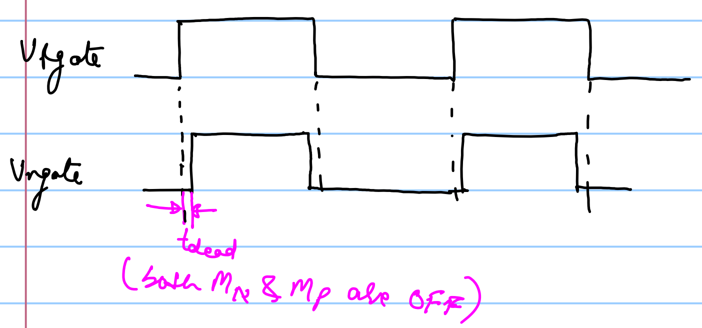


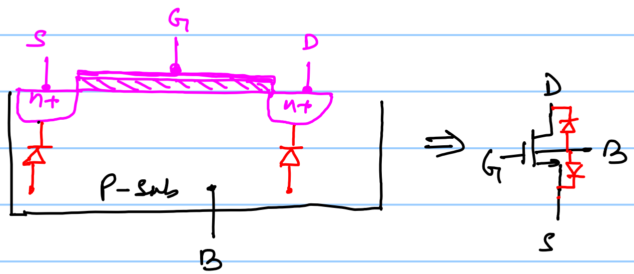
if M_p & M_n are turned ON simultaneously the

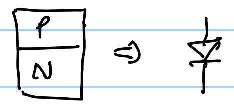
$I_{dd} = \frac{V_{dd}}{100m\Omega} = \frac{1.8V}{0.1} = 18A$ → reliability issues.

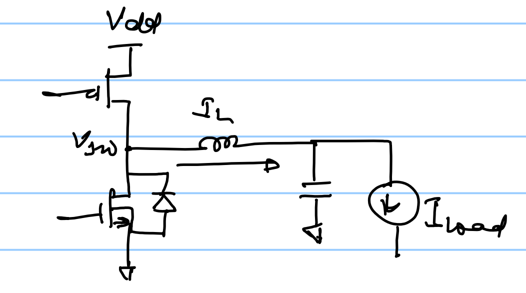
We need to make sure both M_N & M_P are not ON simultaneously.

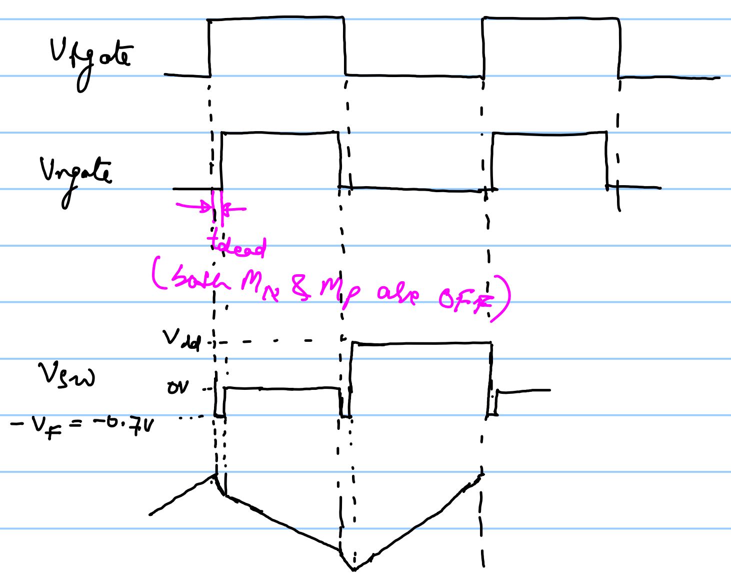
→ use non-overlapped PWM signals
(Break before Make)








Vdd
I_L
V_{sw}
I_{load}


Vpgate
Vngate
t_{dead}
(both M_N & M_P are OFF)
Vdd
V_{sw}
0V
$-V_F = -0.7V$

If ripple current is negligible compared to I_{Load}.

then

$$P_{dead\_sw} = V_F \times I_{Load} \left(\frac{t_{dead}}{T_{sw}} \right) \times 2$$

$$\boxed{P_{dead\_sw} = 2 V_F I_{Load} \frac{t_{dear}}{T_{sw}}}$$

assume, $V_F = 0.7V$

$I_{Load} = 1A$

$T_{sw} = 1\mu s$

$t_{dead} = 10ns$

$$P_{dead\_sw} = 2 \times 0.7 \times 1 \times \frac{10ns}{1\mu s}$$

$$= \frac{1.4}{100} = \frac{1400mW}{100} = 14mW$$

if $t_{dead} = 1ns$

$P_{dead\_sw} = 1.4mW$

$\Rightarrow$ we should minimize t_{dead} to increase efficiency.