

Assignment-1: EE5325 – Power Management Integrated Circuits

Submission due date: August 21, 2017

Exercise-1

In the figure shown below, derive the open and closed loop transfer functions. Find poles and zeroes of the open loop transfer function.

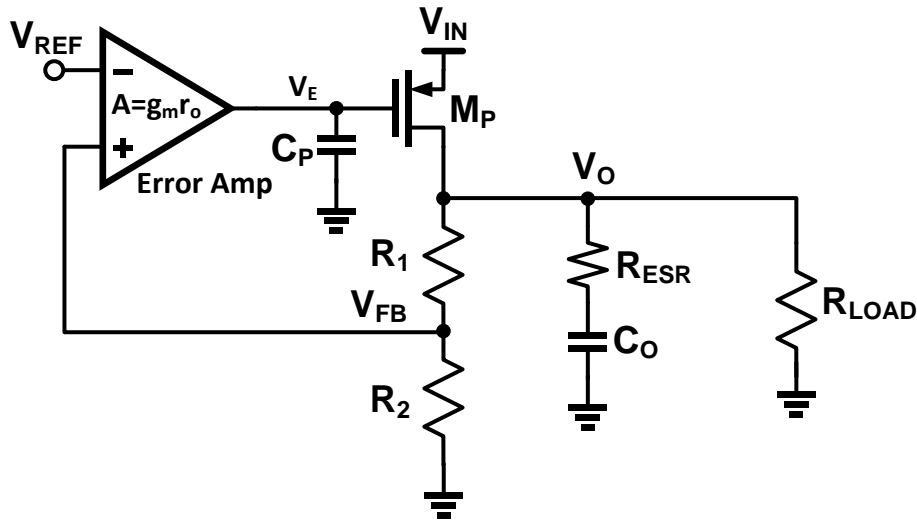


Figure-1

Considering following parameters:

$V_{REF}=0.6V$, $V_{IN}=1.8V$ to $2.5V$, $V_O=1.5V$, $R_2=100k\Omega$

Error amplifier gain, $A=60dB$ and $g_m=100\mu A/V$

g_m of PMOS transistor M_P , $g_{mp}= 1mA/V$ and output resistance, $r_{op}=\infty$

$C_P=1pF$, $C_O=1\mu F$, $R_{ESR}=10m\Omega$, $R_{LOAD} = 1k\Omega$

- Calculate the locations of poles and zeroes of the loop gain. Draw the bode plot for magnitude and phase with phase margin. Determine if the loop is stable or not.
- If op-amp has offset of $-10mV$, find error in the output voltage, V_O .
- Suppose measured V_O was $1.55V$, find the input referred offset.
- Find error in the output voltage due to finite gain.

Exercise-2

Figure-2 shows the conceptual circuit of a PTAT voltage reference:

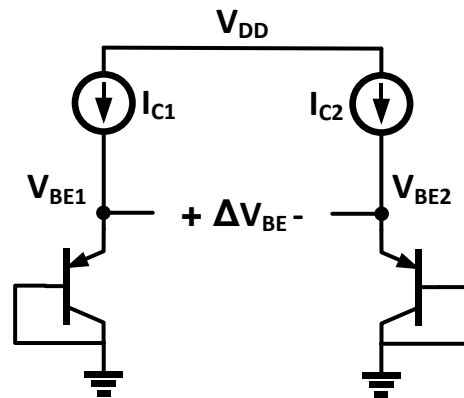


Figure-2

- Assuming Q1 and Q2 identical ($m=1$) and $I_{C1}=3I_{C2}$, plot V_{BE1} , V_{BE2} and ΔV_{BE} w.r.t. Temperature from -40°C to 120°C . What is the temperature coefficients (dV/dT) for the three voltages? Plot the temperature coefficients w.r.t. temperature and comment on non-linearity if there is any.
- Assuming Q1 and Q2 non-identical ($m=20$) and $I_{C1}=I_{C2}$, plot V_{BE1} , V_{BE2} and ΔV_{BE} w.r.t. Temperature from -40°C to 120°C . What is the temperature coefficients (dV/dT) for the three voltages? Plot the temperature coefficients w.r.t. temperature and comment on non-linearity if there is any.
- Assuming Q1 and Q2 non-identical ($m=5$) and $I_{C1}=2I_{C2}$, plot V_{BE1} , V_{BE2} and ΔV_{BE} w.r.t. Temperature from -40°C to 120°C . What is the temperature coefficients (dV/dT) for the three voltages? Plot the temperature coefficients w.r.t. temperature and comment on non-linearity if there is any.

Note:

- For Exercise-2, circuit should be analyzed and plotted on simulator (Cadence, LTSpice, etc.). You can use bipolar transistor model if available or a p-n diode. If size of bipolar or diode can't be changed in the parameter then use multiple devices in parallel.