EE5320: Analog Integrated Circuit Design; Assignment 8

Nagendra Krishnapura (nagendra@iitm.ac.in)

due on 27 April 2015

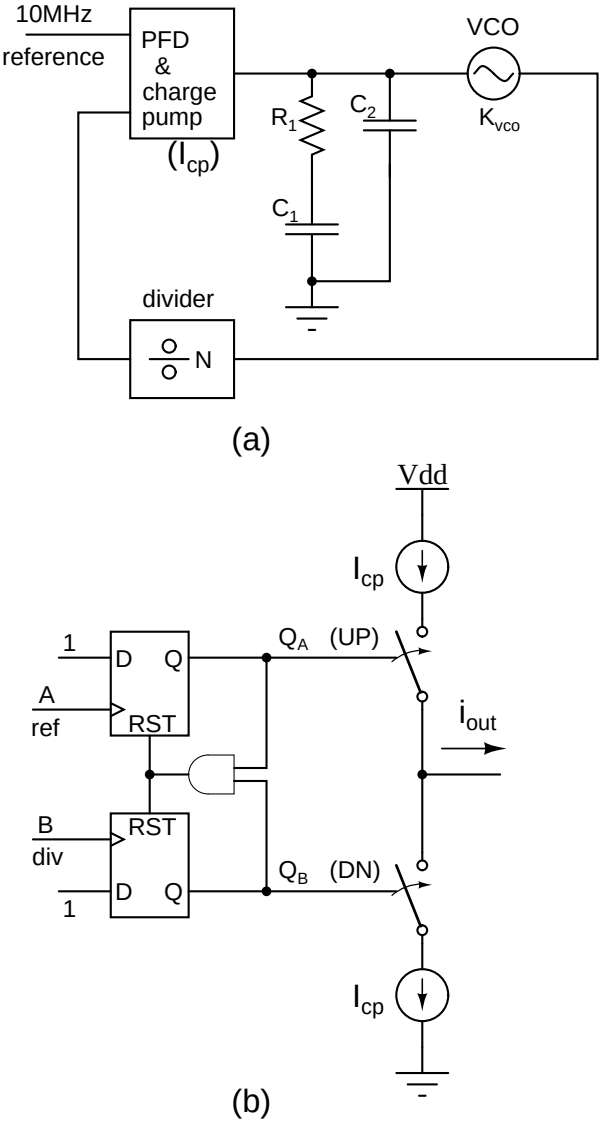

Figure 1:

1. Fig. 1(a) shows a phase-locked loop which multiplies a 10 MHz reference up to 1 GHz. The charge pump details are shown in Fig. 1(b). $K_{VCO} = 100$ MHz/V; $I_{CP} = 100\,\mu$A; $R = 10\,$kΩ; $C_1 = 10$ nF; $C_2 = 0$;

   Determine the loop bandwidth and the location of the loop-gain zero.

   Determine C_2 such that the phase margin is degraded by no more than 5° compared to the original. Determine the extra attenuation (in $\phi_{out}(s)/\phi_{ref}(s)$) at the reference frequency due to the addition of this value of C_2.