Analog Circuits (EE3002/EE5310) : Problem Set 1

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Problem 1

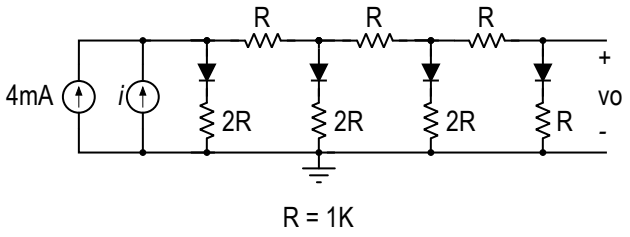

Figure 1: Circuit for problem 1.

In Fig. 1, i is a small signal. Determine the quiescent voltage across the terminals marked vo. To do this, approximate the diode characteristic by a piecewise linear one, by assuming that the voltage drop across a forward biased diode is 0.65 V.

Determine the incremental resistance of every diode in the circuit. Then, determine the small signal voltage across the terminals marked vo. What is the incremental resistance seen by the small-signal current source?

Problem 2

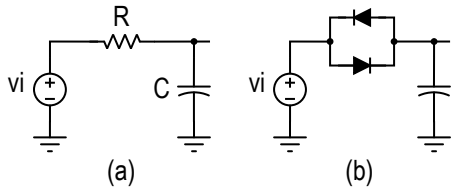

Figure 2: Circuit for problem 2.

One would think that a diode is only useful when it is forward biased (when it behaves like a closed switch), or when operating in reverse-bias (where it behaves like an open switch). This problem illustrates a practical application of a diode when it is neither forward or reverse biased. In integrated circuits, it is often desired to "low-pass filter" a small signal with a filter having a very small bandwidth. In both circuits above, vi is the "small" signal that needs to be filtered with a very low bandwidth filter, say 100 Hz.

A straightforward way of doing this is to use an RC circuit as shown in Fig. 2(a). Assuming the largest resistor that can be realized on an integrated circuit is 1 MΩ (constrained by how much space you want to "waste" on the chip), determine the capacitance C needed to achieve the bandwidth of 100 Hz. Assuming that the density of capacitance per unit area is 10 fF/μm^2 (1 femto = 10^{-15}), determine the area occupied by the capacitor.

Consider now the circuit of Fig. 2(b), where the diodes are characterized by an i-v relationship

$$I_d = I_s \left(e^{\frac{V_d}{V_T}} - 1 \right). \tag{1}$$

where $I_s = 10^{-13}$A. Determine the value of capacitance needed to achieve a low-pass filter with bandwidth 100 Hz. How much chip-area have the diodes saved?

Problem 3

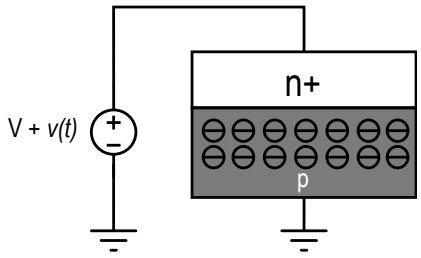

Figure 3: n+p junction in problem 3.

A *linear* capacitor is one where the charge on the plate is *linearly* proportional to the applied voltage, i.e., $Q = CV$. A nonlinear capacitance, on the other hand, has a q-v characteristic given by $Q = f(V)$, where $f(\cdot)$ is a nonlinear function of its argument. Analogous to the way the *incremental* resistance of a nonlinear two-terminal element is defined as the ratio of the *change* in voltage across the element to the *change* in current through it, one can similarly define the incremental capacitance of a nonlinear capacitor as the ratio of the *change* in charge to the *change* in voltage across the capacitor.

The charge stored in a reversed-bias n+p junction with cross-sectional area A, as you have learned in another course, is given by

$$Q = A\sqrt{2q\epsilon_s N_A}\sqrt{\phi_{bi} + V} \tag{2}$$

where V is the reverse-bias voltage, and other terms have their usual meanings. Determine the incremental current flowing into a junction, reverse biased at V, with a small-signal voltage $v(t)$ superposed on it, as shown in Fig. 3.

Problem 4

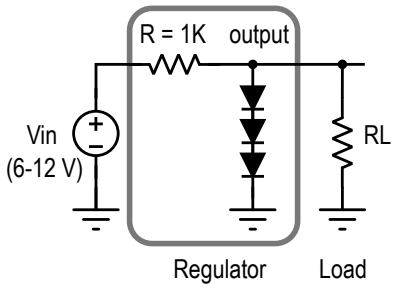

Figure 4: Voltage regulator of problem 4.

A voltage *regulator* takes as an input a high-voltage input that can vary widely, and generates an output voltage that remains constant, irrespective of the input voltage, or the load current drawn. The circuit of Fig. 4 shows a crude voltage regulator made with diodes. The input voltage can vary over the range 6 V–12 V. The three diodes are identical. The load is represented by the resistor RL, and can vary from 5 KΩ to ∞. When $RL = 10$KΩ, and $Vin = 9$ V, the output voltage is 2 V.

a. Determine the saturation current of the diodes.

b. Determine the minimum and maximum values that the output can ever take, for the given ranges of Vin and RL.

c. Determine the *line regulation* of the regulator, which is the ratio of the change in output voltage when Vin varies from 6 V to 12 V (with $RL = 10$KΩ) to the nominal output voltage (i.e, when $Vin = 9$ V).

d. Determine the *load regulation* of the regulator, which is the ratio of the change in output voltage when RL varies from 5KΩ to ∞ (with $Vin = 9$ V) to the nominal output voltage.

Problem 5

In this problem, we delve deeper into the notion of small signal. Consider two nonlinear amplifiers, with input-output characteristics given by $V_{out} = V_{in}^2/V_A$ and $V_{out} = V_A \exp(V_{in}/V_A)$. An incremental gain of 10 is desired of both amplifers.

a. Determine the operating points so that this gain may be achieved.

b. We saw in class that the small signal approximation is valid only when the higher order terms in the Taylor series can be safely neglected in relation to the linear term. Compare the second order derivative of the two amplifers around the operating point. What can you say about the relative magnitudes of the incremental inputs for each of the amplifiers which qualify as small signals?

Problem 6

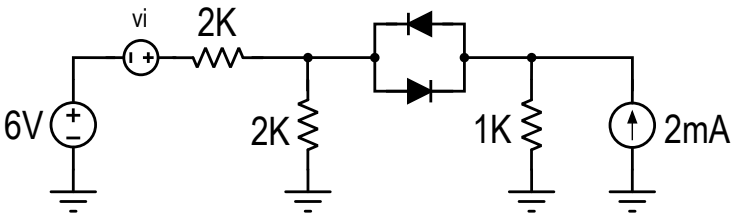

Figure 5: Circuit for problem 6.

For the circuit of Fig. 5, assume that vi is an incremental voltage source. Determine the operating point of the network. Find also the small signal voltage across the 1 KΩ resistor.

Problem 7

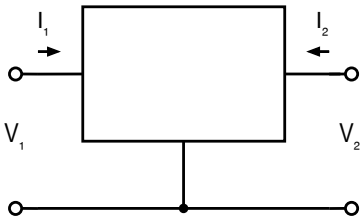

Figure 6: Circuit for problem 7.

Fig. 6 shows a nonlinear, three-terminal two-port network. It is characterized by

$$I_1 = \alpha V_1, I_2 = \beta V_1^2 + \gamma V_2 \tag{3}$$

where α,β and γ are positive constants with appropriate dimensions.

a. Draw the input and output characteristics of this device.

b. Determine the incremental y-parameters of this two port at an operating point (V_1, V_2).

Problem 8

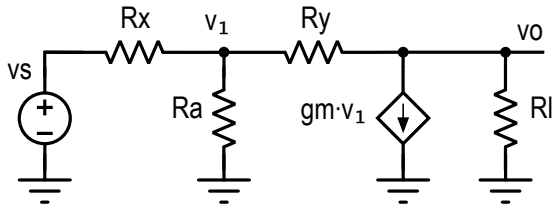

Figure 7: Circuit for problem 8.

For the circuit of Fig. 7, determine the gain vo/vs. Evaluate the limit of this gain as $gm \to \infty$.

Problem 9

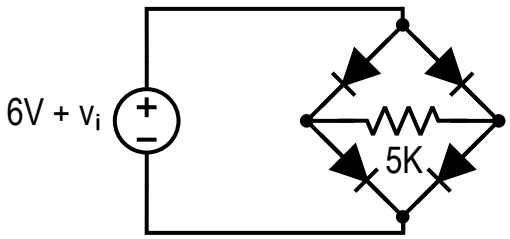

Figure 8: Circuit for problem 9.

For the circuit of Fig. 8, determine the incremental voltage across the 5 K resistor. To find the operating point, assume that the cut-in voltage of a forward-biased diode is 0.65 V. Assume that vi is a small signal.

Problem 10

For the circuit of Fig. 9, determine the current though the diode. To find the operating point, assume that the cut-in voltage of a forward-biased diode is 0.6 V. A small signal voltage vi is inserted in series with the 5 V dc source. Determine the *total* voltage at the node marked **B**.

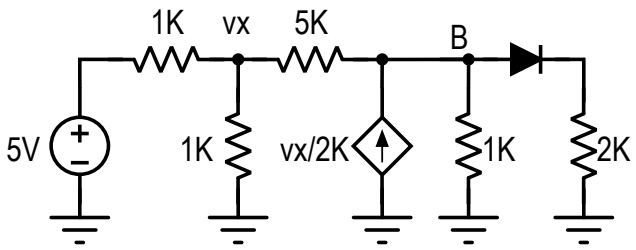

Figure 9: Circuit for problem 10.

Problem 11

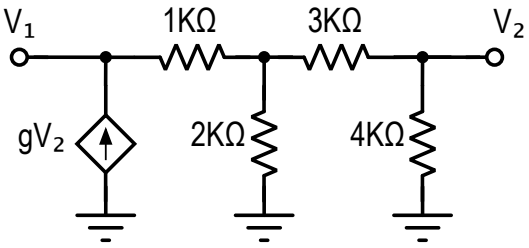

Figure 10: Circuit for problem 11.

What do you understand by the term "unilateral two-port"? What constraints does it impose on the y-matrix?

The circuit of Fig. 10 is a unilateral two-port. Determine g.