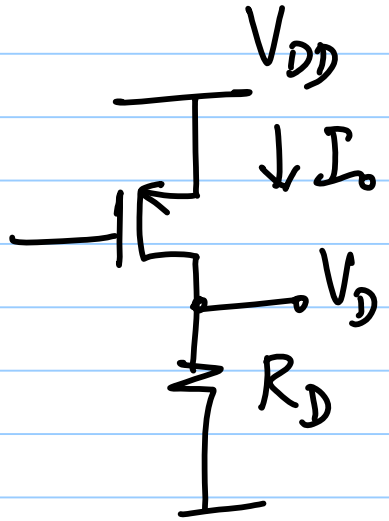
13/9/19

Lec 20

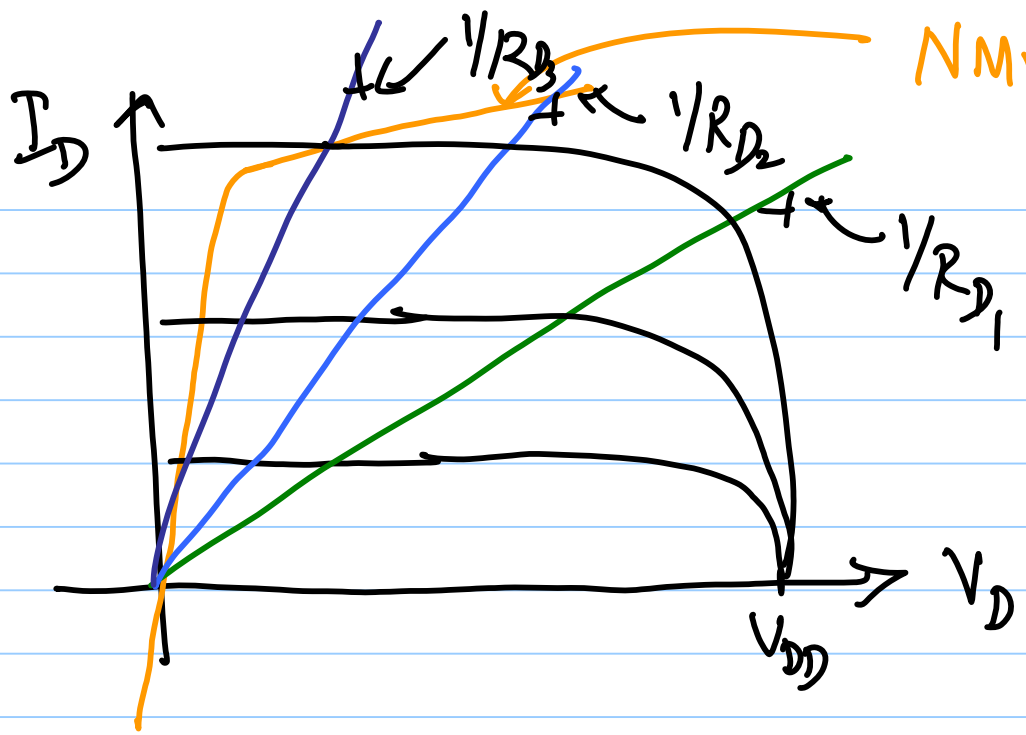


incr. gain $= -g_{m_p} \cdot R_D$

↑ gain ① → ↑ R_D ⇒ V_D ↑ ⇒ PMOS goes towards triode

③ ② → ↑ I_o ⇒ V_D ↑ ...

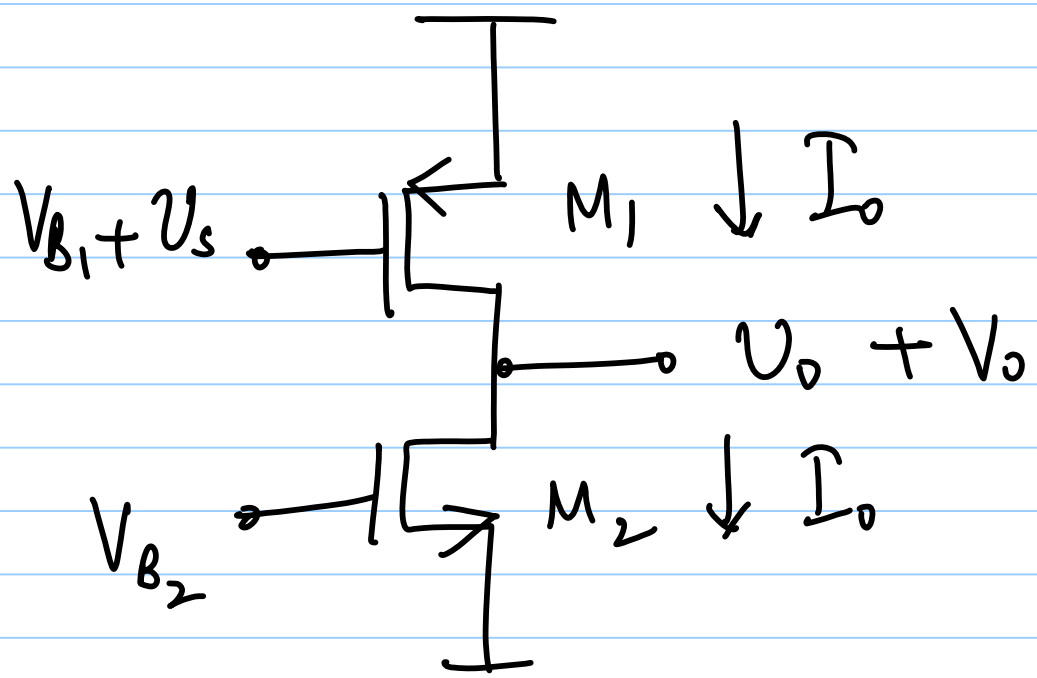
→ ↑ $\left(\frac{W}{L}\right)$ ⇒ $(V_{as} - V_T)$ ↓ ⇒ PMOS moves away from square law; slower circuit

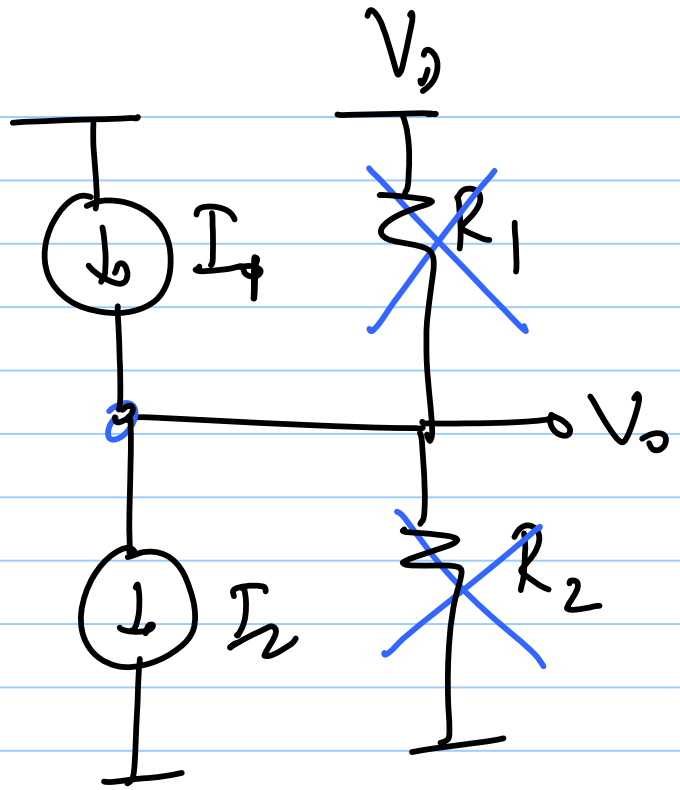


NMOS device char.

$$V_D = I_D \cdot R_D$$

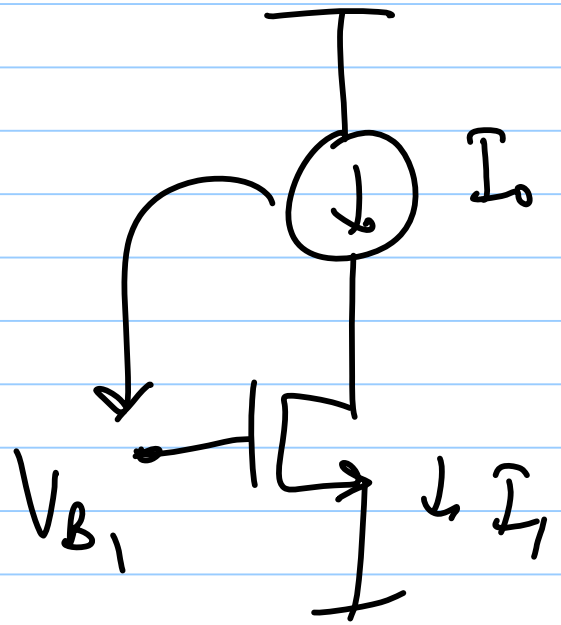
$$R_{D_1} > R_{D_2} > R_{D_3}$$

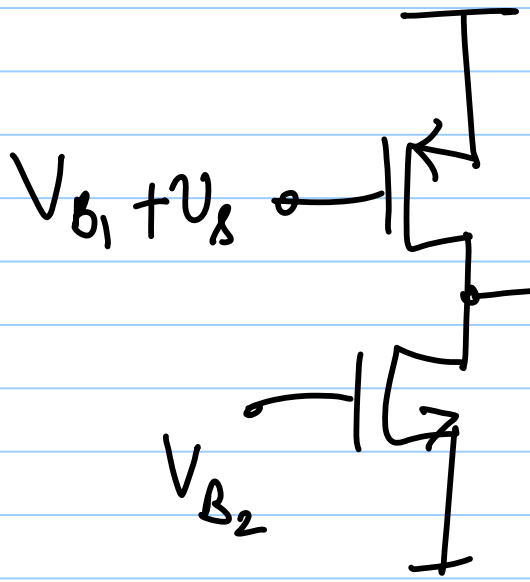

$V_{B_1} + v_s$
M_1
I_0
$v_o + V_o$
V_{B_2}
M_2
I_0



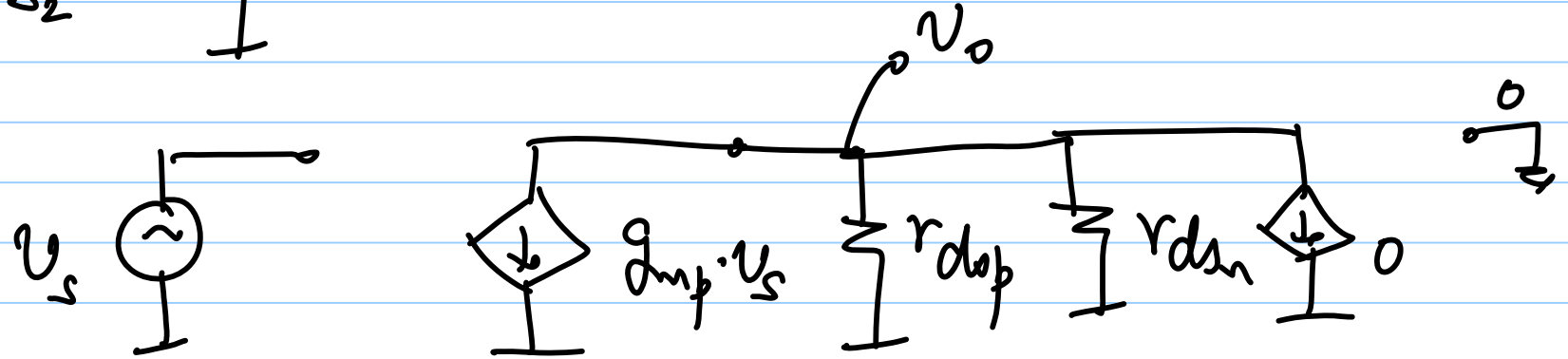
$$I_1 = m_1 \cdot V_o + c_1$$

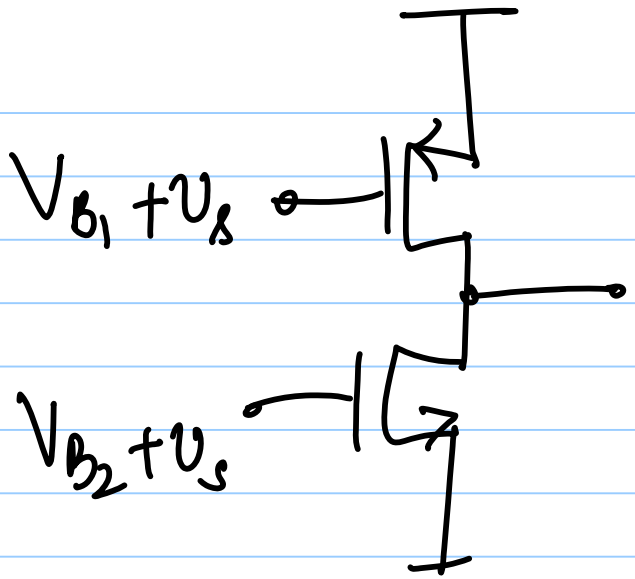
$$I_2 = m_2 V_o + c_2$$


I_0
V_{B_1}
I_1

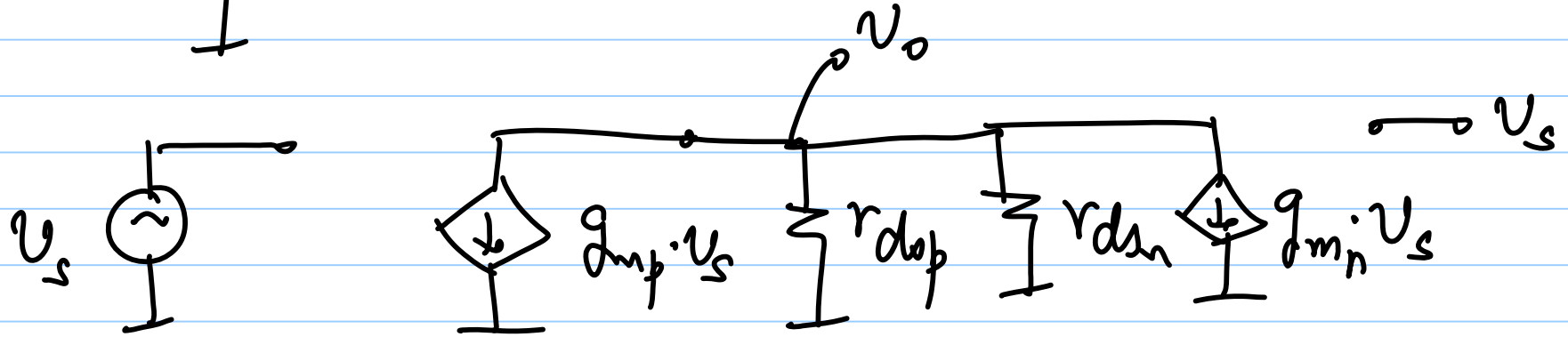


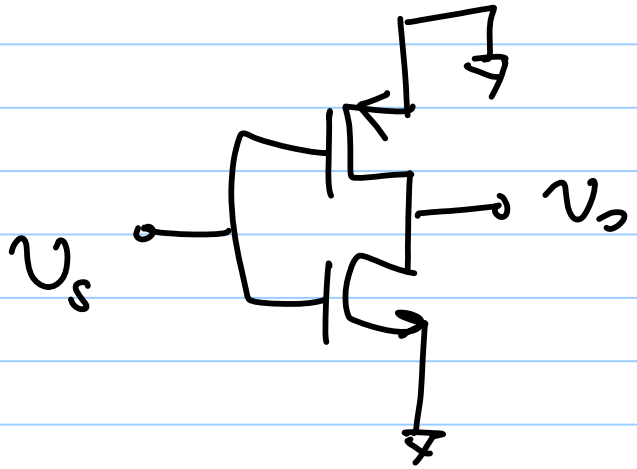
$$\frac{v_o}{v_s} = -g_{m_p}(r_{ds_p} \| r_{ds_n})$$

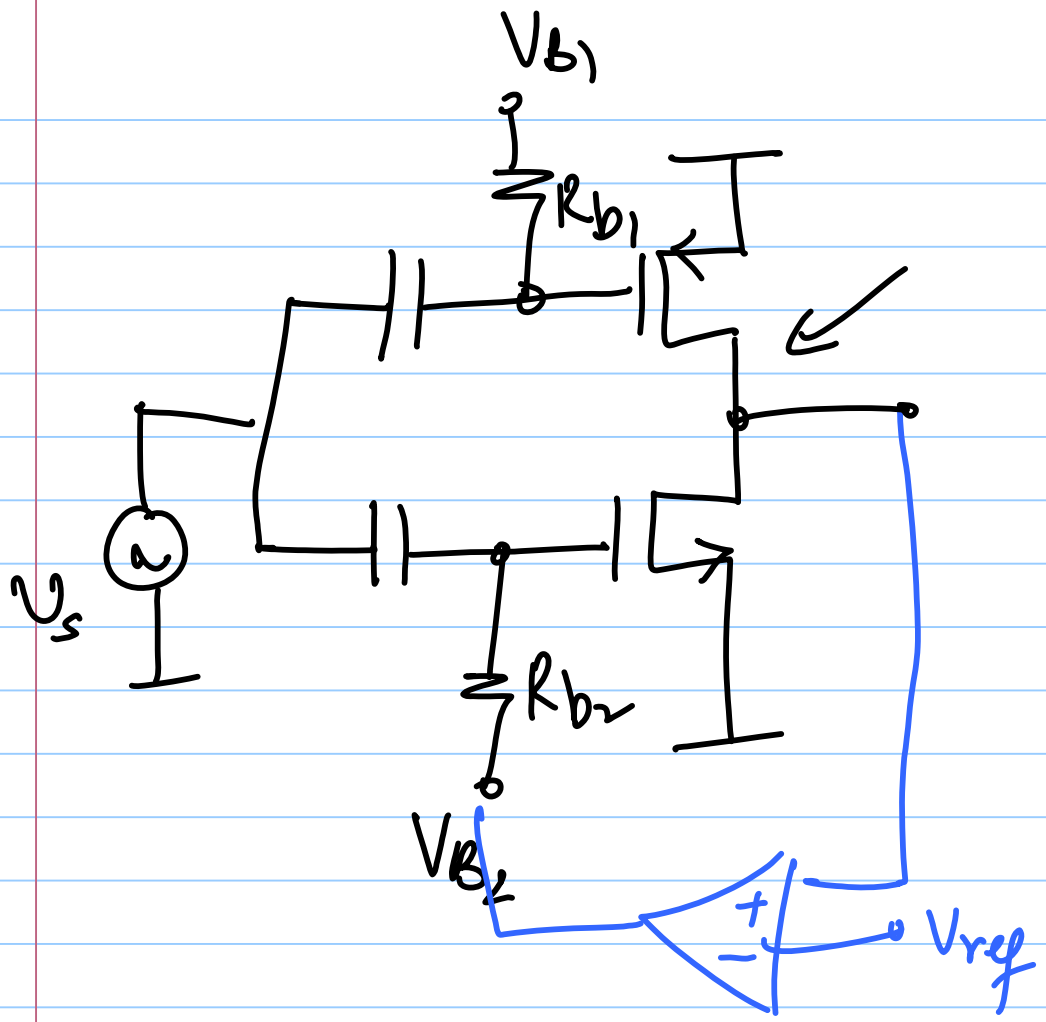


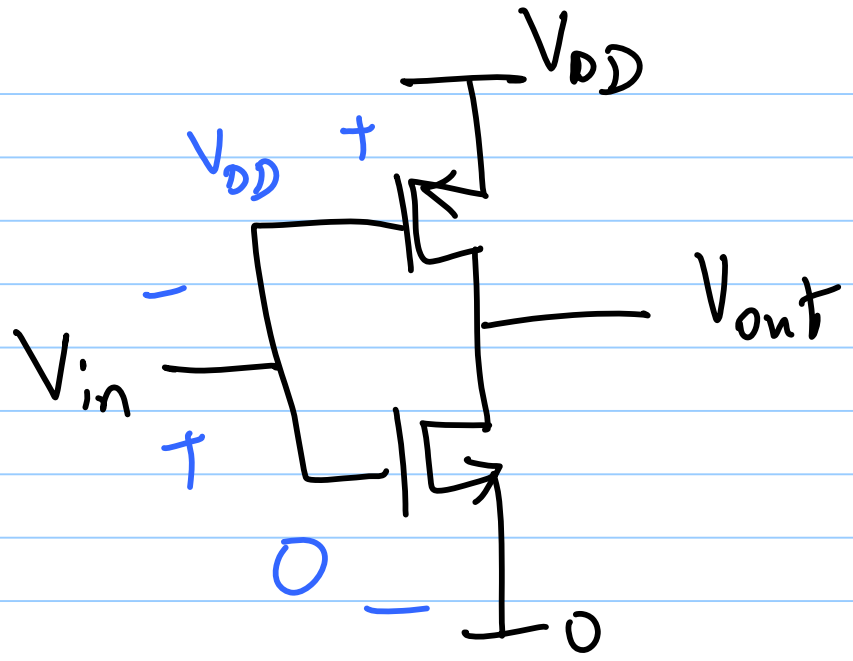


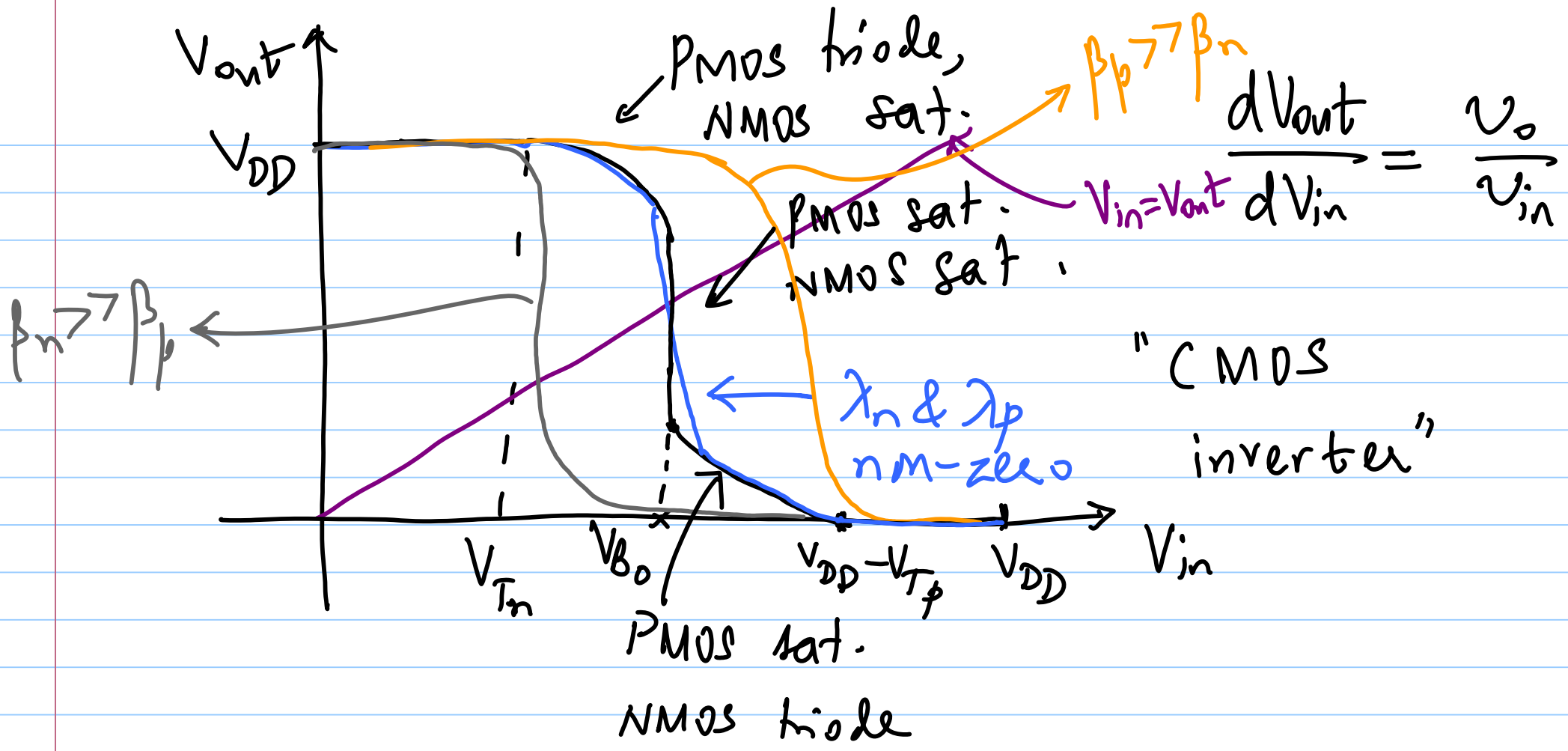
$$\frac{v_o}{v_s} = -\left(g_{m_n} + g_{m_p}\right) \cdot \left(r_{ds_n} \| r_{ds_p}\right)$$






V_{b1}
R_{b1}
v_s
R_{b2}
V_{B2}
+
−
V_{ref}


V_{DD}
V_{DD}
+
−
V_{in}
+
V_{out}
0
−
0


Vout
VDD
PMOS triode,
NMOS sat.
βp >> βn
dVout/dVin = vo/vin
Vin=Vout
PMOS sat.
NMOS sat.
βn >> βp
λn & λp
non-zero
"CMOS
inverter"
VTn
VBo
VDD-VTp
VDD
Vin
PMOS sat.
NMOS triode