Analog Circuits (EE3002/EE5310): Problem Set 8 shanthi@ee.iitm.ac.in

Problem 1

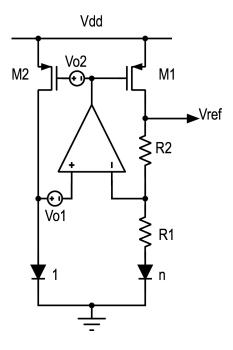


Figure 1: Circuit for problem 1.

In the bandgap reference generator of Fig. 1, all transistors operate in saturation. The incremental output resistances of M1 and M2 may be assumed to be infinite. Assume that the temperature coefficient of the diode with size 1 is -2 mV/K. The opamp is ideal. Assume that the gate-overdrive voltages of M1 and M2 are V_{ov} .

- a. Determine the ratio R2/R1 for Vref to have zero temperature coefficient (ZTC). Assume Vo1 and Vo2 are zero.
- b. Assuming that R2/R1 is the value you found in part (a), determine the effect of opamp offset voltage Vo1, and threshold mismatch Vo2 between M1 and M2. To simplify analysis, assume that Vo1 and Vo2 are small signals.

Problem 2

In the bandgap reference generator of Fig. 2, all transistors operate in saturation. The incremental output resistances of M1 and M2

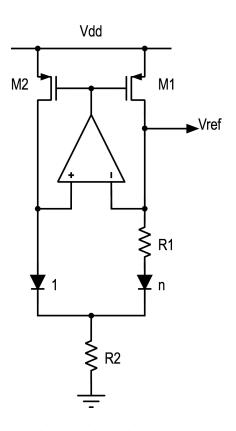


Figure 2: Circuit for problem 2.

may be assumed to be infinite. Assume that the temperature coefficient of the diode with size 1 is $-2 \,\text{mV/K}$. The opamp is ideal. Determine the ratio R2/R1 to achieve a Vref with ZTC.

Problem 3

For all transistors, use $\mu_n C_{ox}=200~\mu\text{A/V}^2$, $\mu_p C_{ox}=50~\mu\text{A/V}^2$, $V_{TN}=V_{TP}=0.1~\text{V}$. Use $\lambda=0$. The (W/L)s of the devices are marked next to them. Assume that the voltage across the diode of size 1 is 0.6~V and $(kT/q)\log_e 8=54~\text{mV}$ at 300~K.

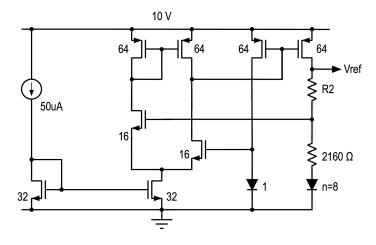


Figure 3: Circuit for problem 3.

Determine R2 to achieve a zero TC for Vref. For this R2, determine the voltage at every node in the circuit. What is the minimum Vdd that can be used while still allowing all transistors to operate in saturation?

Problem 4

Repeat problem 2 for the circuit of Fig. 4.

Problem 5

What should a be to achieve and output with ZTC? What is the reference voltage achieved? As usual, assume that all transistors are in saturation, and have infinite output resistance.

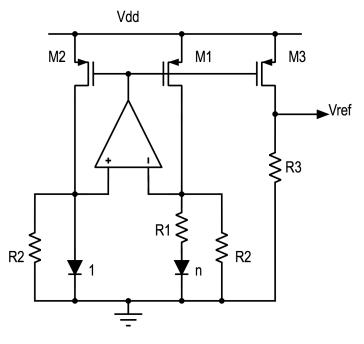


Figure 4: Circuit for problem 4.

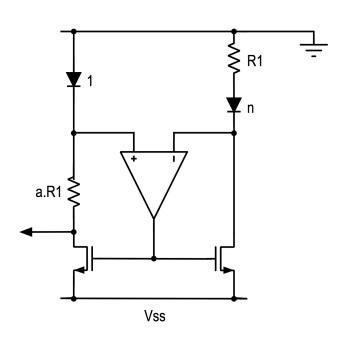


Figure 5: Circuit for problem 5.