EE5310 Analog Electronic Circuits
Opamp Simulation Project
Due 5pm Friday, November 17th, 2017

0.18µm technology parameters:
V_{Tn} = 0.5V; V_{Tp} = 0.5V; $\mu_n C_{ox}$ = 300 µA/V^2; $\mu_p C_{ox}$ = 75 µA/V^2; V_{dd} = 1.8V; L_{min} = 0.18µm; W_{min} = 0.24µm;

For all MOS transistors, use $A_d = A_s = 2WL_{min}$; and $P_d = P_s = 2(W + 2L_{min})$ in simulations.

As part of this project, you are asked to design a two-stage opamp with Miller compensation (dominant-pole), which should be used to make a non-inverting amplifier of gain 2 and a closed-loop -3dB bandwidth of f_b = 5MHz when loaded with a parallel impedance of a resistor R_L and capacitor C_L. The values of the load are given in the table below.

The phase margin of the closed loop circuit should be 60º. Minimize the value of Miller capacitors in all loops. Use zero cancelling resistors in series with miller capacitors.

Roll No.	Input pair	C_L (pF)	R_L (kΩ)
4N	pMOS	10	2.5
4N+1	pMOS	5	5
4N+2	nMOS	10	2.5
4N+3	nMOS	5	5

(1) The first part of your report should be your hand-design, and you should tabulate all calculated values as required in section (2).

(2) Tabulate the following from your simulated design:

(a) W, L and operating points (g_m, g_{ds}, V_{GS} -V_T, I_D) of all transistors. Use transistor names as follows: M_0 = input stage current source; $M_{1\text{-}2}$ = input differential pair; $M_{3\text{-}4}$ = current mirror active load; M_5 = second stage amplifier; M_6 = second stage current source.

(b) Values of other components in the opamp.

(c) DC gain of the opamp.

(d) Power consumption.

(3) Plot the following: (choose appropriate axes limits and font sizes for plotting. Illegible plots do not get any credit).

(a) Loop gain - magnitude and phase; Indicate the phase margin.

(b) Closed loop gain - magnitude and phase; Indicate the -3dB bandwidth.

(c) Transient response of the closed-loop amplifier with a 0.2V differential step (use 0.1ns rise/fall times).

(d) Transient response of the closed-loop amplifier with a 0.1V common-mode step (use 0.1ns rise/fall times).

Do not use an ideal current sources in the tail. You can use one ideal reference current source of 1/10th the tail current of the input differential pair for bias generation. Design the bias generator block that generates bias currents and voltages required in the opamp.Try to determine as many parameters as possible from the specifications and choose sensible starting points for the others. You can assume a gate overdrive of 200mV in your initial calculations. Make sure to use replicas correctly (i.e. same transistor length) wherever applicable.