EE5310/EE3300: Analog Circuits; Tutorial 7

Nagendra Krishnapura (nagendra@iitm.ac.in), Aniruddhan S. (ani@ee.iitm.ac.in)

Due on 16th November 2015

For the following problems, use the data below:
$\mu_n C_{ox} = 100\mu\text{A}/V^2$, $\mu_p C_{ox} = 25\mu\text{A}/V^2$, $V_{Tn} = V_{Tp} = 1\,\text{V}$; $\lambda_n = \lambda_p = 0$ unless otherwise mentioned.

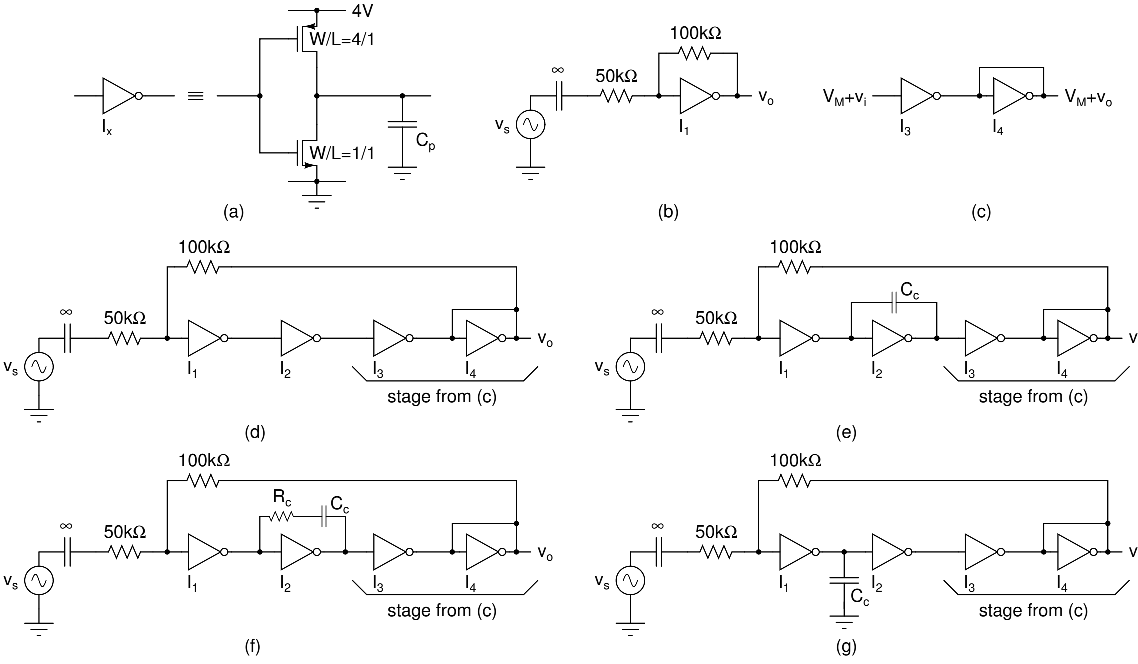


Figure 1: (a) CMOS inverter with a 4 V supply, (b)-(g) Circuits for Problems 2 to 8. The capacitor marked ∞ is large enough to be a short at arbitrarily low frequencies.

Determine the small signal model of the inverter in Fig. 1(a) and use it in the problems below. The output parasitic capacitor $C_p = 100\,\text{fF}$. Use it with the inverter only when mentioned.

1. Determine the closed loop $V_o(s)/V_s(s)$ of the amplifier in Fig. 1(b). What is the dc gain? and how does it compare to the dc gain if the transistor W/L ratios in the inverter are *very* large? What is the -3 dB bandwidth f_{3dB} in Hz? Determine the loop gain by breaking the loop at the input of I_1 and determine the unity loop gain frequency $f_{u,loop}$ in Hz and phase margin ϕ_M in degrees. How is $f_{u,loop}$ related to f_{3dB}?
2. What is v_o/v_i in Fig. 1(c)? Ignore C_p in this case.
3. To improve the loop gain, an additional inverter I_2 is added into the loop as shown in Fig. 1(d). The stage from Fig. 1(c) is also added into the loop (*why?*). Considering C_p only for $I_{1,2}$, determine $V_o(s)/V_s(s)$ of the amplifier in Fig. 1(d). What is the natural frequency? What is the quality factor?

4. To stabilize the amplifier, C_c is added as shown in Fig. 1(e). Again considering C_p only for $I_{1,2}$, determine $V_o(s)/V_s(s)$ and adjust C_c such that the quality factor is unity (damping factor of 0.5). What is the natural frequency f_n in Hz?

   With the value of C_c calculated above, determine the loop gain by breaking the loop at the input of I_1 and find the unity loop gain frequency $f_{u,loop}$ in Hz and phase margin ϕ_M in degrees. How is $f_{u,loop}$ related to f_n?

5. Now include C_p for all four inverters and repeat 4. Closed loop transfer functions are too complicated and a single quality factor cannot be used with order > 2. Therefore, adjust C_c in this case to realize the same phase margin as in 4. For this, you have to resort to a numerical solution. One possibility is to derive the expression for loop gain, substitute all numerical values of components except C_c, and substitute s with $j\omega_{u,loop}$ (which is also a function of C_c. You can use the approximated expression for this. For systems with high dc gain, if the loop gain $L(s) = (b_0 + b_1 s + \ldots)/(a_0 + a_1 s + \ldots)$, $\omega_{u,loop} \approx b_0/a_1$—prove/verify this with known cases). Get the expression for phase margin from this, and solve for C_c numerically for the desired phase margin. Alternatively, just plot the phase margin as a function of C_c and find the answer. *Before actually doing the calculations, clearly reason out what the which way C_c should be changed from the value in 4.*

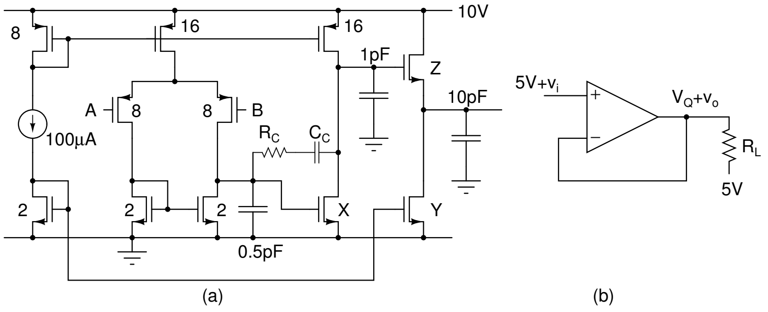
6. Now try the improved circuit in Fig. 1(f). $R_c = 1/g_{m,inv}$. Include C_p for all four inverters. Adjust C_c in this case to realize the same phase margin as in 4 using the procedure described in 5. *Before actually doing the calculations, clearly reason out what the which way C_c should be changed from the value in 5.*

   Find the unity loop gain frequency $f_{u,loop}$ in Hz, and compare it to the values in 4 and 5.

7. Try the stabilization scheme in Fig. 1(g) to obtain the same phase margin as in 4. Can you obtain a quality factor of unity for the closed loop transfer function? State your reasons clearly.

   If you can stabilize it, determine C_c, find the unity loop gain frequency $f_{u,loop}$ in Hz, and compare it to the values in 4, 5, and 6.

8. Repeat 7 with $\lambda_n = \lambda_p = 0.1/\mathrm{V}$.



(a)

(b)

Figure 2: (a) MOS opamp (numbers next to transistors are aspect ratios), (b) Unity gain voltage buffer using the opamp in (a). Ignore the capacitors for questions 9 to 14.

9. For the opamp in Fig. 2, find out which of A and B is the non-inverting input.

10. It is desired that when all devices are in saturation, the quiescent voltages at the drains of the input transistors are equal. Determine X.

11. The opamp must be able to sink or source 1 mA current. Also, it must have an open loop output resistance of $500\,\Omega$. Determine Y and Z.

12. The opamp is used to realize the unity gain buffer in Fig. 2(b). For $R_L = \infty$, determine the small signal dc gain v_o/v_i, small signal output resistance, and swing limits on v_i such that all transistors are in saturation.

13. Repeat 12 for $R_L = 5\,\mathrm{k}\Omega$ and $500\,\Omega$. What do you notice?

14. Use $\lambda_p = \lambda_n = 0.02/\mathrm{V}$ and repeat 12 for $R_L = 5\,\mathrm{k}\Omega$. What do you notice?

15. With capacitors loading each of the stages as shown in Fig. 2(a), find the values of frequency compensation components R_c and C_c to obtain a phase margin of 60°. Choose $R_c = 0$. What is the bandwidth of the unity gain buffer? Use suitable approximations everywhere.

16. Repeat 15 with R_c chosen to eliminate the right half plane zero.