

# EE2019–Analog Systems and Lab: Tutorial 5

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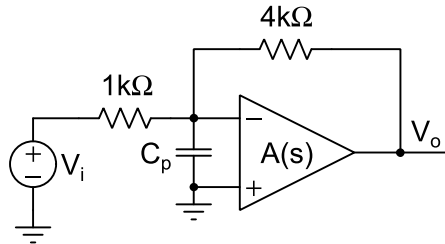


Figure 1: Circuit for problem 1

1. Fig. 1 shows an inverting amplifier. The opamp has a gain  $A(s) = A_0/(1 + s/p_1)(1 + s/p_2)$  where  $A_0 = 20000$ ,  $p_1 = 1 \text{ krad/s}$ ,  $p_2 = 10 \text{ Mrad/s}$ .  $C_p$  is a parasitic capacitor.

- What is the phase margin of the system with  $C_p = 0$ ?
- What is the closed loop bandwidth of the system? (Calculate this from (a) Unity loop gain frequency, (b) Natural frequency of the second order system, and (c) Exact calculation—computing the frequency at which the gain magnitude drops to  $1/\sqrt{2}$  times the dc gain.; Compare the estimates so obtained)
- What is the value of  $C_p$  for which the circuit becomes unstable?
- With  $C_p$  being the value calculated in the previous part, can you change the circuit so that the phase margin is  $60^\circ$  without changing the opamp or the closed-loop dc gain  $V_o/V_i$ ?

2. Fig. 2 shows a transimpedance amplifier. The opamp has a frequency independent gain  $A_0$ . The feedback resistor  $R$  has a parasitic capacitor  $C$ .  $C$  is distributed across the length of the resistor and should be modeled as shown in Fig. 2(b) where the infinite number of infinitesimal  $\Delta R$  and  $\Delta C$  sum up to  $R$

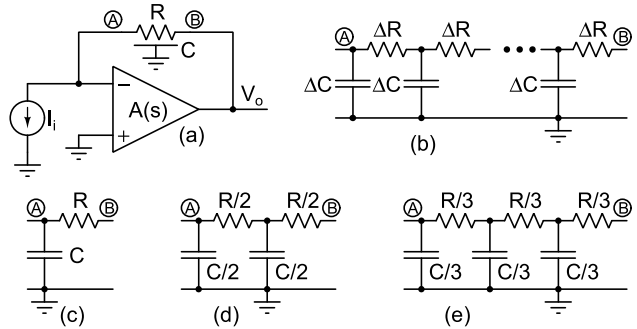


Figure 2: Circuit for problem 2

and  $C$  respectively. This cannot be analyzed easily, so we model it as shown in Fig. 2(c), (d), or (e). Analyze each case and comment on the effect of  $A_0$  on stability or damping. (In addition to stability, this problem also tells you something about oversimplified models).

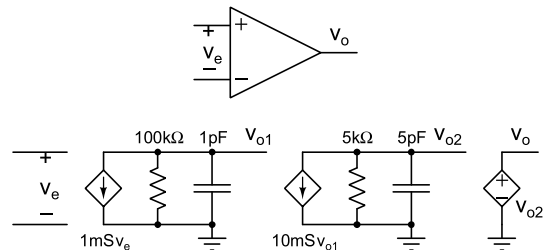


Figure 3: Circuit for problem 3

3. Fig. 3 shows the internal schematic of an opamp. This opamp is used to realize a unity gain, non-inverting amplifier.

- What is the phase margin?
- Connect a capacitor across one of the existing capacitors inside the opamp so that the phase margin is  $60^\circ$ .

Repeat the above if the opamp is used to realize an inverting amplifier of gain  $-4$ .