EE2019 Analog Systems and Lab: Problem Set 6

Problem-1

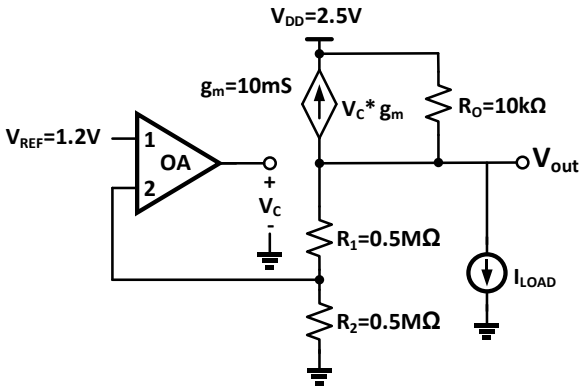

Figure 1: Circuit for Problem-1

Figure 1 shows a linear regulator. Assuming op-amp OA is ideal:

a) Determine the polarity of input terminals 1 & 2 of the op-amp for negative feedback operation.

b) Find the output voltage V_{out}.

c) Find the minimum and maximum value of V_C if I_{LOAD} varies from 1mA to 10mA.

Problem-2

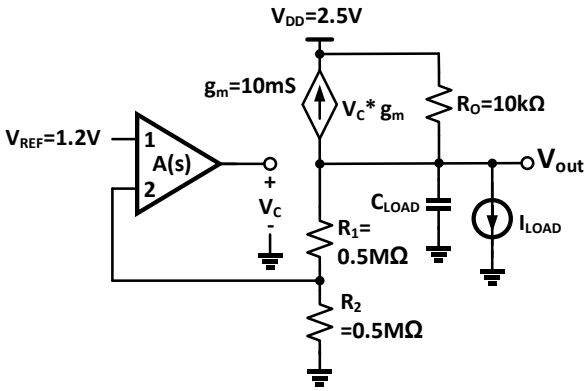

Figure 2: Circuit for Problem-2

Figure 2 shows the linear regulator of Figure 1 with a real 2-stage compensated op-amp having transfer function:

$$A(s) = \frac{100}{(1+5x10^{-6}s)(1+5x10^{-8}s)}$$

a) Assuming op-amp pole as dominant, find the maximum value of the load capacitor, C_{LOAD} to maintain the phase margin > 45º. Support your answer with bode magnitude and phase plot.

b) Is it possible to use C_{LOAD} larger than the value found in (a) and still achieve a phase margin > 45º? Support your answer with bode magnitude and phase plot.

c) Determine the value of C_{LOAD} for which phase margin becomes 0º.

d) Find the steady error in V_{out} due to finite dc loop gain.

Problem-3

Simulate the circuit of Figure 2 in LTSpice and compare the result found in Problem-2 with your simulated results. Comment on differences, if there are any. For Problem 2 (b), perform transient analysis with initial condition V_{out}=0, observe the magnitude and frequency of oscillations at V_{out} and relate the same with your loop gain analysis.

Problem-4

In class, we saw that the response of a "slow" linear time-invariant system to a rapidly varying input like v_i in Figure 4 is approximately the same as that due to v_i^. In this problem, we will convince ourselves of this by working a specific example on LTSpice simulation.

Assume that v_i has a frequency of 1 MHz, and a duty cycle of 10%. RC = 1 mS. On the same graph, plot $v_o(t)$ when the input is $v_i(t)$, and when it is v_i^(t).

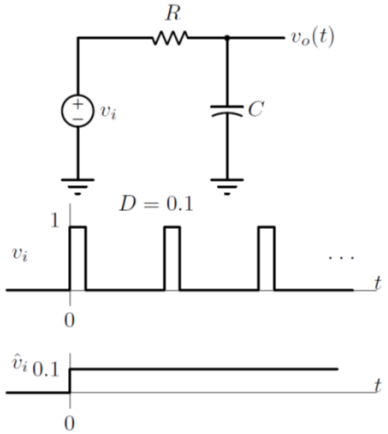

Figure 4: Circuit for Problem-4

Problem-5

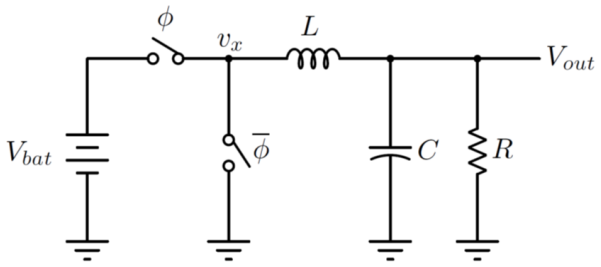

Figure 5: Circuit for Problem-5

Figure 5 shows a buck converter. The battery voltage V_{bat} is 5V. ϕ and $\bar{\phi}$ are complementary switch drive signals. The duty cycle of ϕ is denoted by D. The switching frequency is 1.5 MHz. $L = 2.2\ \mu H$ and $C = 22\ \mu F$. The load resistor $R = 10\Omega$.

a) Determine D needed to achieve $V_{out} = 3.3V$.
b) Determine the transfer function from v_x to V_{out}.
c) Using the observation that the pole frequency of the LC filter is much lower than the switching frequency, determine the ripple in the inductor current and output voltage.
d) Sketch the current waveforms in the inductor and capacitor in steady state.
e) Sketch the voltage waveform V_{out} in steady state.

Problem-6

As usual, the switching period *Ts* is much smaller than the time-constant of the LC network. S1 and S2 are controlled by complementary waveforms, and the waveform controlling S1 is shown in the figure. Determine the average output voltage *vo*, and the average current drawn from the source. Draw the steady state current and voltage waveforms through/across the inductor and capacitor.

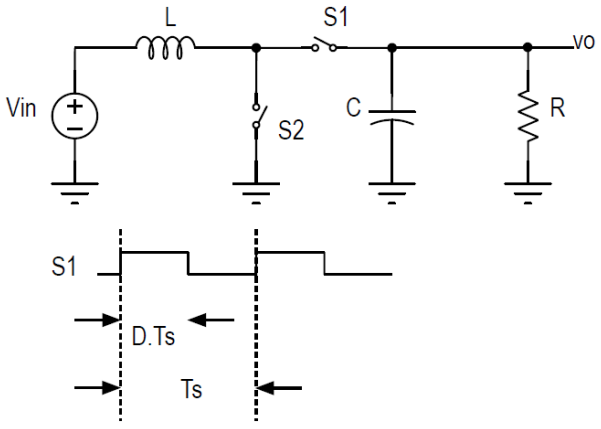

Figure 6: Circuit for Problem-6

Problem-7

Figure 7 shows the circuit diagram of a type-I (integral) compensated buck converter with output voltage, Vout regulated at 2.5V for input supply, V_{DD}=5V and load current, I_{LOAD}=1A. . Assuming switches S_P and S_N are ideal.

a) Model the buck converter in continuous time domain and find the small signal loop gain transfer function.
b) Determine the value of capacitor C_1 to achieve the gain margin of > 20dB and draw the bode magnitude and phase plot.
c) Find the value of control voltage, V_{CTRL} and duty cycle, D to regulate the output voltage at 2.5V.
d) Find the value of peak to peak inductor ripple current and peak-to-peak output ripple voltage.
e) Draw the steady state waveforms for PWM voltage (V_{PWM}), switch currents (I_P and I_N), inductor current (I_L) and output voltage (Vout).

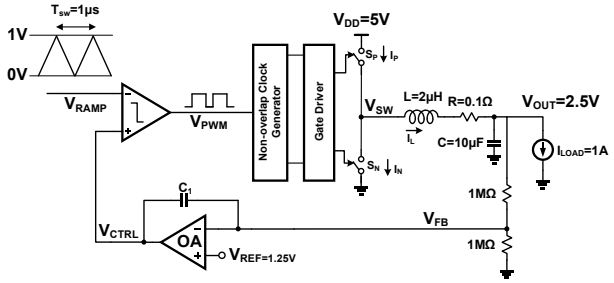

Figure 7: Circuit for Problem-7

Problem-8

Design the buck converter circuit shown in Figure 7 and its continuous time model in LTSpice.

a) Perform AC analysis and plot the loop gain magnitude and phase response of the continuous time model and verify your results found in Problem-7 (b). Observe and comment on the effect of varying capacitor (C_1) value on unity gain frequency (w_u) and gain margin. Use enough points per decade in your AC simulation to get the correct value of Q_O due to LC resonance.
b) Perform transient analysis and plot waveforms V_{CTRL} and V_{OUT} of buck converter and corresponding signals in its continuous time mode on the same graph. Verify that V_{CTRL} and V_{OUT} of the buck converter have the average value as of its continuous time model. Comment on the differences if observed any. Use initial condition V_{OUT}=0 in your transient simulation. Verify your results found in Problem 7 (c), (d) and (e).