EC5135/EC3102: Analog Circuits
Tutorial 6

$\mu_n C_{ox} = 300\,\mu\text{A}/V^2$, $\mu_p C_{ox} = 75\,\mu\text{A}/V^2$, $V_{Tn} = V_{Tp} = 0.6\,\text{V}$; $\lambda_p = \lambda_n = k_\lambda/L$, where $k_\lambda = 0.12/(\text{V}\,\mu\text{m})$

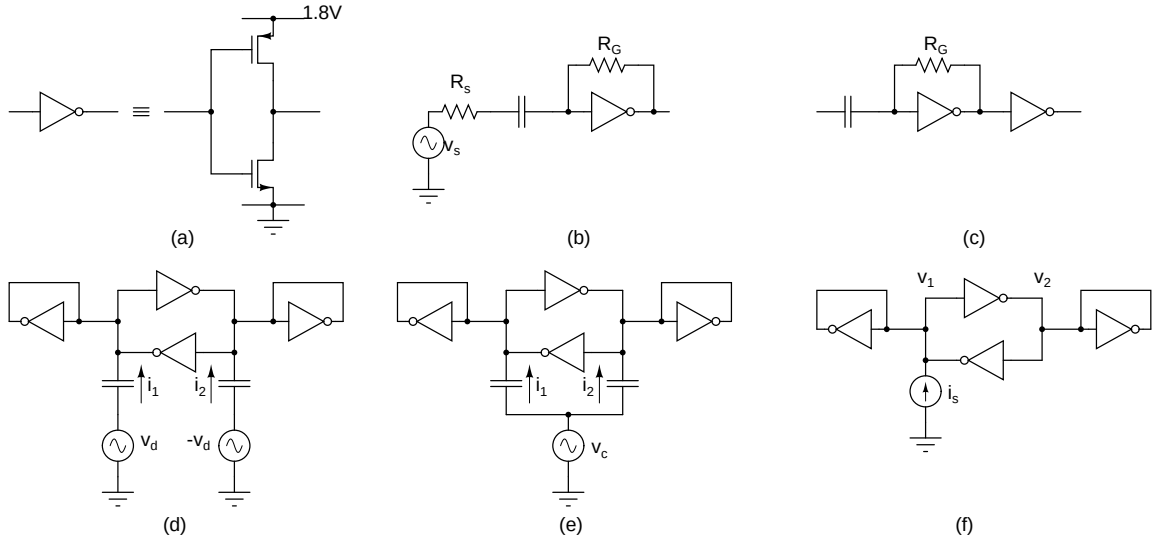

Figure 1:

1. Design the inverter in Fig. 1(a) to have a self bias voltage of 0.9 V and a quiescent current of 10 μA when self biased. W and L of all transistors are constrained to be at least 0.24 μm and 0.18 μm respectively. What is the dc gain of this inverter?

2. What is the constraint on R_G such that it doesn't affect the gain of the self biased inverter (Fig. 1(b))? Under this constraint, what are the maximum and minimum output voltages such that both transistors are in saturation?

3. The two inverters in Fig. 1(c) are identical. R_G satisfies the constraint above. What is the quiescent output voltage? What is the amplitude of the input sinusoid such that the output just reaches the swing limits calculated above?

4. What additions do you need to make to this circuit so that the small sinusoidal input can be converted to a square, (almost) digital waveform?

5. Assume that the threshold voltage of the nMOS transistor in the second inverter in Fig. 1(b) differs from the nominal value by ΔV_{Tn}. Find the value of ΔV_{Tn} for which the quiescent output voltage is half way towards the output swing limit.

6. Fig. 1(d, e) show a circuit driven by out of phase and in phase (small) signals. Calculate(symbolically) the small signal currents i_1 and i_2 in in the two cases. Comment on the magnitude of the currents in the two cases.

7. Based on the above results, calculate the small signal voltages v_1 and v_2 in Fig. 1(f). What might be the utility of this circuit?