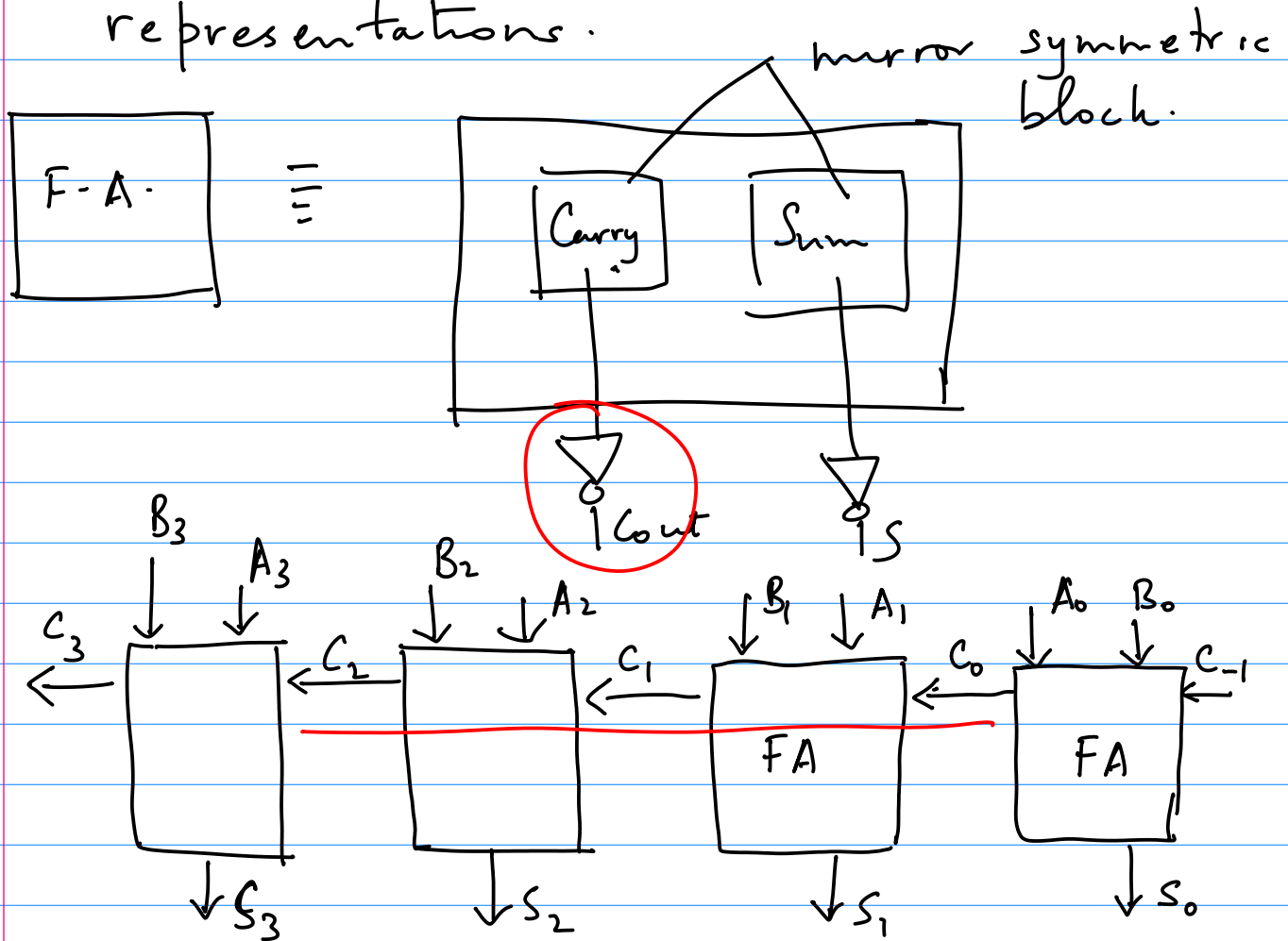


$$S(A, B, C_{in}) = ABC_{in} + \overline{C_{out}}(A + B + C_{in})$$

$$C_{out}(A, B, C_{in}) = AB + C_{in}(A + B)$$

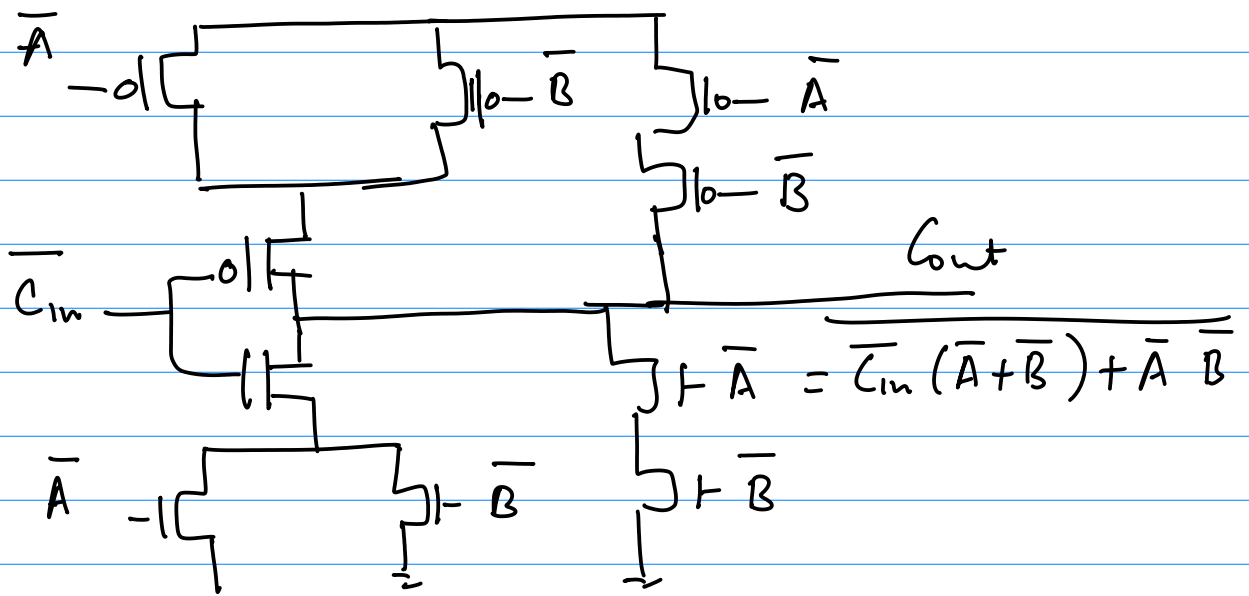
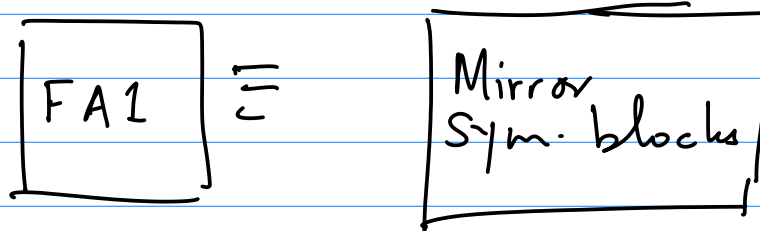
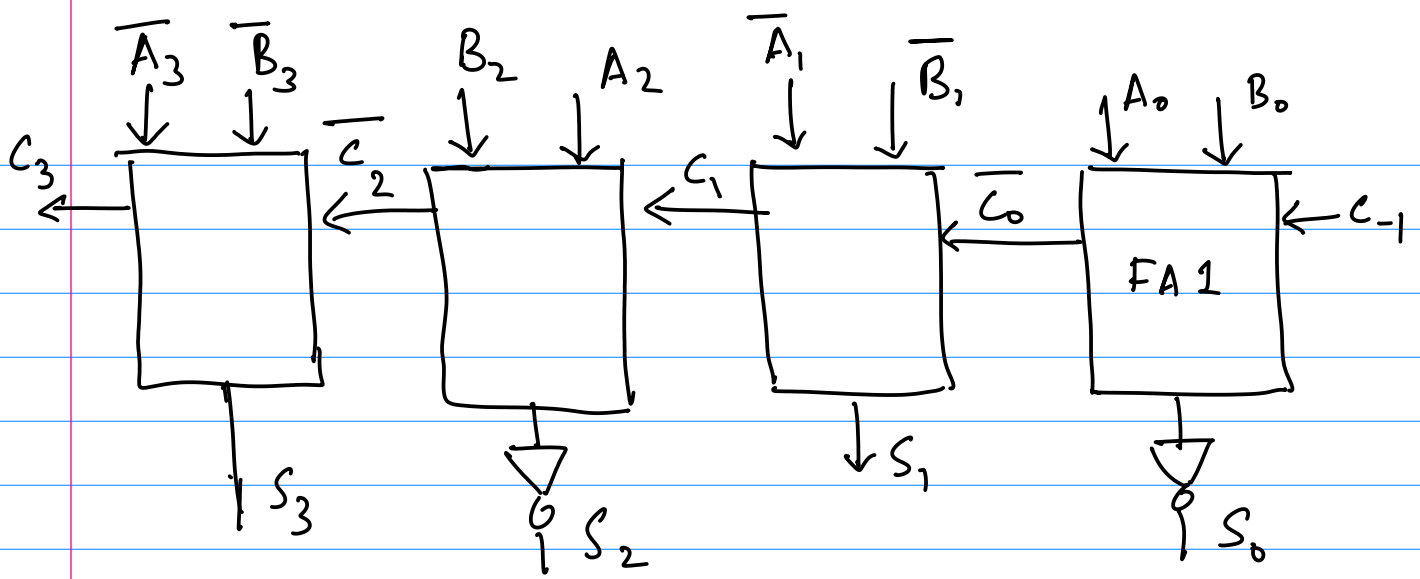
$$\begin{cases} \overline{S}(A, B, C_{in}) = S(\overline{A}, \overline{B}, \overline{C_{in}}) \\ \overline{C_{out}}(A, B, C_{in}) = C_{out}(\overline{A}, \overline{B}, \overline{C_{in}}) \end{cases}$$

Use this to get mirror symmetric representations.



$t_{inv} : 1 \text{ unit}$
 $t_{cout} : 3 + 1$
 $t_{sum} : 4 + 1$

$t = 0; A_i, B_i, (i = 0, \dots, 3), C_{-1}$
 $C_0 : t = 4 \quad C_1 : t = 8$
 $S_0 = t = 5 \quad S_1 : t = 9$
 $C_2 : t = 12 \quad C_3 : 16$
 $S_2 : t = 13 \quad S_3 : \underline{\underline{17}}$



S_3 : 13,
 C_3 : 12

Critical path:
 Carry path

Can put extra processing in inputs; optimise carry path for speed.

$$C_{out}(A, B, C_{in}) = \Sigma(3, 5, 6, 7)$$

$$\begin{array}{l} 011, 101, 110, 111 \\ \underbrace{\hspace{1.5cm}} \\ A \oplus B = 1 \quad A, B = 1 \\ C_{in} = 1 \quad C_{in} = X \end{array}$$

$$G = AB \quad (\text{Generate})$$

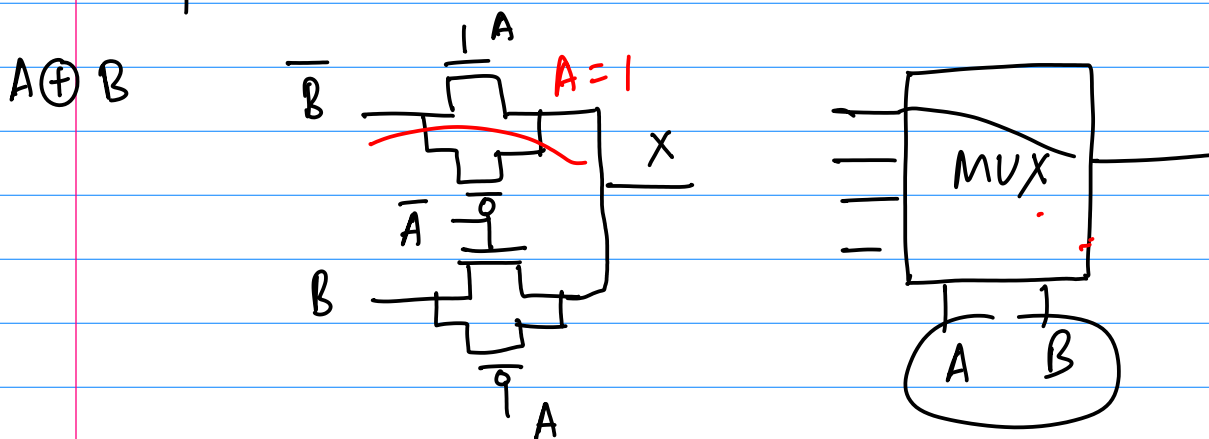
$$P = A \oplus B = A\bar{B} + \bar{A}B$$

$$C_{out} = G + PC_{in}$$

$$= \bar{P}A + PC_{in} \rightarrow$$

$$\bar{P} = \bar{A}\bar{B} + \underline{\underline{AB}}$$

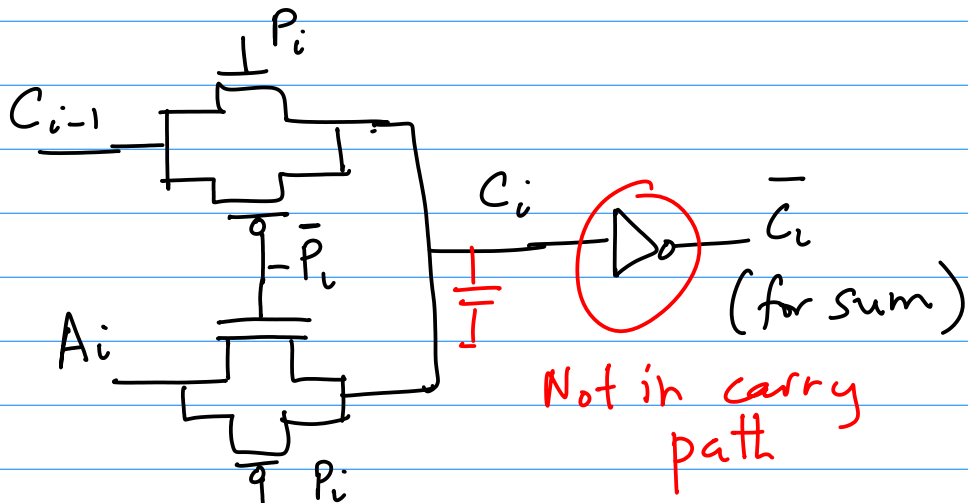
Implementation with transmission gates



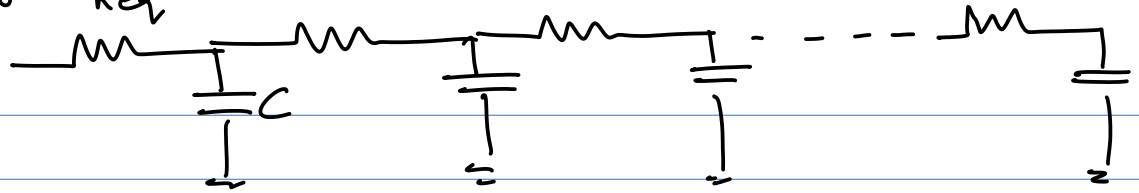
$$S = P \oplus C_{in} = P\bar{C}_{in} + \bar{P}C_{in}$$

$$t=0; \quad \underbrace{A_i, B_i}$$

$$t=2 \quad P_i \quad \forall i$$



Carry: R_{eq}

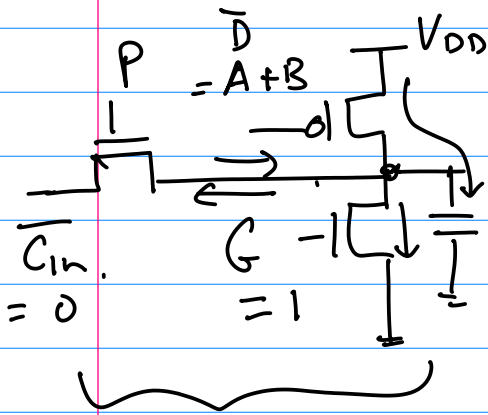


Can get very slow unless buffers are placed appropriately. (Delay $\propto N^2$ without buffers)

$$P = A \oplus B$$

$$G = AB \quad : \quad \text{carry generate}$$

$$D = \bar{A} \bar{B} \quad : \quad \text{carry kill.}$$



$$C_{out} = \sum (0, 1, 2, 4)$$

$$A, B = 1 \quad \checkmark$$

$$C_{in} = 1 \quad \checkmark$$

$$A \oplus B = 1$$

$$A, B = 0 \quad C_{in} = 0 \quad P = 1$$