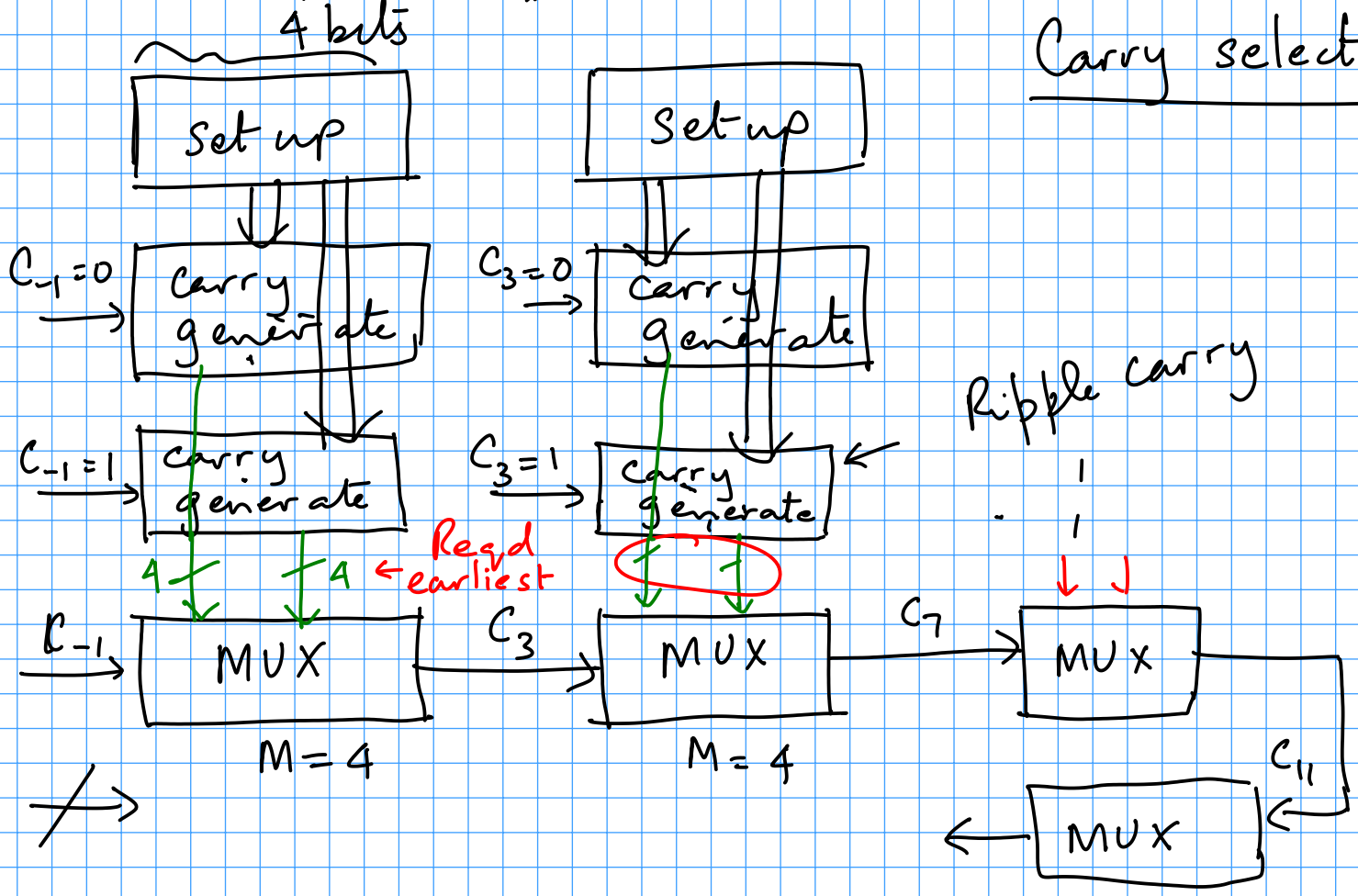
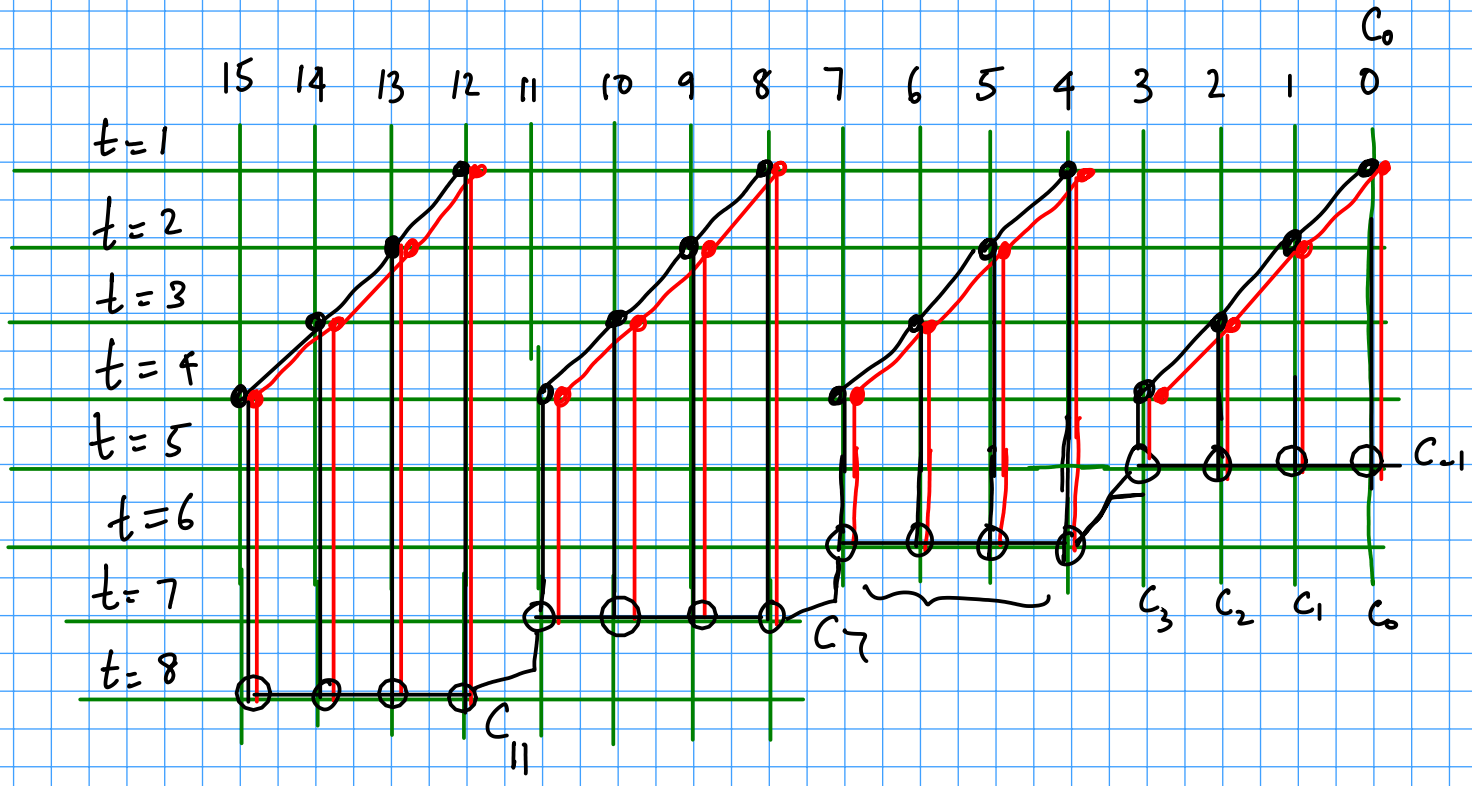
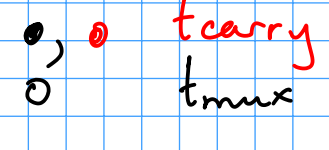
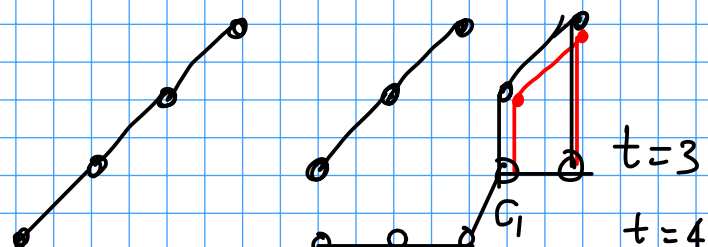
Carry select

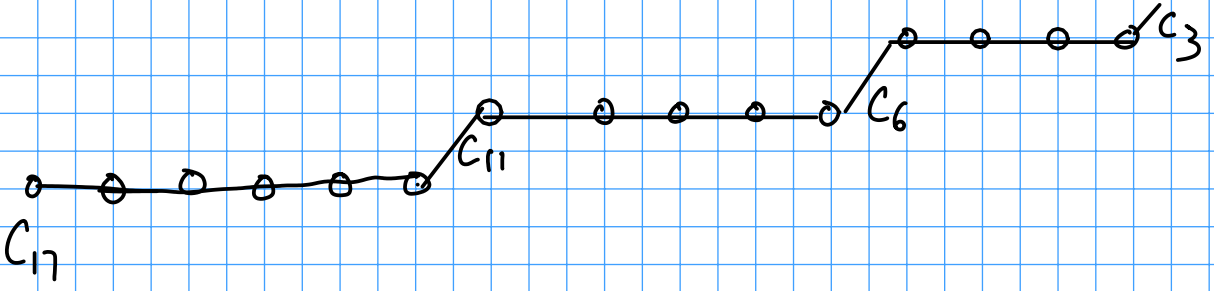




$t_{carry} = t_{mux}$







For large adders, instead of $\left(\frac{N}{M}\right) t_{mux}$, we will get $\sqrt{2N}\, t_{mux}$

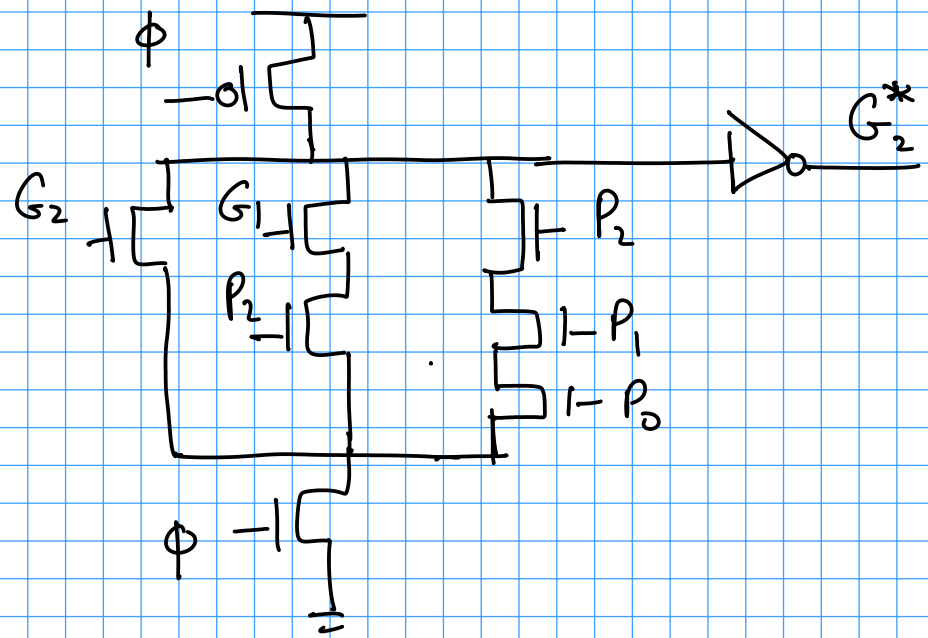
Carry lookahead:

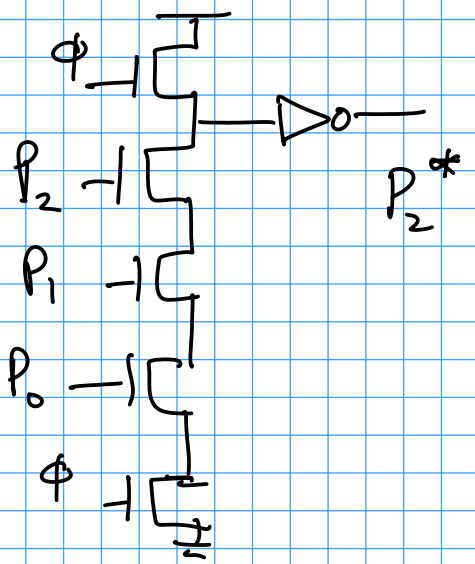
$$C_0 = G_0 + P_1 C_{-1}$$

$$C_1 = G_1 + P_1 C_0 = (G_1 + P_1 G_0) + (P_1 P_0) C_{-1}$$

$$C_2 = \underbrace{(G_2 + P_2 G_1 + P_2 P_1 G_0)}_{G_2^*} + \underbrace{(P_2 P_1 P_0)}_{P_2^*} C_{-1}$$

$$C_3 = (G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0) + (P_3 P_2 P_1 P_0) C_{-1}$$





Can do this for any number of bits, but gates will become bulky and sluggish. large self capacitance.

Instead of one large bulky gate, cascade smaller gates.

Define "dot" operator as follows.

"dot" Operator

$$\bullet \longrightarrow (G_2, P_2) \bullet (G_1, P_1) = (G_2 + P_2 G_1, P_2 P_1)$$

$$\begin{aligned} C_1 &= g_1 + P_1 g_0 + P_1 P_0 C_{-1} \\ &= (g_1, P_1) \bullet (g_0, P_0) \bullet (C_{-1}, 0) \\ &= (g_1 + P_1 g_0, P_1 P_0) \bullet (C_{-1}, 0) \\ &= (g_1 + P_1 g_0 + P_1 P_0 C_{-1}) \end{aligned}$$

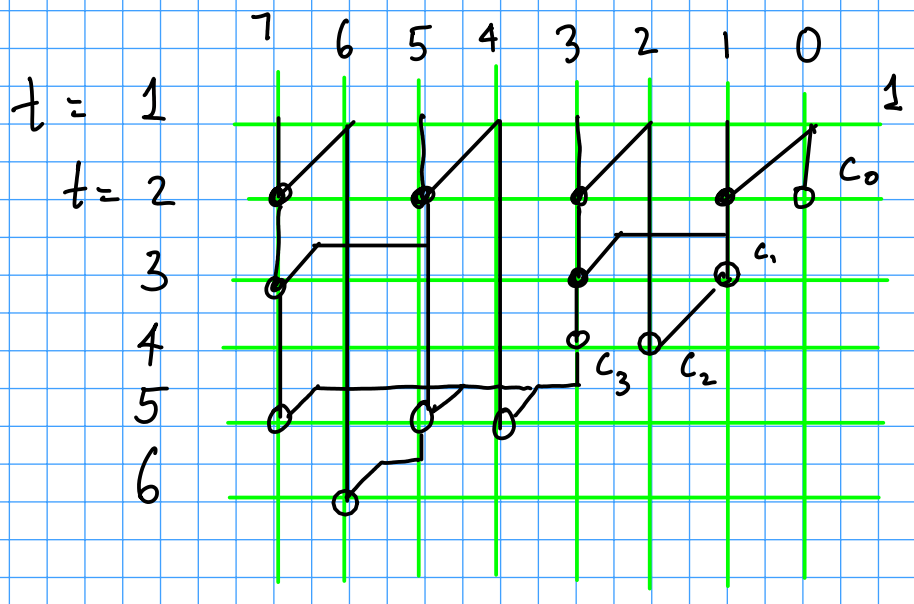
Operator "dot" $\bullet$

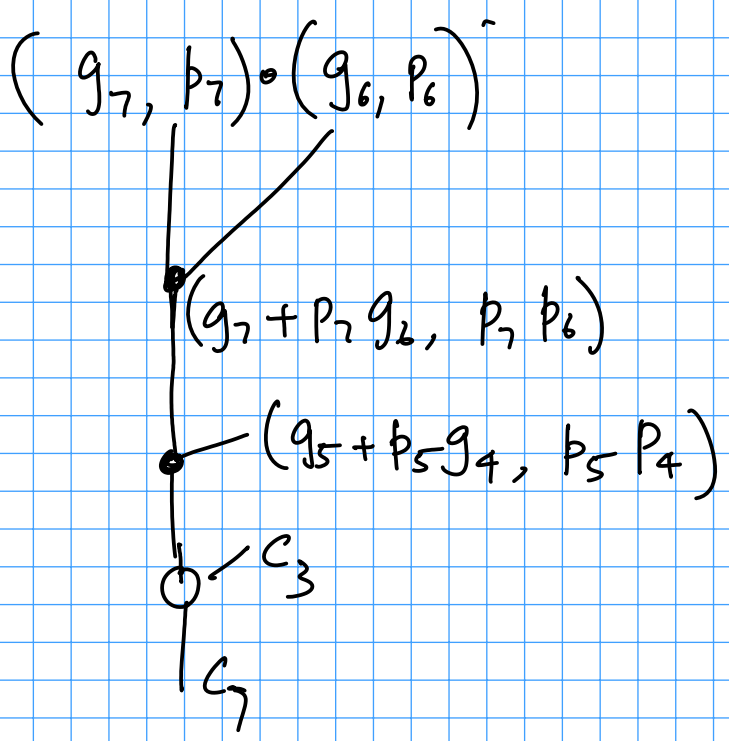
$$(G_2, P_2) \bullet (G_1, P_1) = (G_2 + P_2 G_1,\ P_2 P_1)$$

0; $(G, P) \bullet (C, 0)$

$$(g_3 + p_3 g_2,\ p_3 p_2) \bullet (g_1 + p_1 g_0,\ p_1 p_0)$$

$$= (g_3 + p_3 g_2 + p_3 p_2 g_1 + p_3 p_2 p_1 g_0,\ p_3 p_2 p_1 p_0)$$




$(g_7, p_7) \circ (g_6, p_6)$
$(g_7 + p_7 g_6,\ p_7 p_6)$
$(g_5 + p_5 g_4,\ p_5 p_4)$
c_3
c_7