VLSI DATA CONVERSION CIRCUITS : PROBLEM SET 4
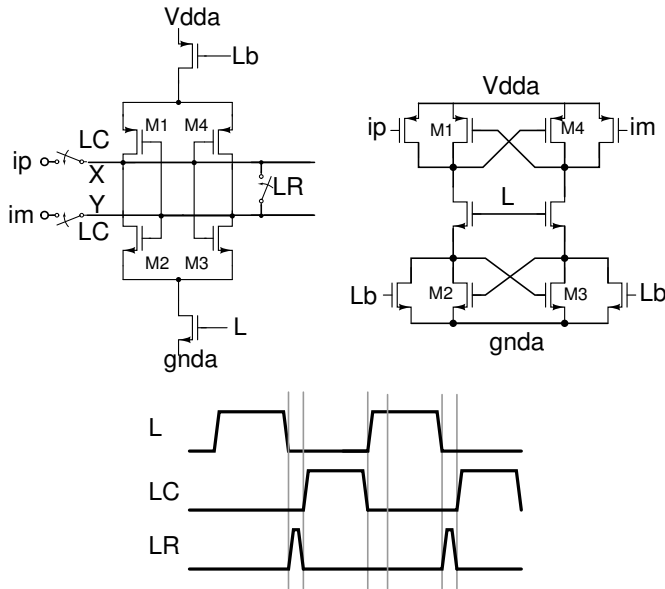
Problem 1

Figure 1: Latch circuits for Problem 1.

In this problem, we attempt to understand the issue of dynamic offset. Consider the two latch circuits in Fig. 1. The first latch was discussed in class. Another candidate latch (with the advantage of greatly simplified clocking) is shown towards the right of the figure. In both latches, L is the latch signal, while Lb is its complement. For simplicity, use an ideal clock generator. Vdd = 1.8 V. The input is fully differential, with a common-mode voltage of 0.9 V. The clock frequency is 10 MHz.

1. Use minimum sizes for all transistors. Choose appropriate implementations for the switches. Determine dynamic offset using the following procedure - the differential input is to be made a slow ramp, increasing at 2 mV every clock period, starting from $-Vdd/5$ and going all the way to $Vdd/5$. We hope that the offset will lie within this range. The "threshold" of the latch (ideally to be zero) can be found to within 2 mV by observing when the regenerated output flips sign. Take care of the following during simulation - choose the time step of the simulation to be sufficiently small so that the waveforms during regeneration do not change appreciably. Which of the latches has more dynamic offset ? Why ? In your report, draw the circuit diagrams with all device sizes marked. Also on one graph, plot the waveforms of all latch nodes in that clock period where the latch flips sign.

2. Deliberately add a capacitance of 0.5 fF at the drain of M1 only, and repeat part (a). What do you notice? Why?
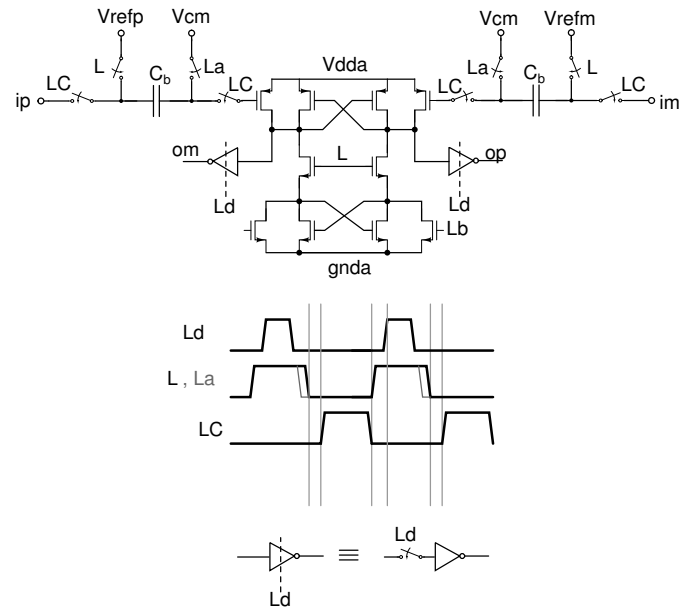
Problem 2

Figure 2: Latch circuit for Problem 2.

This problem discusses another way of subtracting differential references from the differential input. This is done by the use of coupling capacitors Cb as shown in Fig. 2.

1. Explain clearly how this circuit works.

2. What is the capacitance looking in from the input when LC is high?

3. How will you choose Cb ?

4. Using this as the basic building block, design a 4 bit flash ADC. Vdd = 1.8 V. The full scale input is to be 3 V (peak-to-peak differential), with a common-mode voltage of 0.9 V. Assume you have ideal voltage sources of 1.65 V and 0.15 V from which to operate the ladder. How will you choose the value of the ladder resistors ? Design the digital back-end (transition detect and the 1-of-N to binary converter).

5. Show the spectrum of the ADC output for a full-scale sinewave at about fs/2. What is the SQNR (in dB) ? One way of doing this is to print the four ADC output bits into a file, read the file into MATLAB, convert from binary to decimal, and do the FFT in MATLAB. Another way of doing this is to use an ideal 4-bit DAC at the output of the ADC and run an FFT on the DAC output in Eldo.