VLSI DATA CONVERSION CIRCUITS : PROBLEM SET 2

Problem 1

A signal $x(t)$ is known to be of the form $A_1 \sin(2\pi f_{in} t + \phi_1) + A_2 \sin(2\pi 2 f_{in} t + \phi_2) + A_3 \sin(2\pi 3 f_{in} t + \phi_3)$. $x(t)$ is sampled at a rate $f_s > 6 f_{in}$. 1024 samples are taken and multiplied with a **Blackman-Harris Window**. The magnitude of the FFT of the resulting 1024 point sequence is given in the attached file $y.mat$. In other words, denoting the window by $w[n]$ and the sampled input sequence by $x[n]$, $y[n]$ is obtained using the following MATLAB command `y=abs(fft(x.*w'))`. How will you determine A_1, A_2 and A_3 from y ?

Problem 2

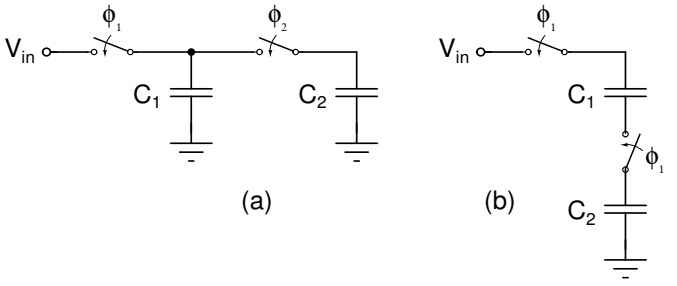

Figure 1: Circuits for Problem 2.

In class, we derived a parasitic insensitive switched capacitor amplifier developing the basic idea shown in Fig. 1(a). Here, C_1 is charged to V_{in} in ϕ_1, and we attempt to transfer this charge ($C_1 V_{in}$) onto C_2 in ϕ_2. This problem investigates another line of thought, which aims to accomplish the same objective. The basic idea is shown in Fig. 1(b). The argument is as follows - if C_1 and C_2 were initially uncharged, when they are simply connected in series with V_{in} as illustrated in the figure, the charge on the top plate of C_2 will be equal in magnitude to that on the bottom plate of C_1. The trick is, therefore, to figure out how C_2 should be chosen so that the charge in C_1 can be made to be $C_1 V_{in}$. Once you know this, proceed along the same lines as we did in class to derive another parasitic insensitive amplifier and accumulator.

Problem 3

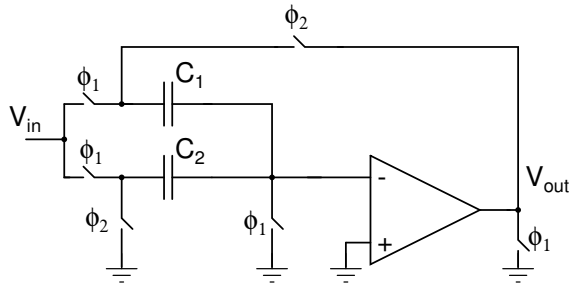

Figure 2: Circuit for Problem 3.

- Determine the gain of the switch-capacitor amplifier shown in Fig. 2. What should C_2 be (in terms of C_1) to achieve a gain of 2 ? Assuming an opamp transfer function of GB/s, plot GB required to achieve 0.1% output settling in a time $T_s/2$.
- The opamp has a finite gain A. $C_1 = C_2$. Determine the amplifier gain now.
- Draw and simulate a fully differential version of the circuit of Fig. 2. For simulation, use the macromodel for the fully differential opamp, as shown below. Assume that the opamp is sampling at a rate of 25 MHz. Use real switches, and a real non-overlapping clock generator. Determine $Cdom$ in the macromodel so that the output of the amplifier settles to better than 0.1% of the final value in half a clock cycle. Use $V_{cm} = 0.9$ V, $Vmax = 1.6$ V and $Vmin = 0.2$ V. The input to be amplified is a 1 MHz fully differential sine-wave with an amplitude of 1 V (p-p differential), with a common-mode voltage of 0.9 V. Plot the input and output waveforms, as well as the waveforms at the inputs of the opamp.

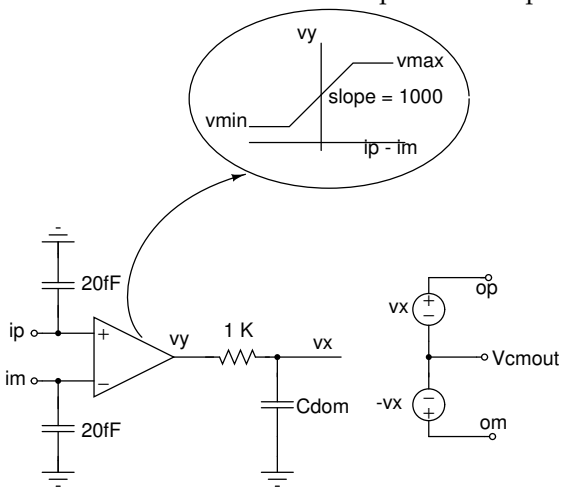

Figure 3: Opamp macromodel for Problem 3.