VLSI DATA CONVERSION CIRCUITS : PROBLEM SET 1

Problem 1

This problem is intended to illustrate the effect of oversampling on the required performance of an antialias filter placed before a sampler. For simplicity, assume that the anti-alias filter is an Nth order Butterworth filter, with

$$|H(f)| = \frac{1}{\sqrt{1+\left(\frac{f}{f_{3dB}}\right)^{2N}}} \tag{1}$$

where f_{3dB} denotes the 3 dB bandwidth of the filter. The signal bandwidth is 1 MHz. It is desired that the attenuation of the anti-alias filter in the first "alias" band should be atleast 60 dB. The attenuation of signal at 1 MHz should be lesser than 0.5 dB. Consider the following cases

- The sampling rate is 4 MHz. What is the minimum order required of the anti-alias filter ? What is the bandwidth ? For the minimum order, how much can the filter bandwidth vary, while still meeting the requirements on attenuation ?

- The sampling rate is 40 MHz. What is the minimum order required of the anti-alias filter ? What is the bandwidth ? For the minimum order, how much can the filter bandwidth vary, while still meeting the requirements on attenuation ?

Problem 2

This problem is intended to understand the effects of random offset, gain mismatch and timing skew on the performance of a 2-way time-interleaved sampler. Assume that the sampling frequency of the complete sampler is f_s. The input is a 1 V sinusoid with a frequency $f_{in} = \frac{97}{1024} f_s$. To make sure you are doing the FFT right, determine the spectrum of an ideal sampler output. Draw the spectrum in all the following cases.

- The two samplers in the interleaved system have offsets of 2 mV and -5 mV respectively. How much lower in power is the tone at $f_s/2$ when compared to the input ? Do a hand calculation and confirm. Express your answer in dB.

- The two samplers in the interleaved system have gains of 0.99 and 1.01 respectively. What tones do you see in the spectrum now ? Do a hand calculation and confirm the strength of the tones. Express your answer in dB.

- Ideally, the individual samplers making up the ping-pong system sample at $2kT_s$ and $(2k+1)T_s$ respectively. In practice, there is timing skew - namely, the samplers sample at $2kT_s - t_o/2$ and $(2k+1)T_s + t_o/2$, where t_o is the "timing skew". Using the approach used in class, determine the effect of timing skew on the output spectrum for a sinewave input. Simulate for a timing offset of $T_s/100$.

Problem 3

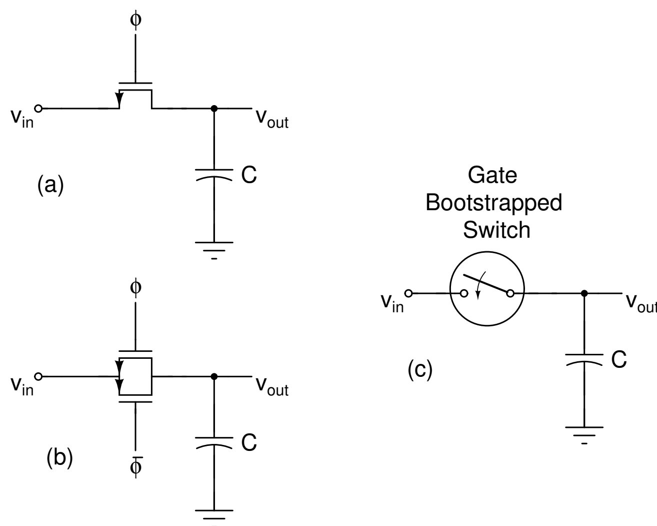

Figure 1: Circuits for Problem 3.

This problem is intended to compare the performance of three different sample-and-hold circuits. Assume that each circuit is one half of a fully differential arrangement. In order to enable a fair comparison of the three topologies, we design them for the same specifications, which are the following :

a. Sampling frequency of 100 Msps.

b. Tracking bandwidth of 200 MHz.

c. Peak-to-peak differential input signal swing of 1 V_{pp}.

d. Input common-mode voltage of $0.8\,\mathrm{V}$.

e. Peak Signal to Thermal Noise Ratio of 70 dB.

For all the three circuits, use the $0.18\,\mu\mathrm{m}$ TSMC process parameters, and

a. Decide the size of the sampling capacitor.

b. Choose the device sizes. For the arrangement of Figure 1(c), you may use an “ideal” clock generator - that is one generated using pulse sources.

c. Simulate the distortion when the input frequency is approximately $\frac{f_s}{2}$. Use a 64 point FFT record. Compare the distortion generated by each circuit.

c. Simulate the distortion when the input is at approximately $\frac{f_s}{9}$. Compare the distortion generated by each circuit. How do the distortion numbers compare with the ones you got when the input frequency is close to $\frac{f_s}{2}$?