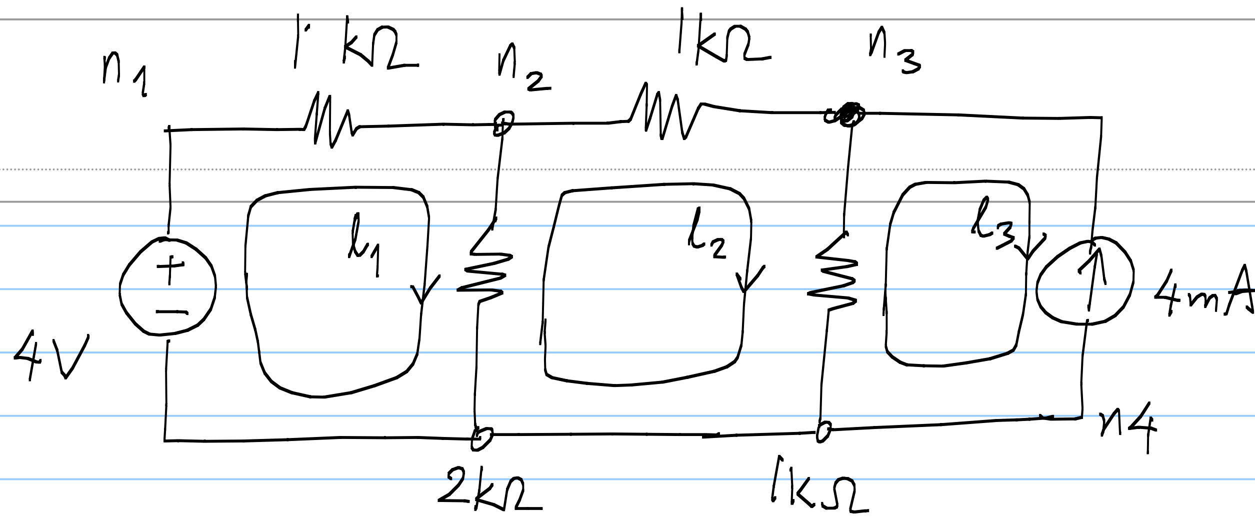
P1

Note Title

6/16/2008

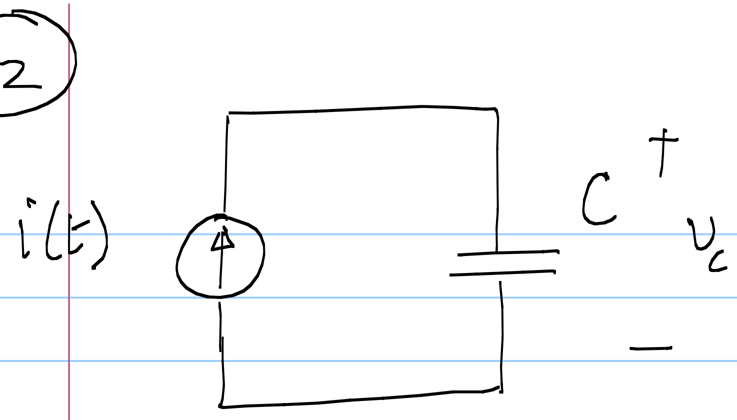


(a) Set up node equations with n4 as reference

(b) Set up mesh equations with loops l_1, l_2, l_3

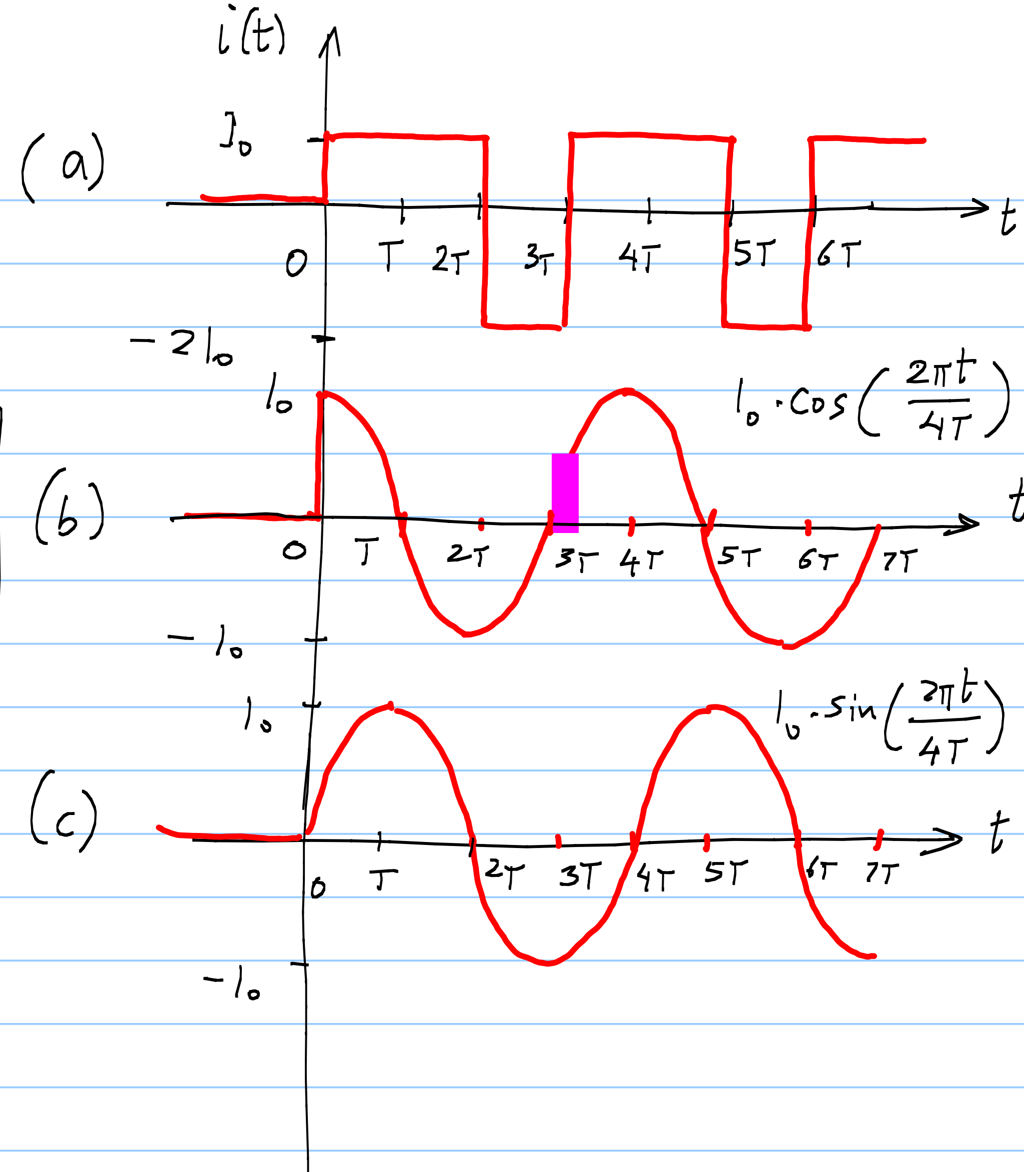
(c) Find the voltage across all 1kΩ resistors using superposition.

P2



Find $v_c(t)$ when $i(t)$ is as shown in (a), (b) or (c)

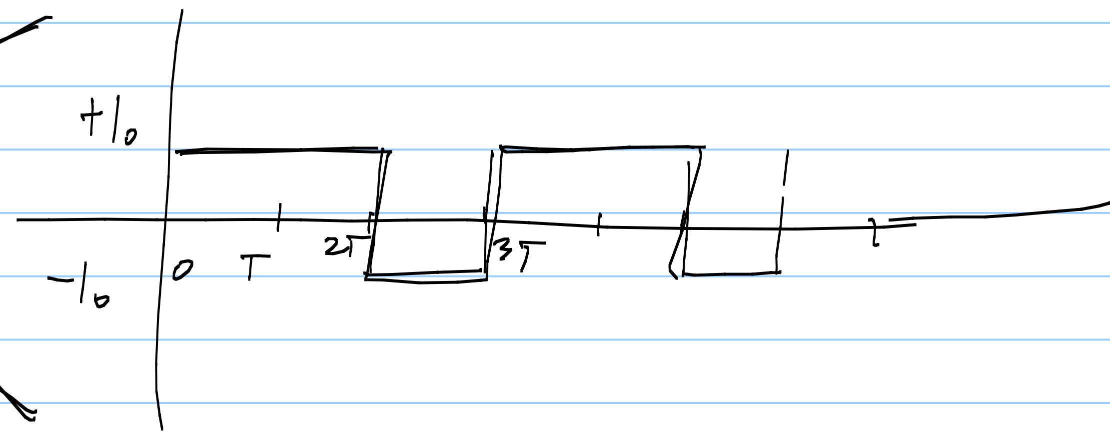
In all cases, initial voltage across the capacitor is zero



P1: * Complete the superposition solution.

* Solve Mesh & Node equations by inverting the matrix & verify

P2:



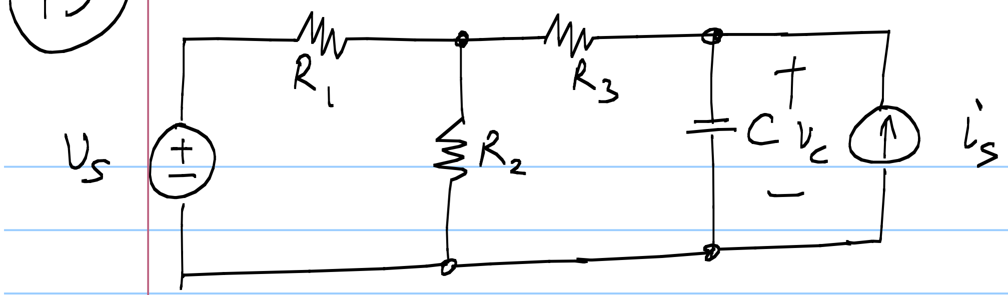
P2: Calculate numerical solutions for

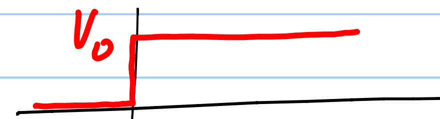
$C = 1nF$

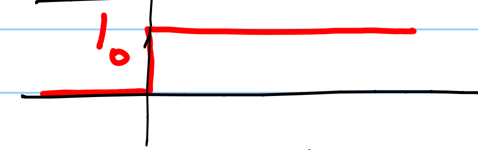
$I_0 = 1\mu A$

$T = 1ms$

P3

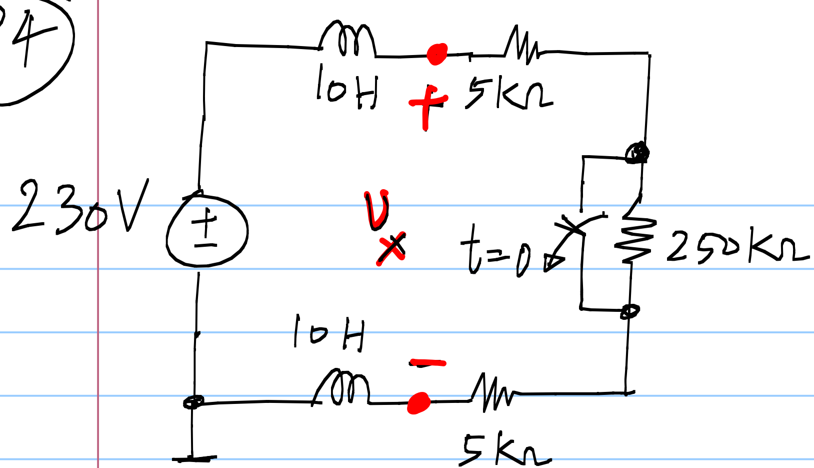


* Setup the differential equation governing the circuit above
* Solve $v_c(t)$ for $i_s = 0$, $v_s =$ 

* Solve $v_c(t)$ for $v_s = 0$, $i_s =$ 

* Find $V_c(s)/V_s(s)$, $I_s = 0$; Determine poles & zeros; sketch $\left|\frac{V_c(j\omega)}{V_s(j\omega)}\right|$ & $\angle\frac{V_c}{V_s}$
* Find $V_c(s)/I_s(s)$, $V_s = 0$; Determine poles & zeros; sketch $\left|\frac{V_c(j\omega)}{I_s(j\omega)}\right|$ & $\angle\frac{V_c}{I_s}$

P4



The switch is opened at $t=0$. Setup the differential equation governing the circuit and solve for $v_x(t)$

SIMULATE

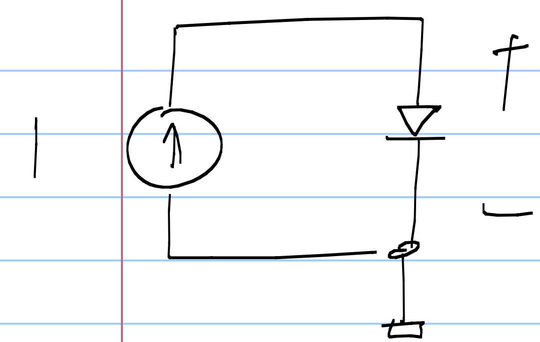
P3

Simulation: $R_1 = 3k\Omega$, $R_2 = 6k\Omega$, $R_3 = 2k\Omega$, $C = 10nF$

$V_0 = 3V$, $I_0 = 1mA$

* Simulate the response to steps in v_s & i_s
* Simulate frequency responses from V_s & I_s
* Compare with calculated values.
* Can you arrange simultaneous steps in V_s & I_s so that V_c doesn't change at all? Simulate

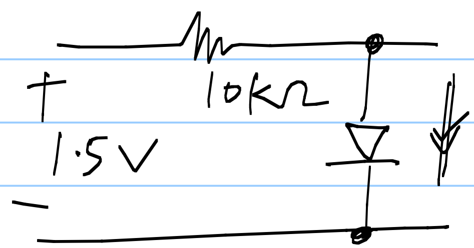
P5 (a) Simulate I-V characteristics of a diode



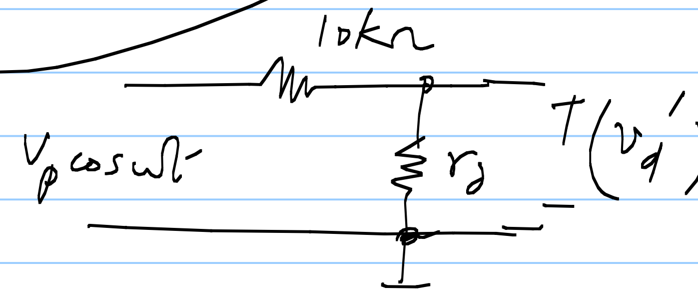
Plot I vs. V

Small signal model

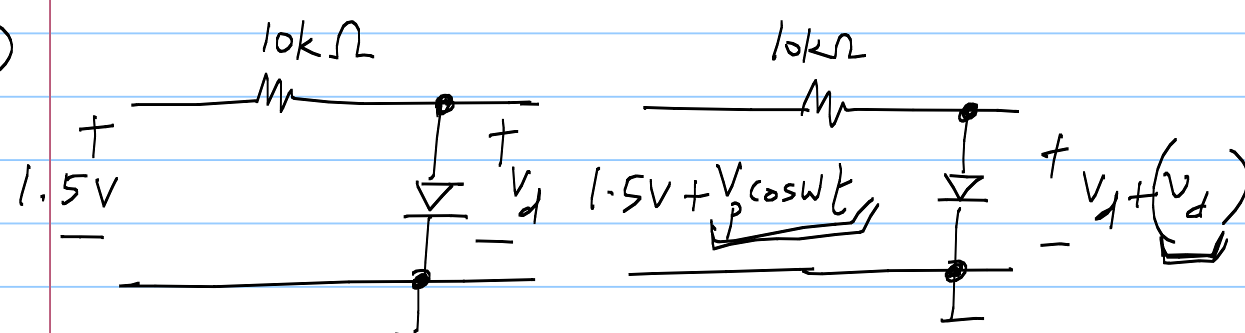
(b)



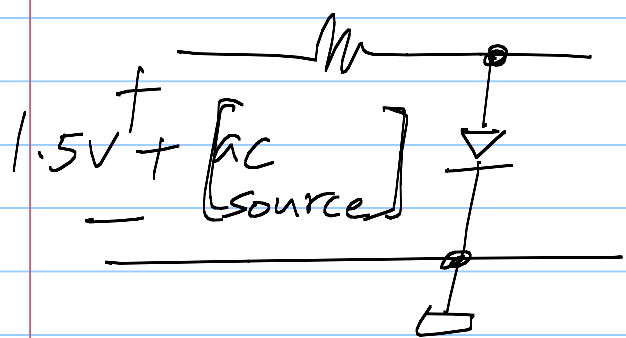
Determine I_d.



(c)



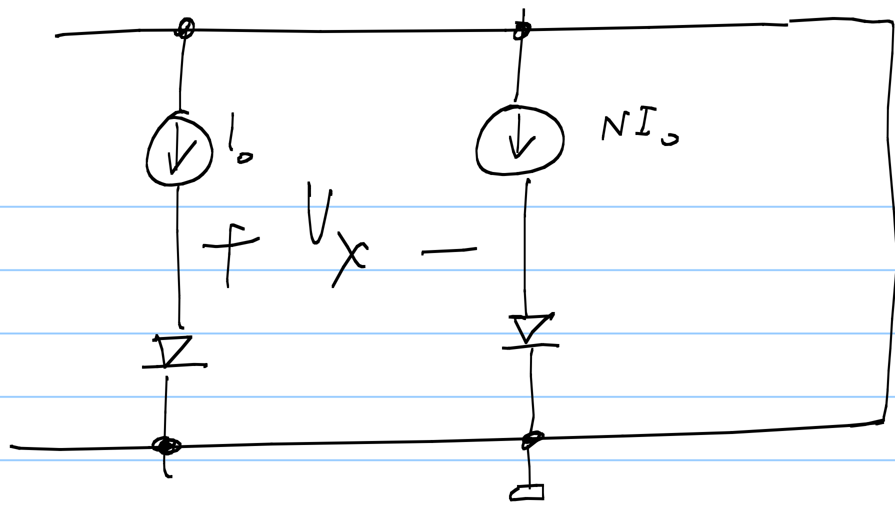
DC, Transient. (AC)



AC analysis:

* Calculate the operating point
* Replace all components by small signal equivalent
* Run sinusoidal steady state analysis

P6



Calculate the voltage V_x with the ideal diode model (exponential)

Compare

Simulate → sweep the temperature & plot V_x vs. temp.

(P7) You are required to realize a negative feedback amplifier of gain = 10, gain accuracy = 0.05%, 99% settling time = 1 μs.

* Determine the unity gain frequency and the dc gain of the opamp.
* Realize the opamp for the above application using VCCS, C, VCVS. Choose C in the range (1pF, 10pF)
* Realize the amplifier. The current driven from the opamp output must be 100 μA for a 100 mV dc input
* what is the 3dB bandwidth of this amplifier (in Hz)

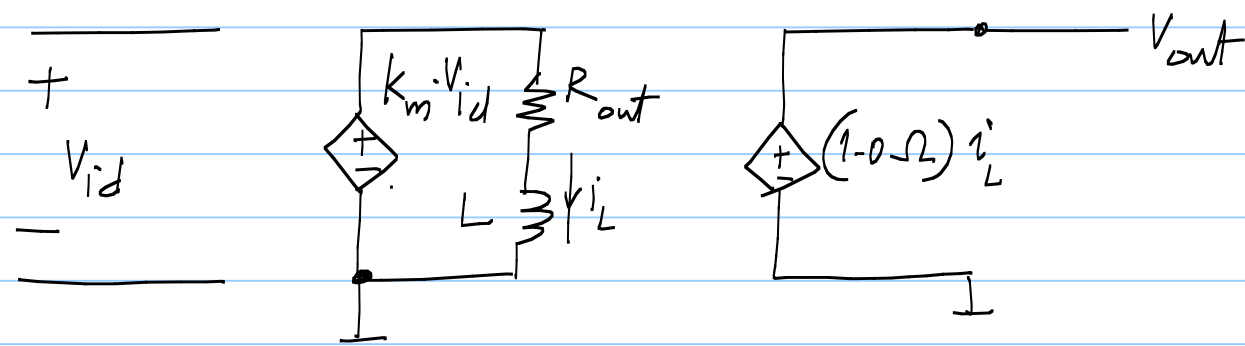
(P8) In the amplifier designed yesterday, assume that the opamp swing is limited to $\pm 5V$ & that its slew rate is $5\ MV/s$. For (a) & (b) assume a small ω so that slew rate limitation doesn't occur.

(a) Sketch the output for $v_i = 1V + 2V\cos(\omega t)$

(b) If $V_i = V_p \cos\omega t$, what is the highest value of V_p without producing a distorted output?

(c) What is the highest frequency at which a full amplitude (5V) sinusoidal output can be produced without distortion

(P9) For the opamp designed earlier, come up with a model using an inductor instead of a capacitor for integration.



* Come up with the values of K_m, R_{out} for a given ω_u & A_o and an assumed value of L.
* Verify the model in the simulator.

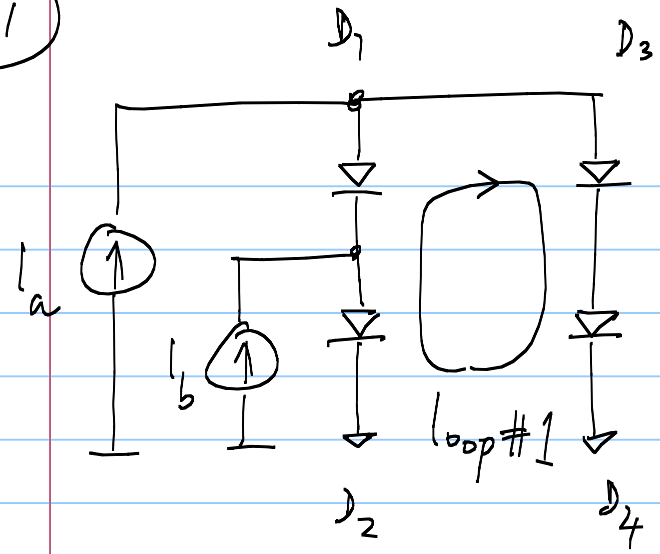
(P10) Assuming that a MOS transistor is biased in the saturation region, sketch $\sqrt{I_D}$ versus V_{GS}.

* What type of plot is it?
* How can you determine K & V_T from the plot? $\left(I_D = K \cdot \frac{W}{2L} \cdot (V_{GS} - V_T)^2 \right)$
* Simulate I_D vs. V_{GS} of a $\frac{10\mu m}{2.5\mu m}$ transistor

  Vary V_{GS} from 0 to 1.5V keeping V_{DS} @ 1.2V

  Extract the values of K & V_T from the plot
* Simulate the o/p characteristics for $V_{GS} = 0, 0.5, 1.0, 1.5V$

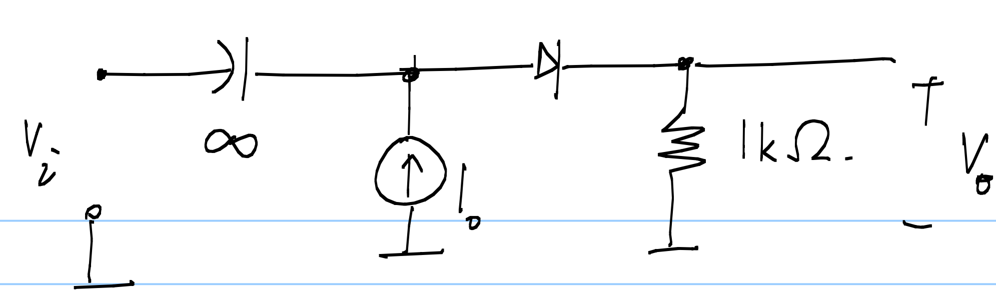
P11



Assuming a diode characteristic of $I_D = I_s \cdot \exp(V_d/V_t)$, calculate the current in the four diodes.

Hint: write KVL for loop #1 & express diode voltages in terms of their currents

P12



* Evaluate the small signal transfer $\frac{V_o}{V_i}$ for

(a) $I_o = 1mA$, (b) $I_o = 0.1\mu A$

(Assume that the capacitor is a short at the frequencies of interest.)

* What is a possible application of this?

* Simulate with $V_i = 50mV \cos(2\pi \cdot 1kHz \cdot t)$ & a step in I_o

P13: Assign opamp signs for dc negative feedback around them. Explain the reasoning clearly.