Twenty third National Conference on Communications

Millimeter-wave Circuit and System Design in CMOS: Basics and Recent Advances

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Twenty third National Conference on Communications

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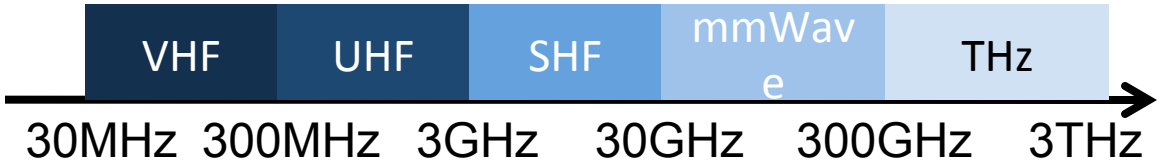
Outline

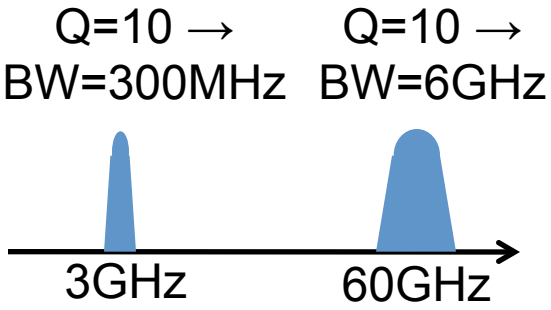
- **Brief History of mmWave in CMOS**
- Active and Passive Device Modeling
- Low-Noise Amplifier Design
- Oscillators and VCOs
- Power Amplifiers
- Multiple-Antenna Systems

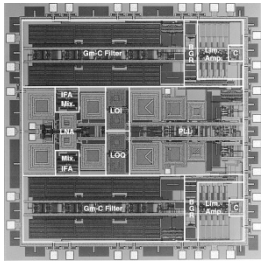
mmWave: What, Why?



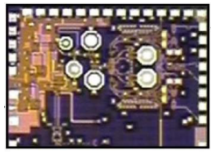
The mmWave frequency range is defined as the range of frequencies where the free-space wavelength ranges from 10mm to 1mm. Therefore, it ranges from $3x10^8$ m/s ÷ 0.01m = **30GHz** to $3x10^8$ m/s ÷ 0.001m=**300GHz**.

Why operate in this range?





11.2mm² 0.5μm CMOS GPS receiver (1997)



3.8mm² 90nm CMOS 60GHz receiver (2008)

MORE BANDWIDTH!

THINGS GET SMALLER!

Initial Applications of mmWave

Homeland Security

- Detection of concealed weapons.
- Airport security.
- Airborne chemical sensing.

Medical Imaging

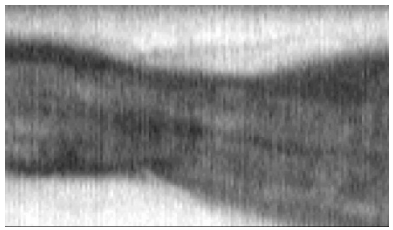


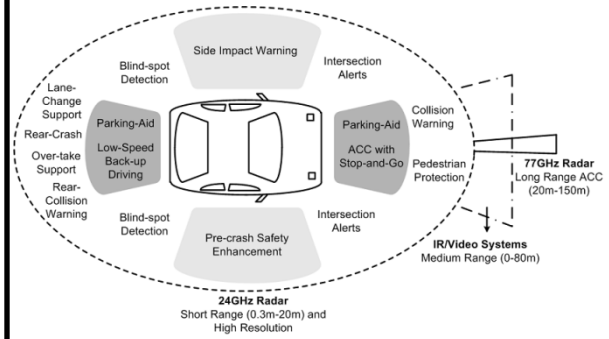
Image of the back of the knee through denim jeans.

- Sub-surface temperature mapping.
- Non-invasive medical diagnostics for arthritis, skin cancer, rheumatism.

Defense Applications

- Electronic warfare.
- High-resolution radar.
- Wide-bandwidth communication.

Intelligent Transportation



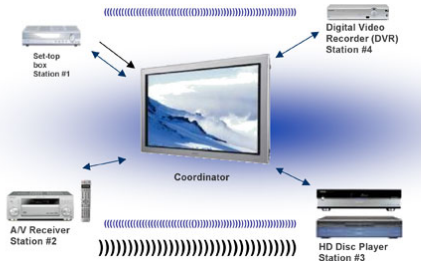
Vehicular mmWave radars for collision avoidance, blind-spot detection, automatic cruise-control.

Aeronautics

mmWave passive image of aircraft runway

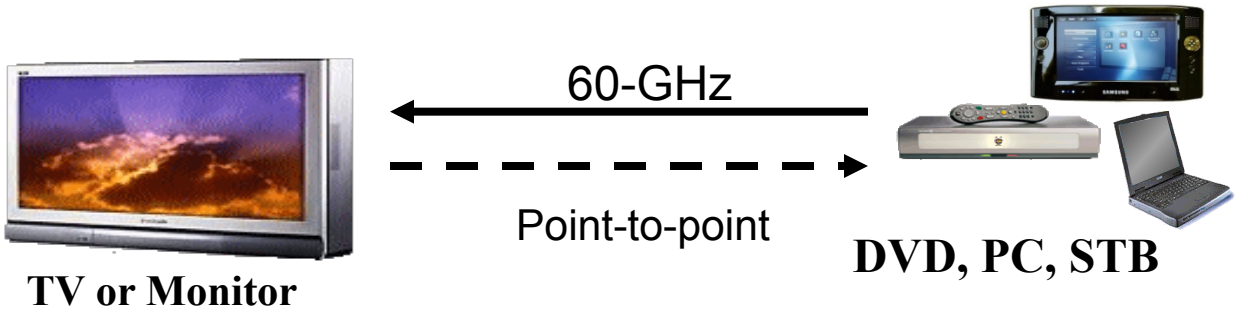
mmWave passive imagers for all-weather landing systems.

Consumer Wireless

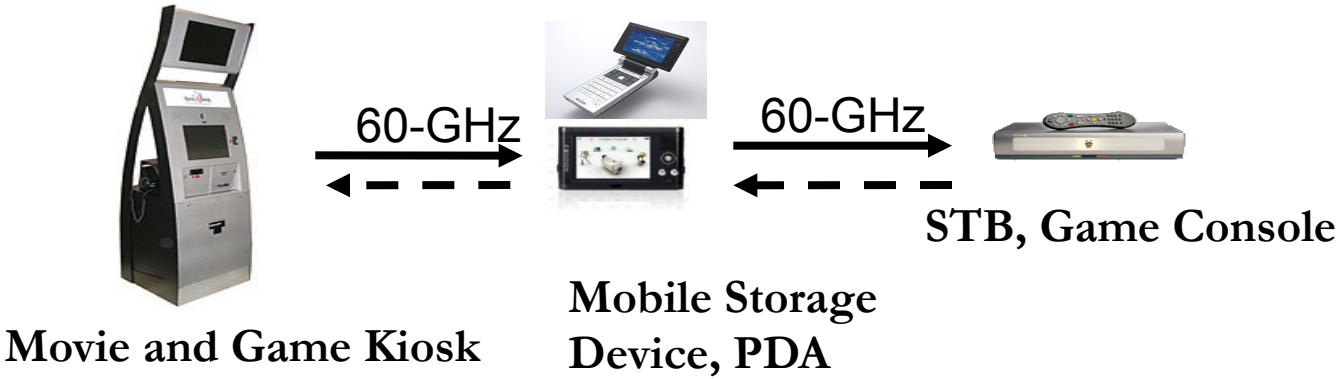


- 60GHz high-data-rate networks for home multimedia (Wireless HDTV).
- Wireless "last-mile" transmission.

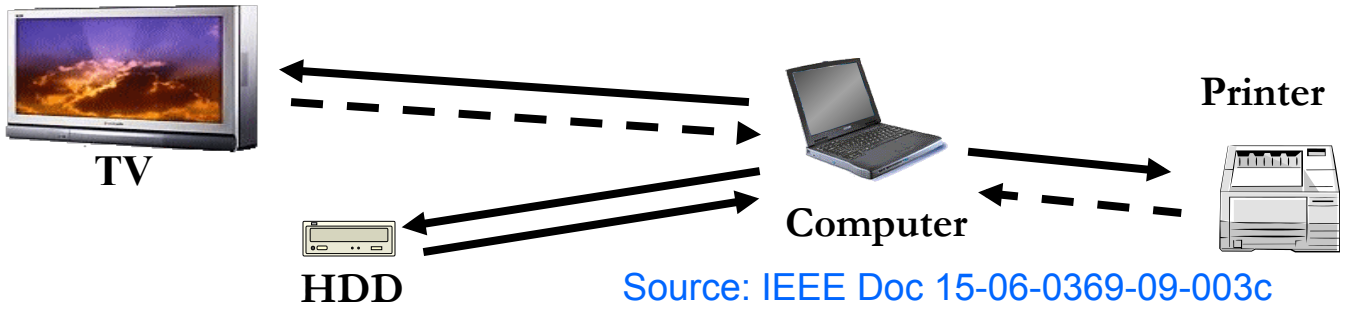
Example: 60GHz Usage Scenarios



Usage Model 1
Streaming HD Video
(Uncompressed)
1080i > 1.5 Gb/s
1080p > 3 Gb/s



Usage Model 2
"Point-and-shoot" file transfer
1-3 Gb/s burst data
1-3 m range

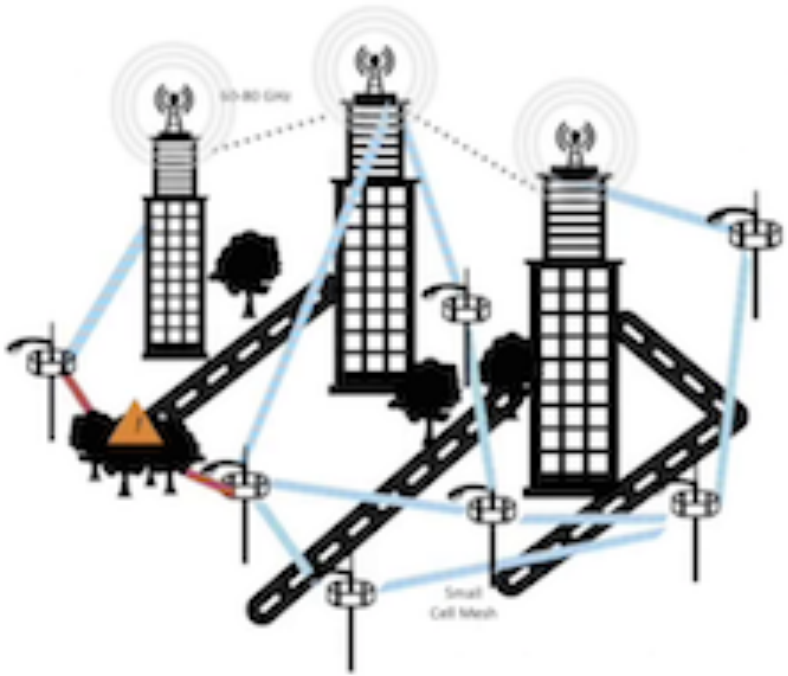


Source: IEEE Doc 15-06-0369-09-003c

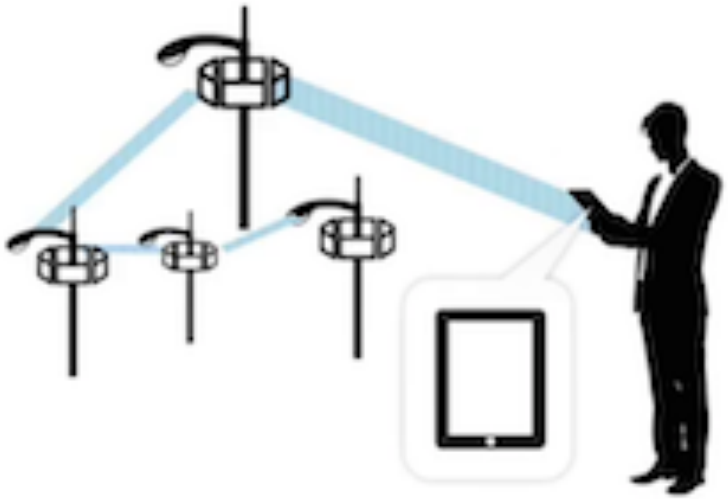
Usage Model 3
Personal Area Network
Streaming video + file transfer

The 5G Hype

Millimeter Wave Use Cases for 5G Cellular



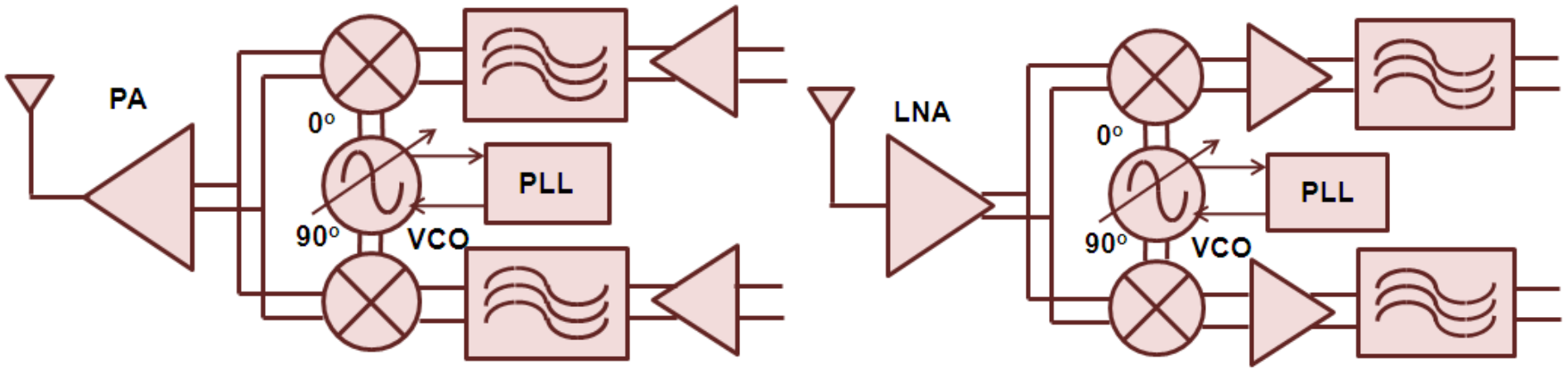
Backhaul



Access

Image courtesy Interdigital

mmWave Design Challenges



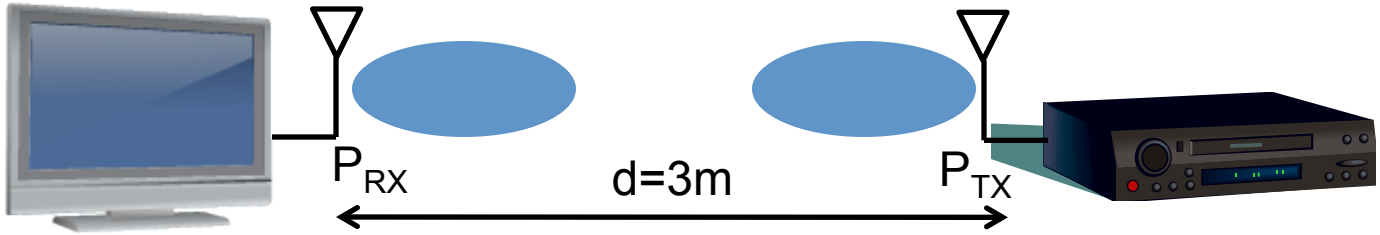
- High-power, high-efficiency, high-linearity mmWave PAs.
  - P_{out}~30dBm at efficiency>20%
- Wide-tuning-range mmWave VCOs.
  - >25% tuning range at 100GHz and above.
- Low-cost mmWave electromagnetic interfaces/packages
  - Antenna arrays in package or on silicon?
- mmWave low-noise amplifiers.
- Low-power mmWave phased-array SoCs.

Hard(ish)

Moderate

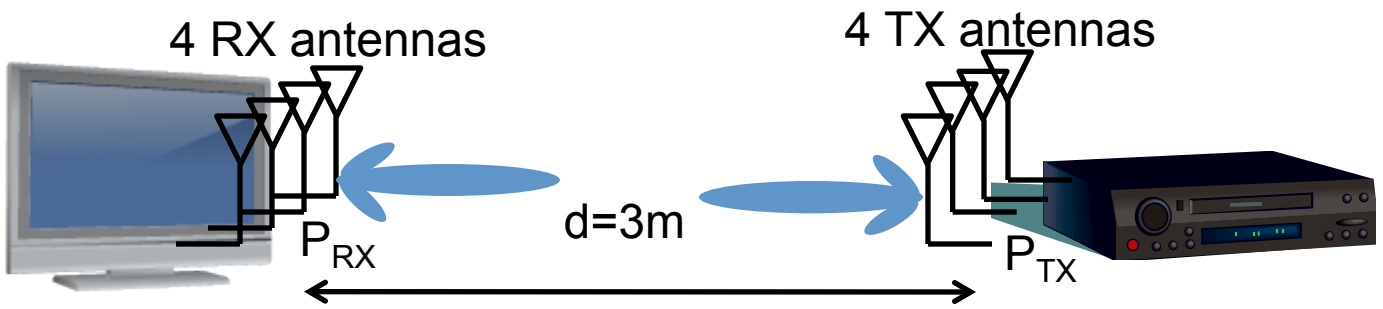
Relatively solved

mmWave Link-Budget Challenges



Component	Contribution
Transmitter Power (P_{TX})	10dBm (10mW) → TECHNOLOGY RELATED CHALLENGE
Transmitter Antenna Gain	2dBi (for a typical omnidirectional antenna)
Path loss @1m, 60GHz	-78dBm → mmWAVE-RELATED CHALLENGE
Shadowing loss	10dB (due to multipath fading etc.)
Receiver Antenna Gain	2dBi (for a typical omnidirectional antenna)
Received Power (P_{RX})	-74dBm
Noise Level (kTx50Ω)	-174dBm
Noise Bandwidth (BW)	1GHz (for 1Gbps data transmission) → mmWAVE-RELATED CHALLENGE
Receiver Noise Figure (NF)	10dB (based on current silicon technology) → TECHNOLOGY RELATED CHALLENGE
Total Noise Power (kTx50ΩxBWxNF)	-74dBm
Signal-to-Noise Ratio (SNR)	0dB
Typical SNR required for demodulation	10dB → NOT ENOUGH SNR!

Multiple Antennas to the Rescue



Component	Contribution
Total transmitter Power (P_{RX})	16dBm (coherent addition of the powers of 4 transmitting antennas)
Transmitter Antenna Gain	8dBi (transmitted beam becomes 4 times more directional)
Path loss @1m, 60GHz	-78dBm
Shadowing loss	-10dB (due to multipath fading etc.)
Receiver Antenna Gain	2dBi (for a typical omnidirectional antenna)
Received Power at each antenna (P_{TX})	-62dBm
Noise Level (kTx50Ω)	-174dBm
Noise Bandwidth (BW)	1GHz (for 1Gbps data transmission)
Receiver Noise Figure (NF)	10dB (based on current silicon technology)
Total Noise Power (kTx50ΩxBWxNF)	-74dBm
Signal-to-Noise Ratio (SNR)	-62dB + 12dB (coherent addition of 4 RX antennas) – (-74dB + 6dB (coherent addition of noise)) = 18dB
Typical SNR required for demodulation	10dB → 8dB margin!

Outline

- Brief History of RF/mmWave in CMOS
- **Active and Passive Device Modeling**
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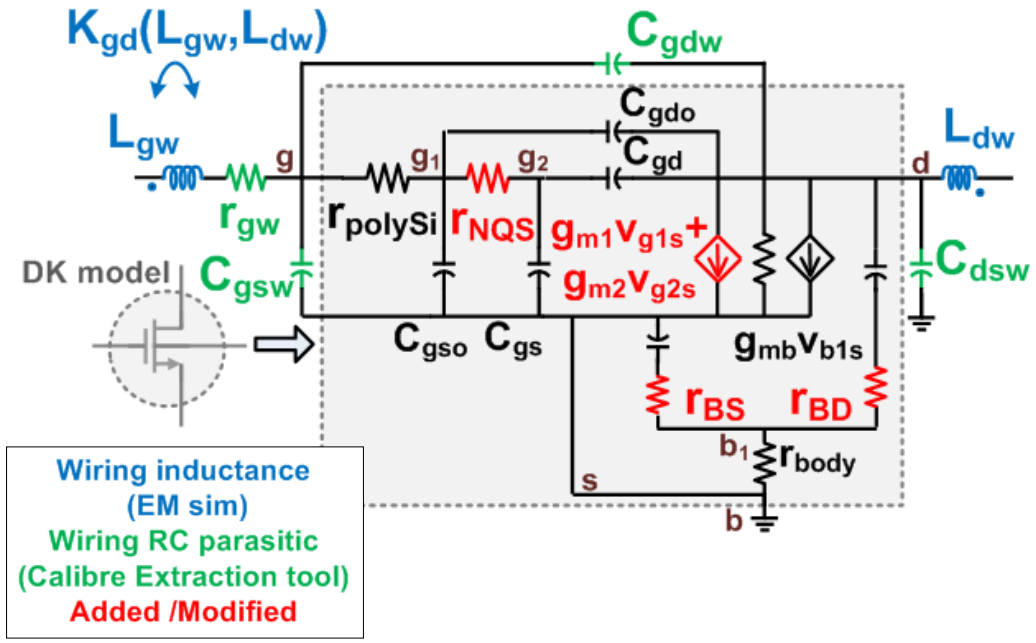
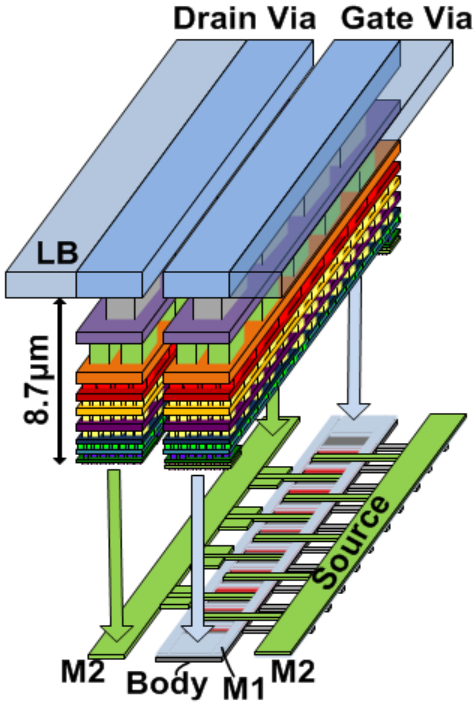
- Multiple-Antenna Systems

IBM 45nm SOI CMOS Modeling

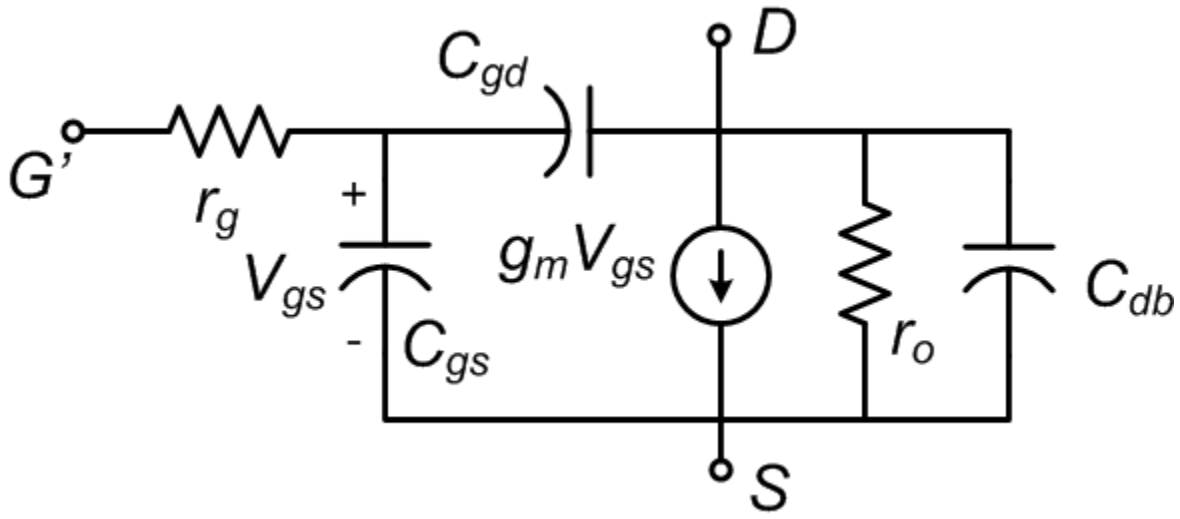




Custom *gate-over-device* layout

- Modern BSIM FET models include many high-frequency effects.
  - NQS resistance, substrate parasitics.
- Layout-related parasitics are also very important for mmWave.
  - Wiring resistances and capacitances (Calibre PEX).
  - Via inductance and coupling (IE3D EM field solver).

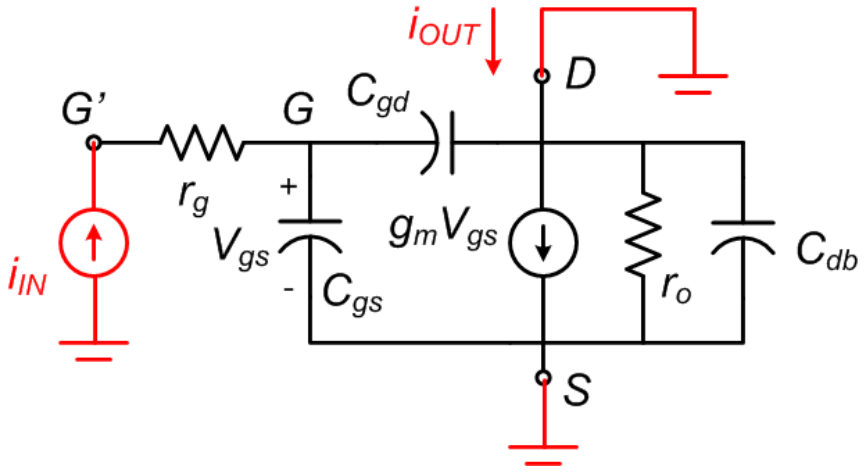
Simplified High-Frequency Model

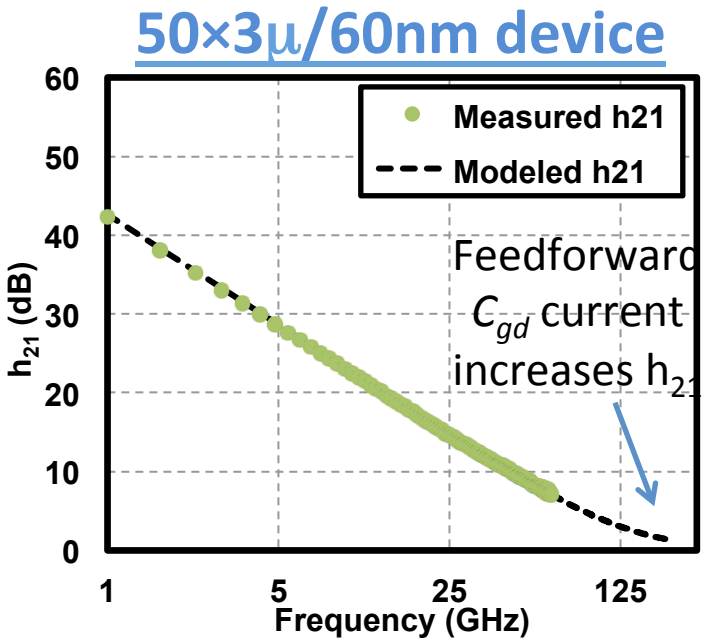


- Lump poly-silicon gate resistance and NQS gate resistances into a single r_g.
- Ignore substrate resistance.
- Ignore threshold modulation.
- Ignore inductive parasitics from vias and layout.

Useful for analysis and intuition.

Unity Current-Gain Frequency (f_T)





$$V_{gs} = i_{IN} / s(C_{gs} + C_{gd})$$

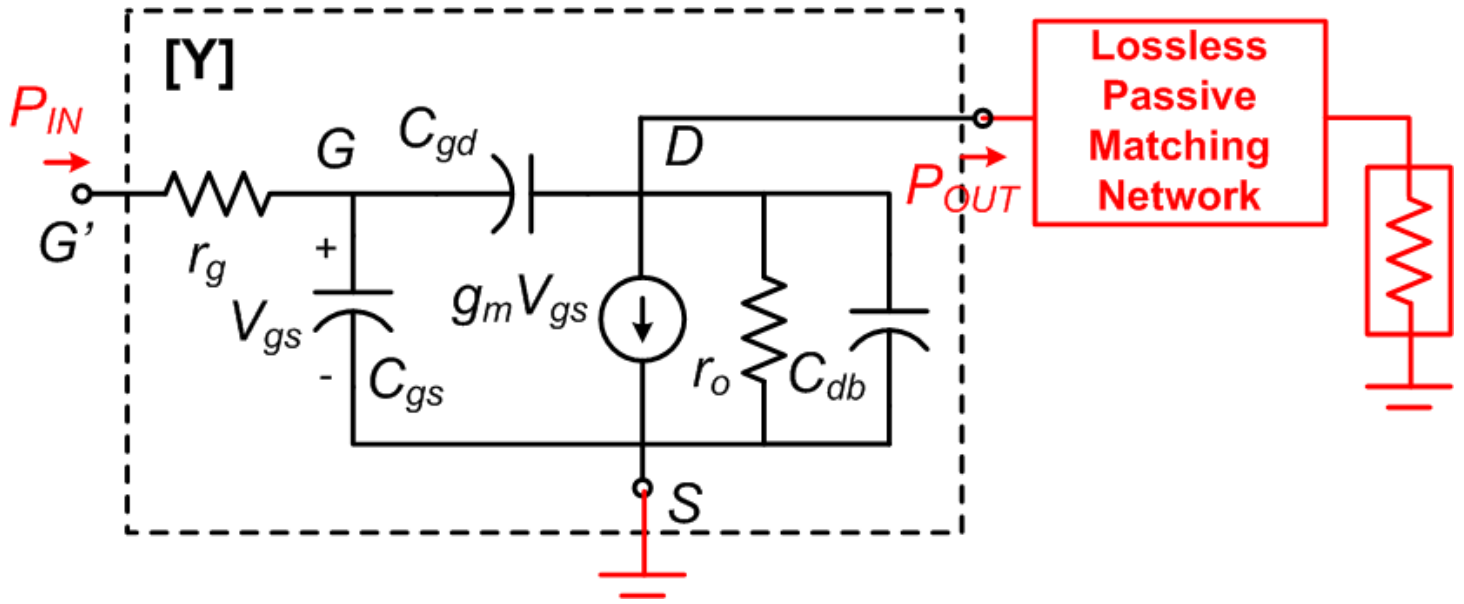
$$\underbrace{i_{OUT} = g_m V_{gs}} \Rightarrow \frac{i_{OUT}}{i_{IN}}(\omega) = \frac{g_m}{j\omega(C_{gs} + C_{gd})}$$

Ignoring feed-forward C_{gd} current

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

- f_T is the frequency at which device current gain becomes 1.
- Useful for mixed-signal circuits, but not for RF/mmWave.

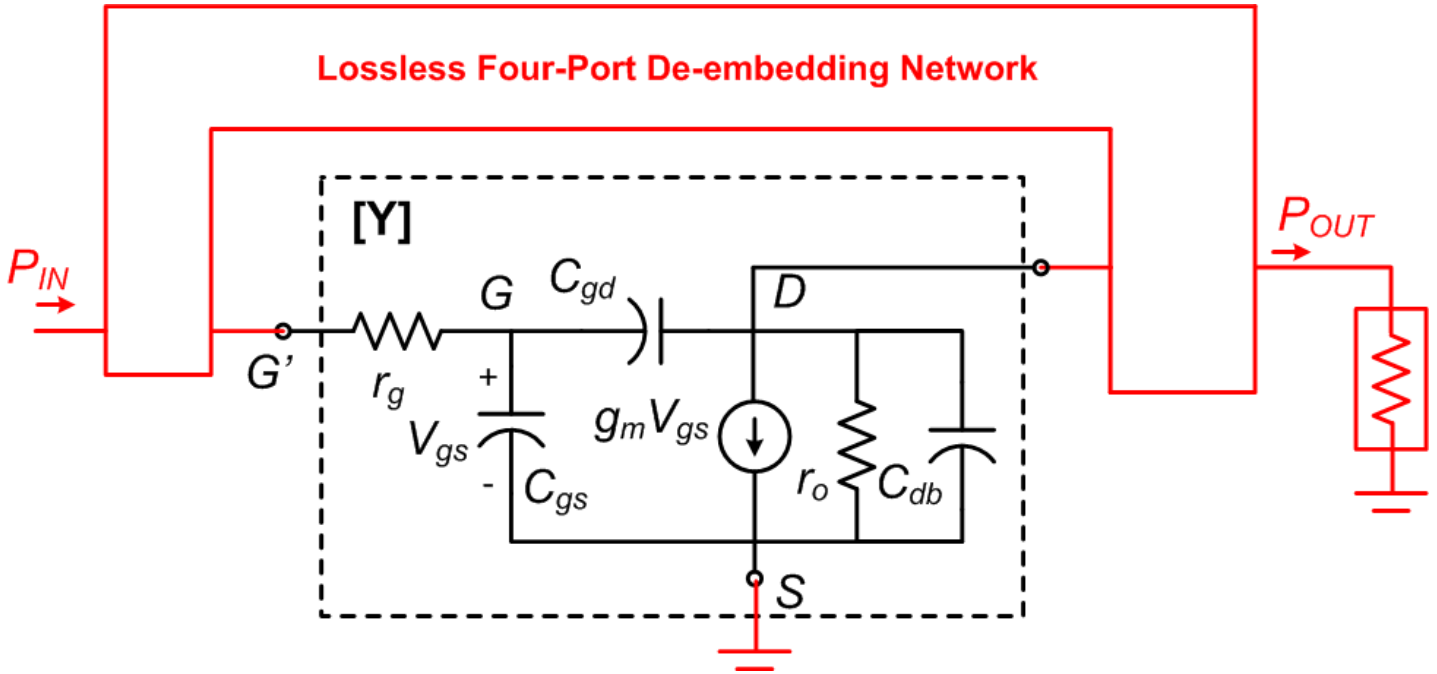
Maximum Available Gain *(MAG)*



$$MAG = \frac{\left|Y_{21}/Y_{12}\right|^2}{x+\sqrt{x^2-1}} \quad \text{where} \quad x = \frac{2\,\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}]-\mathrm{Re}[Y_{12}Y_{21}]}{\left|Y_{12}Y_{21}\right|}$$

- *MAG* is the power gain *(P_{OUT}/P_{IN})* achieved when a lossless passive matching network is used to maximize power gain.
- At low frequencies, MAG is undefined as the device is not unconditionally stable.

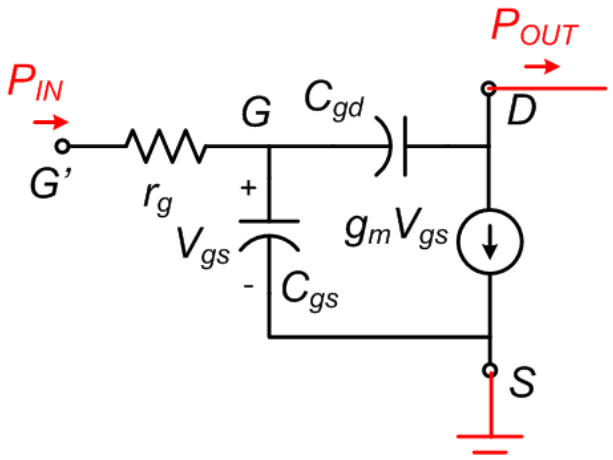
Mason's Unilateral Gain (*U*)



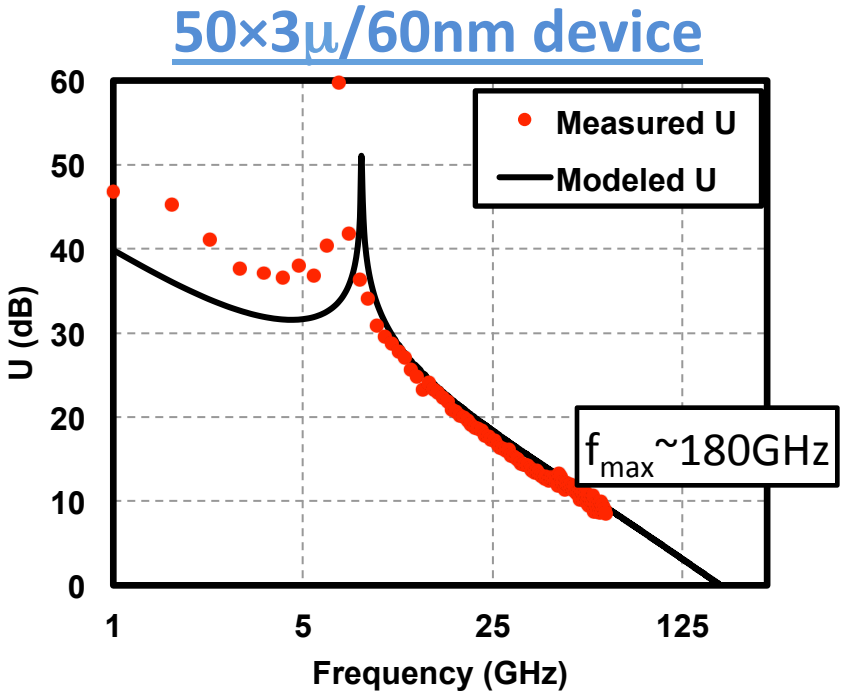
$$U = \frac{\left|Y_{12} - Y_{21}\right|^2}{4(\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}] - \mathrm{Re}[Y_{21}]\mathrm{Re}[Y_{12}])}$$

- *U* is the power gain (P_{OUT}/P_{IN}) achieved when a lossless passive 4-port de-embedding network is used to unilateralize the device.
- Intuitively, U uses feedback to improve power gain beyond MAG.

f_{max}

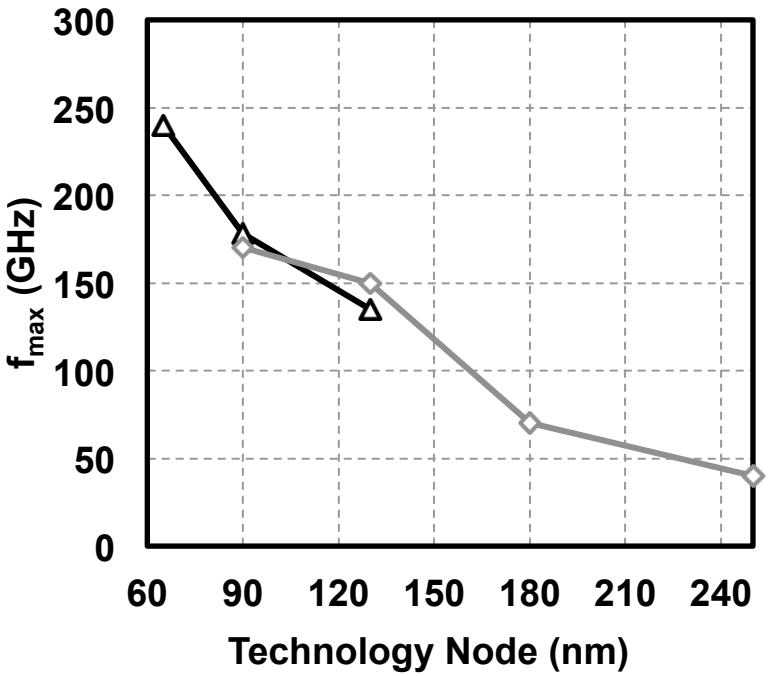


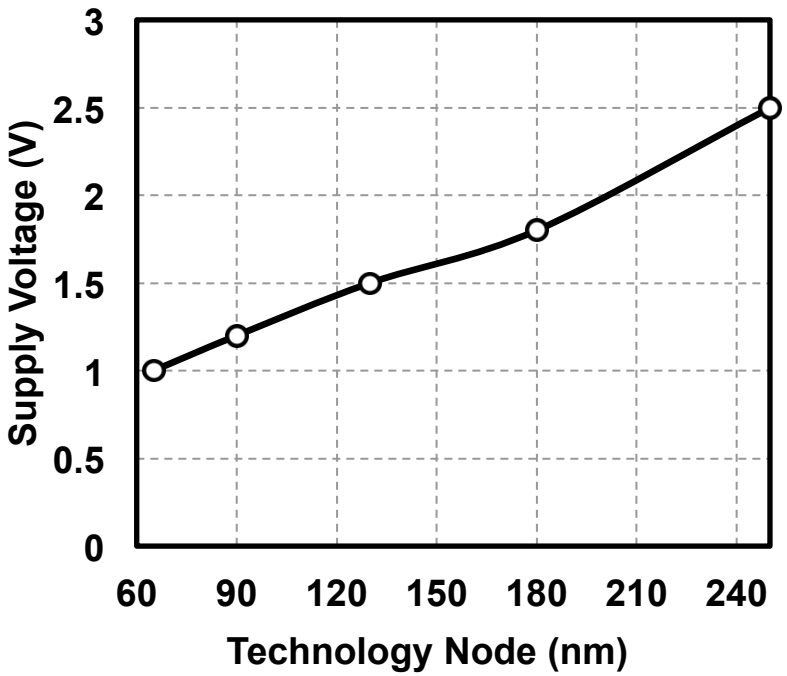
$$f_{\max} = \frac{g_m}{4\pi\sqrt{r_g(C_{gs}+C_{gd})C_{gd}}}$$



- The various power gain metrics such as *U* and *MAG* all become unity or 1 at f_{max}.
- Unlike f_T, f_{max} depends on loss mechanisms within the device.
- f_{max} is also called *Maximum Oscillation Frequency*.

CMOS Technology Scaling

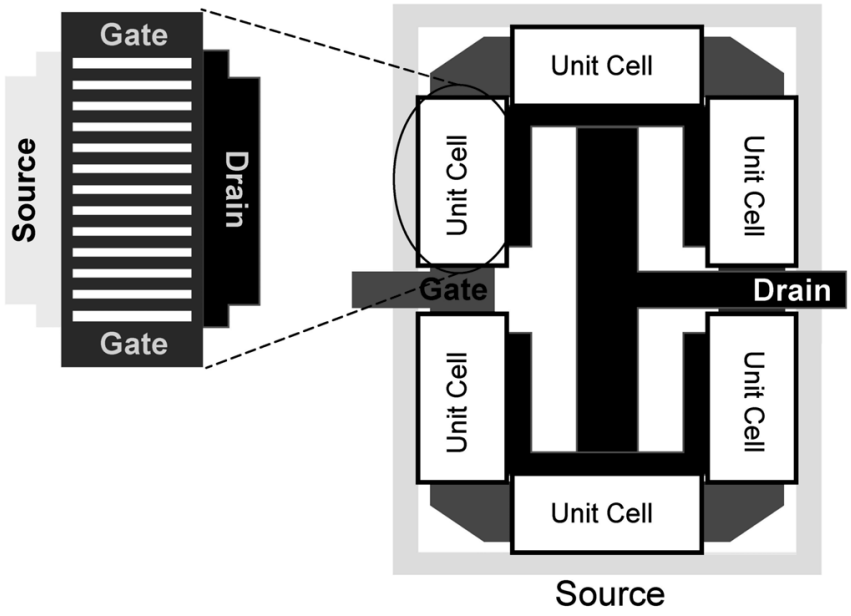


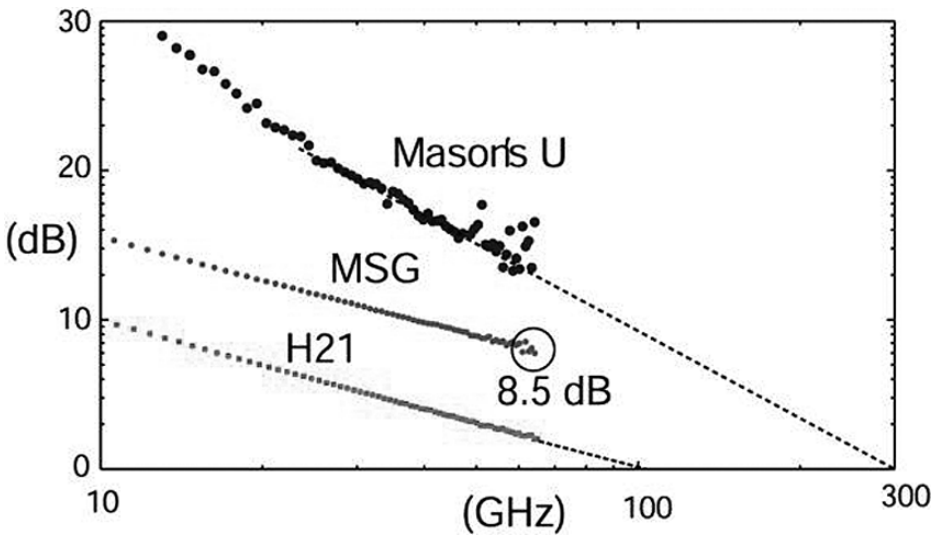


$$f_{\max} V_{DD}^2 \approx 250 \text{ GHz - V}^2$$

- As CMOS technology scales, f_{max} is improving enabling mmWave and even THz circuits and systems.
- Supply voltages are unfortunately reducing as well.
  - Power generation in RX and linearity in RX become challenging.

"Round Table" Layout*

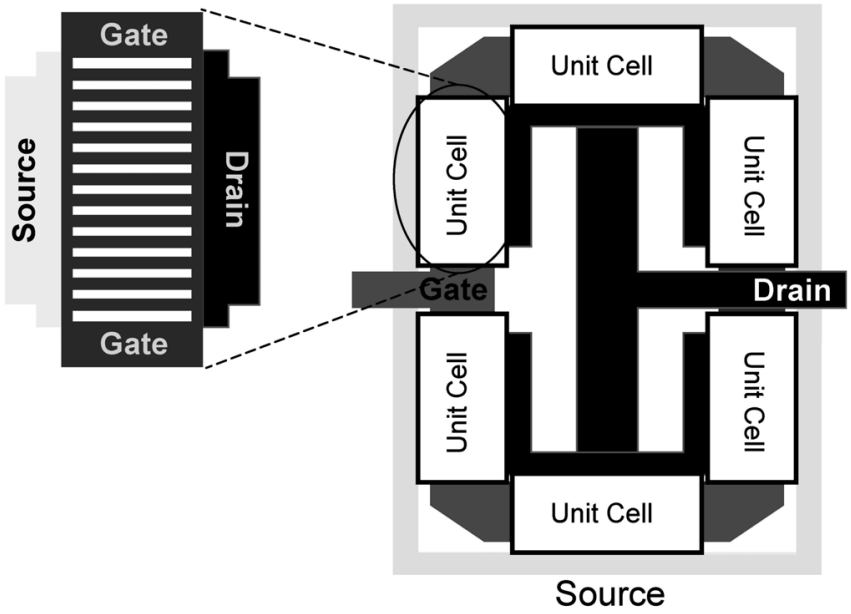




- Can be thought of as a multiplicity approach for large devices.
- Modular approach that can be scaled to larger device sizes.
- Main drawback is that the drain is in the middle of the layout and requires long interconnects to break free.
- Despite high reported f_{max}, this approach is not widely used.

* Figures are the property of the IEEE

"Round Table" Layout*



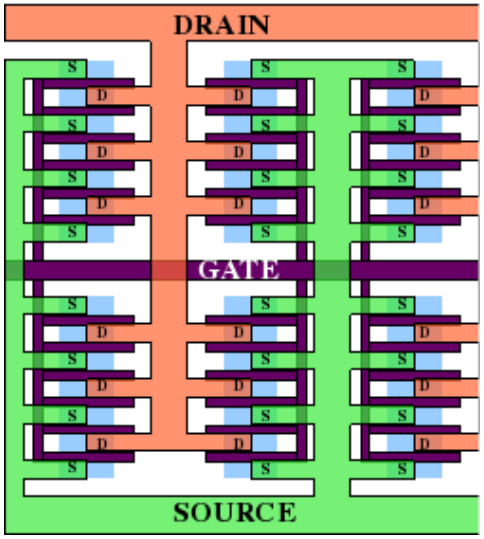
COMPARISON OF SMALL-SIGNAL PARAMETERS FOR A ROUND-TABLE LAYOUT VERSUS A REGULAR MULTI-FINGER LAYOUT

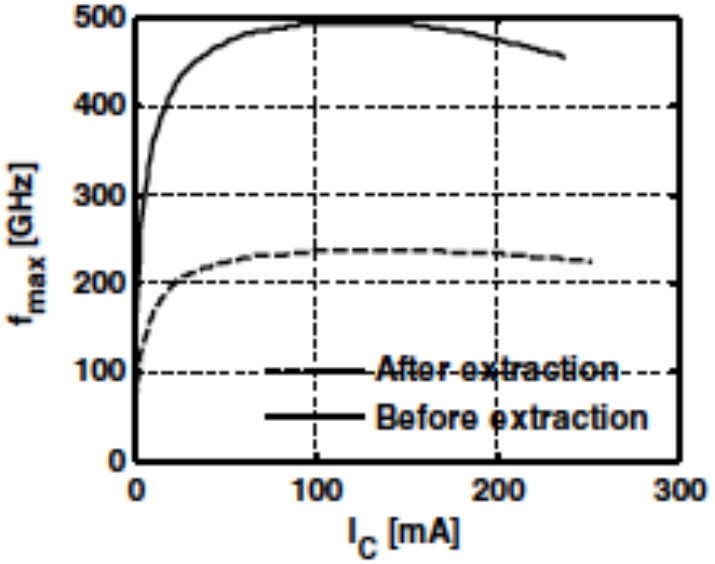
	Regular 1	Round Table
R_g (Ω) (total)	4.46	2.23
R_d (Ω)	3.54	2.42
R_s (Ω)	672m	438m
C_{gs} (fF)	35.7	57.1
C_{gd} (fF)	21.3	17.2

- As can be seen from the measurements, the layout emphasizes resistance over capacitance.
- Heydari, B.; Bohsali, M.; Adabi, E.; Niknejad, A.M., "Millimeter-Wave Devices and Circuit Blocks up to 104 GHz in 90 nm CMOS," in *Solid-State Circuits, IEEE Journal of* , vol.42, no.12, pp. 2893-2903, Dec. 2007 doi: 10.1109/JSSC.2007.908743

* Figures are the property of the IEEE

"Zipper" Layout*

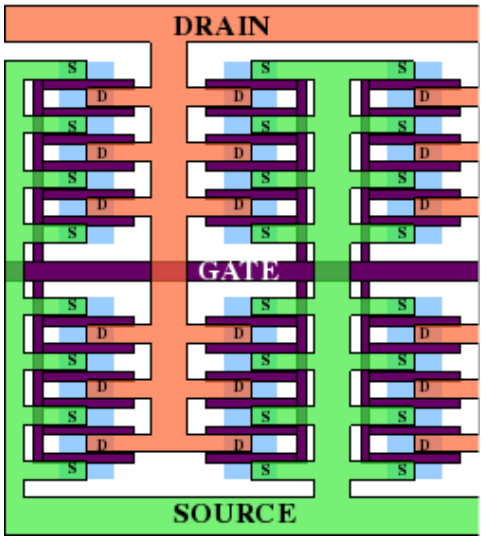


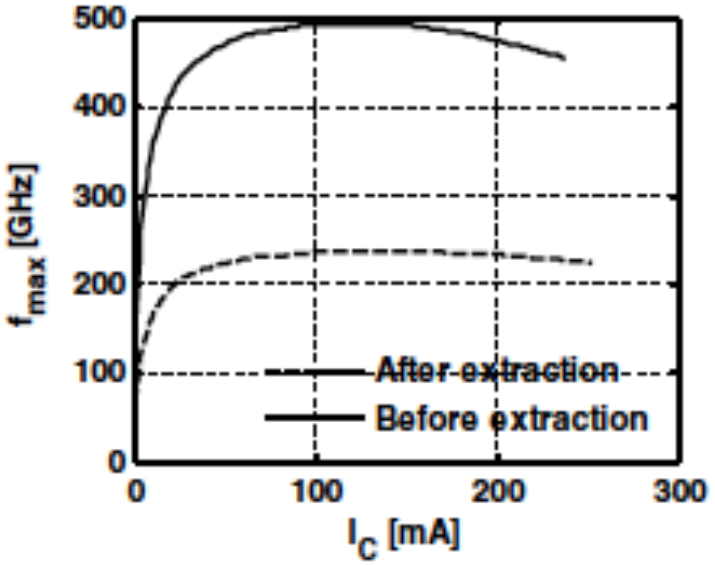


- Can be thought of as a multiplicity approach for large devices. Requires fairly complex EM simulations of the multi-port interconnections.
- Measured f_{max} results are not available in the literature. Simulated fmax is around 240GHz for a 155mm device in 45nm SOI CMOS.

* Figures are the property of the IEEE

"Zipper" Layout*

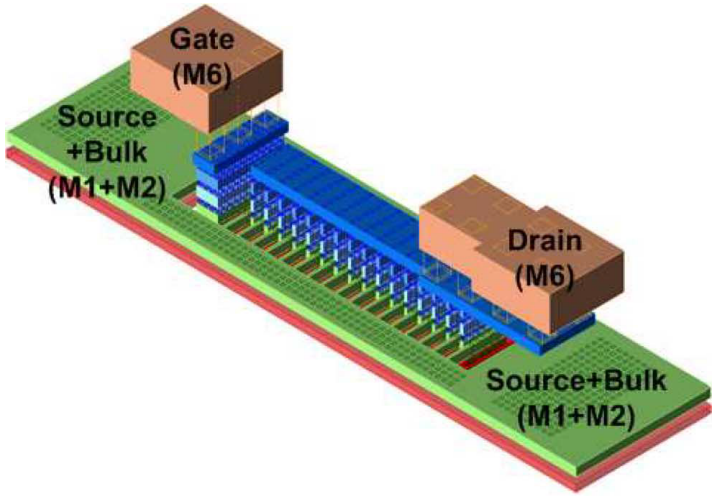




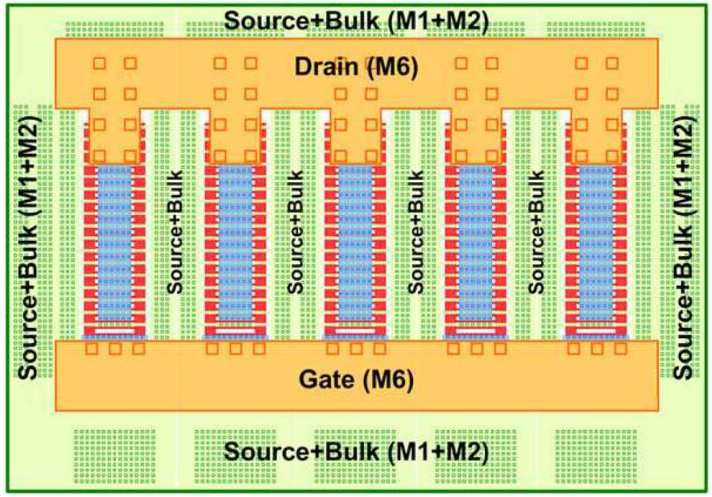
- Pornpromlikit, S.; Dabag, H.-T.; Hanafi, B.; Joohwa Kim; Larson, L.E.; Buckwalter, J.F.; Asbeck, P.M., "A Q-Band Amplifier Implemented with Stacked 45-nm CMOS FETs," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2011 IEEE* , vol., no., pp.1-4, 16-19 Oct. 2011 doi: 10.1109/CSICS.2011.6062465

* Figures are the property of the IEEE

"Drain Above Device" Layout*



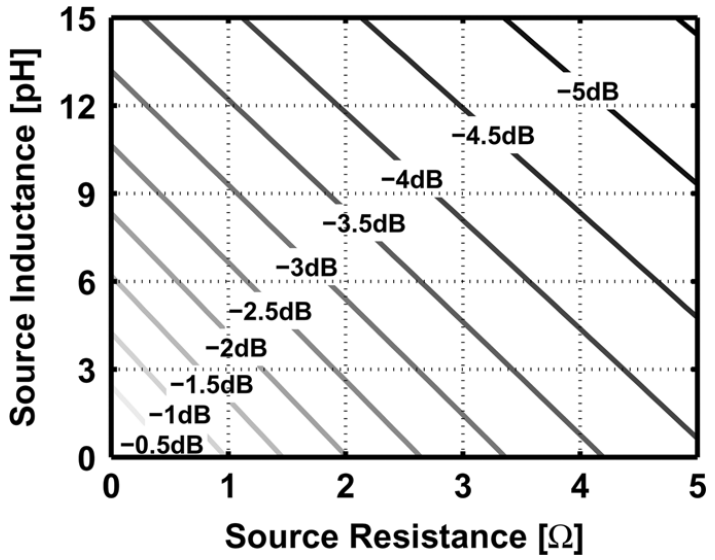
(a)



(b)

- Perhaps the most popular and effective multiplicity approach for large devices.
- Was originally proposed for PA designs because it prioritizes source and drain resistance, while not compromising gate resistance significantly.

Degradation in U due to source wiring.



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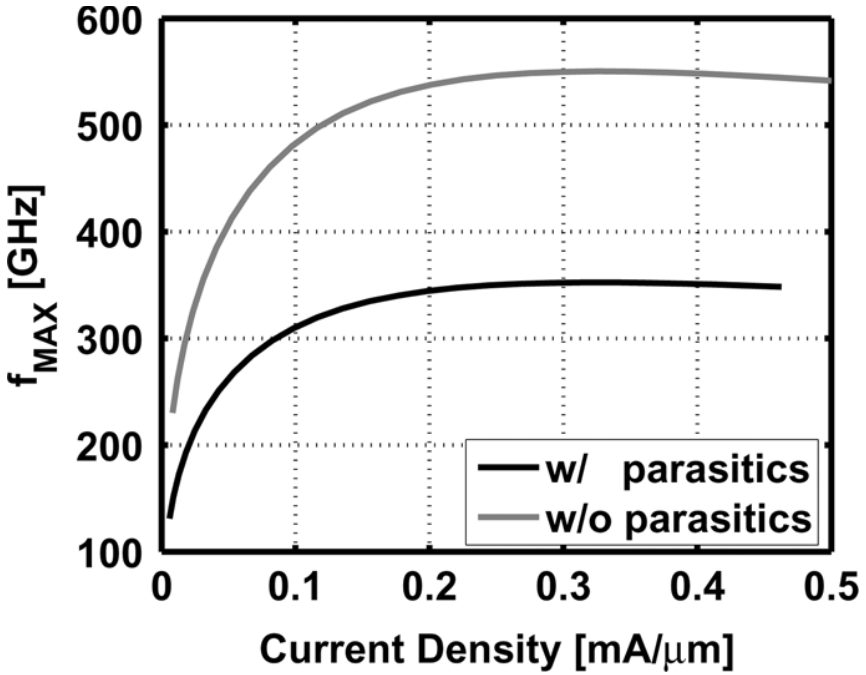
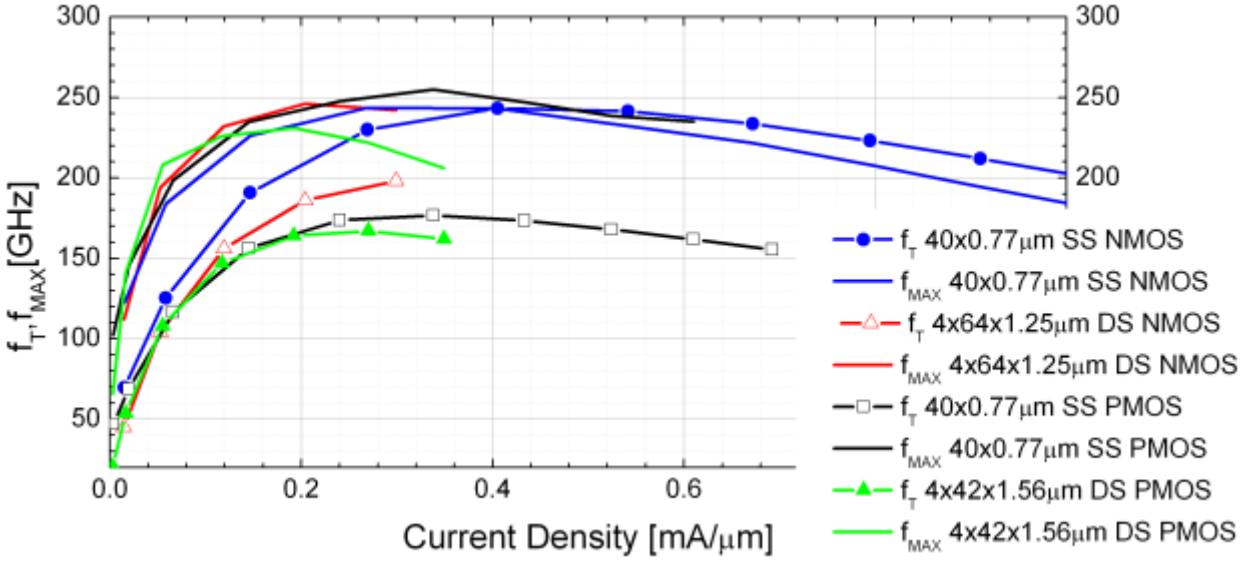


- Measured results are unavailable but simulations indicate ~350GHz f_{max} in 65nm CMOS.

- Dixian Zhao; Reynaert, P., "A 60-GHz Dual-Mode Class AB Power Amplifier in 40-nm CMOS," in *Solid-State Circuits, IEEE Journal of* , vol.48, no.10, pp.2323-2337, Oct. 2013

* Figures are the property of the IEEE

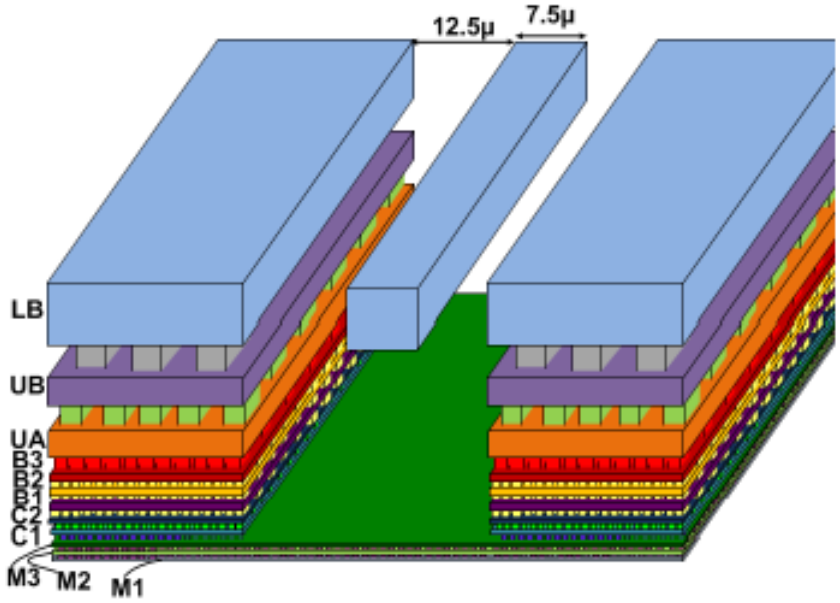
NMOS vs PMOS in Scaled CMOS*



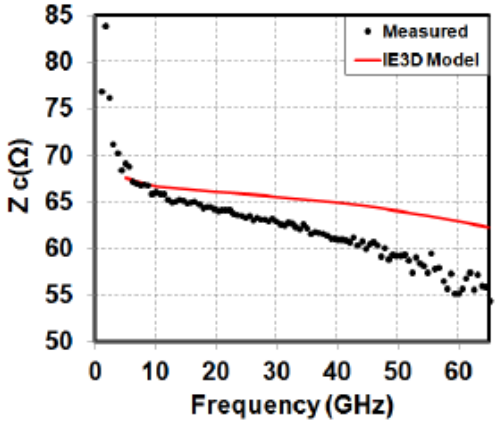
- Due to strain engineering, the mobility of electrons and holes are very similar in highly scaled CMOS. There are reports of fmax being the same for NMOS and PMOS in 45nm SOI.
- A. Balteanu et al., "A 45-GHz, 2-bit power DAC with 24.3 dBm output power, >14 Vpp differential swing, and 22% peak PAE in 45-nm SOI CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE* , vol., no., pp.319-322, 17-19 June 2012.

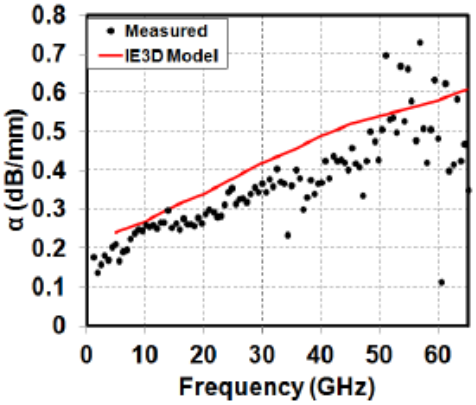
* Figures are the property of the IEEE

Transmission Lines



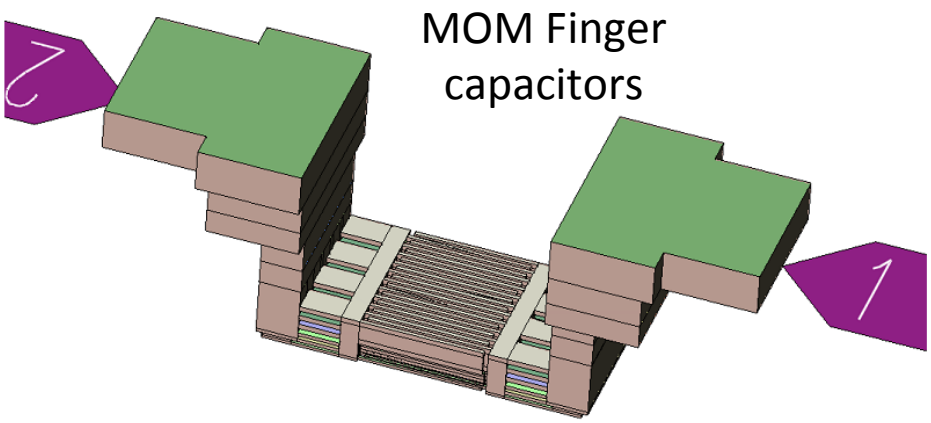
Typical CPW in a 45nm SOI BEOL

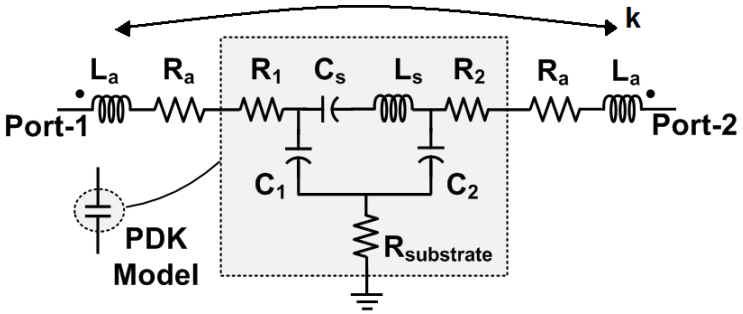


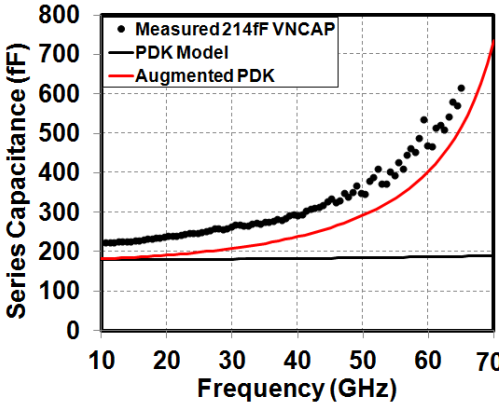


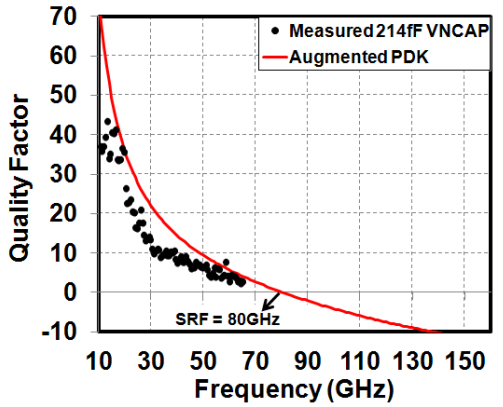
- Popular on-chip t-lines are microstrip, coplanar waveguide (CPW).
  - Microstrips achieve higher characteristic impedance.
  - CPWs achieve better isolation due to side-shielding and help in satisfying metal fill requirements.
- Slow-wave techniques can be used to reduce t-line length.

Capacitors



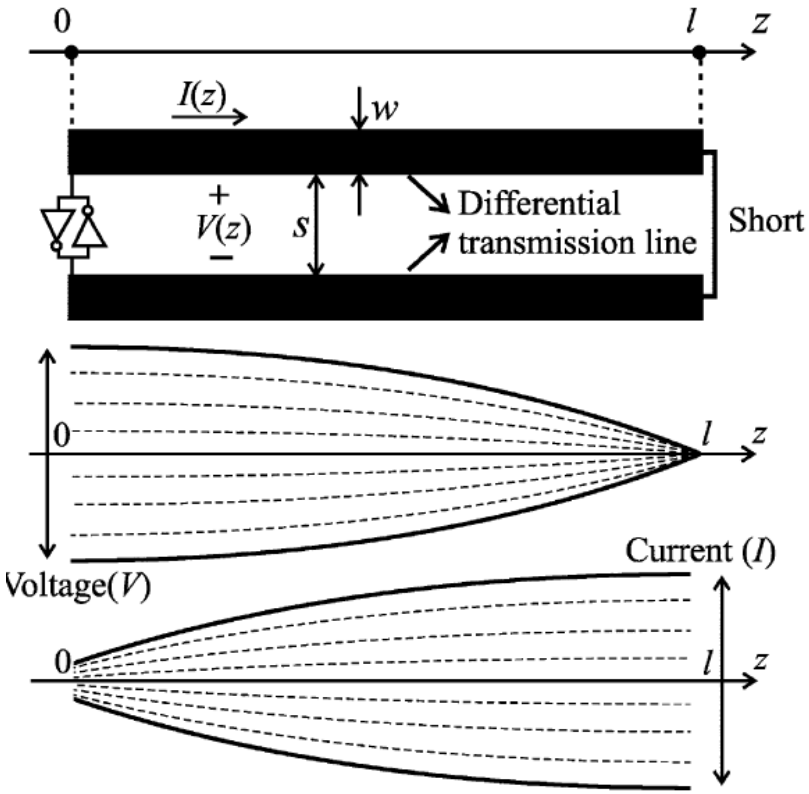






- EM simulations are required to capture high-frequency effects.
  - Self-resonance due to parasitic inductance, skin-effect losses etc.
- Q<10 is typical for mmWave frequencies, making capacitors the bottleneck over inductors.

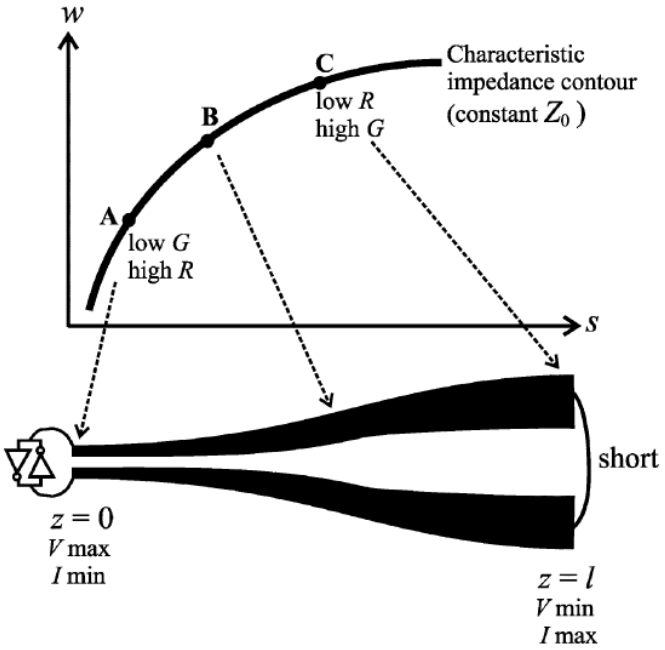
Wave Adaptive Line Tapering*

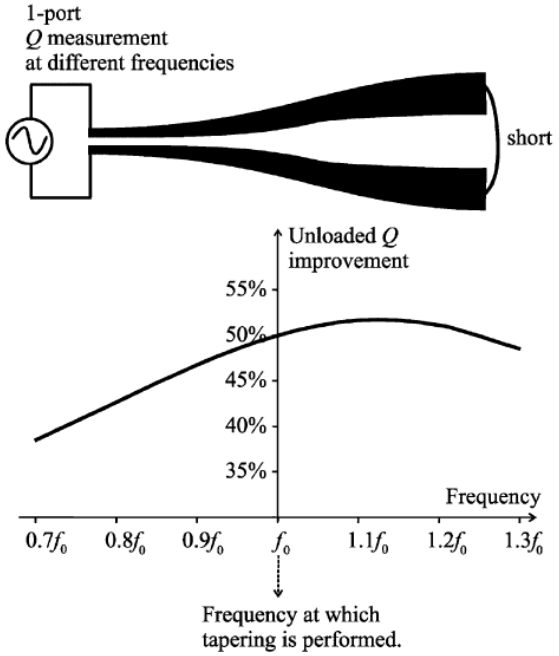


- Transmission-line resonators support standing waves with voltage and current amplitudes that vary along the line.
- Therefore, for different parts of the line, series resistance and shunt conductance play different roles.

* Figures are the property of the IEEE

Wave Adaptive Line Tapering*





- W and S of a shielded CPW can be tapered to reduce R at the expense of G in regions of high current, and reduce G at the expense of R in regions of high voltage.
- Andress, W.F.; Ham, D., "Standing wave oscillators utilizing wave-adaptive tapered transmission lines," in *IEEE JSSC*, vol.40, no.3, pp.638-651, March 2005.

* Figures are the property of the IEEE

Refs for On-Chip Actives/Passives

- C. H. Doan et al, "Millimeter-wave CMOS design," JSSC.
- C. Patrick Yue et al, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," JSSC.
- T. S. D. Cheung et al, "Shielded passive devices for silicon-based monolithic microwave and millimeter-wave integrated circuits," JSSC.
- T. S. D. Cheung et al, "Design and Modeling of mm-Wave Monolithic Transformers," BCTM 2006.

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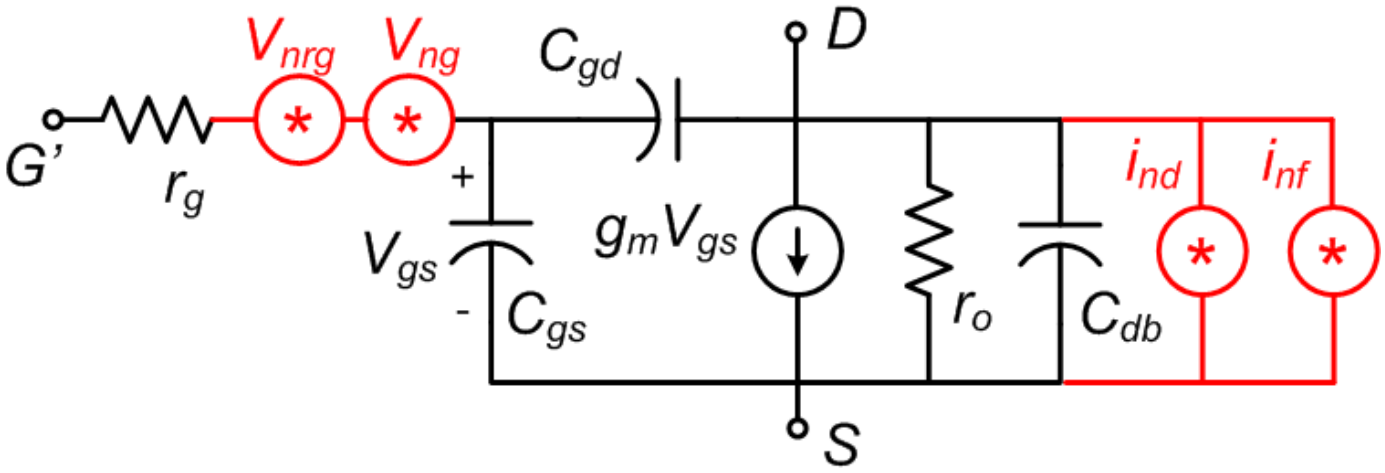
Outline

- Brief History of mmWave in CMOS
- Active and Passive Device Modeling
- **Low-Noise Amplifier Design**
- Oscillators and VCOs
- Power Amplifiers
- Multiple-Antenna Systems

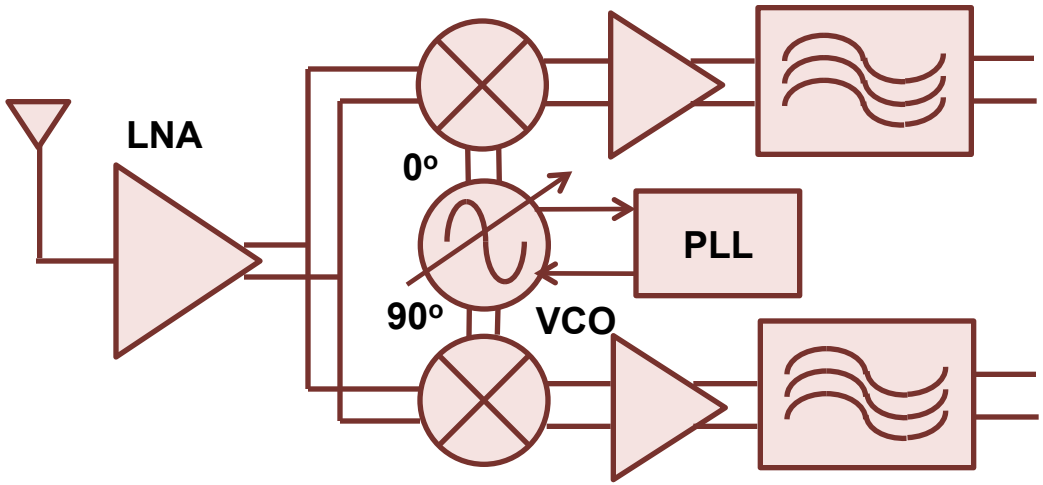
Device Noise Model



$$\frac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma g_{d0} \qquad \frac{\overline{i_{nf}^2}}{\Delta f} = \frac{k}{f}\frac{g_m^2}{WLC_{ox}^2} \qquad \frac{\overline{V_{ng}^2}}{\Delta f} = \frac{4kT\delta}{5g_{d0}} \qquad \frac{\overline{V_{nrg}^2}}{\Delta f} = 4kTr_g$$

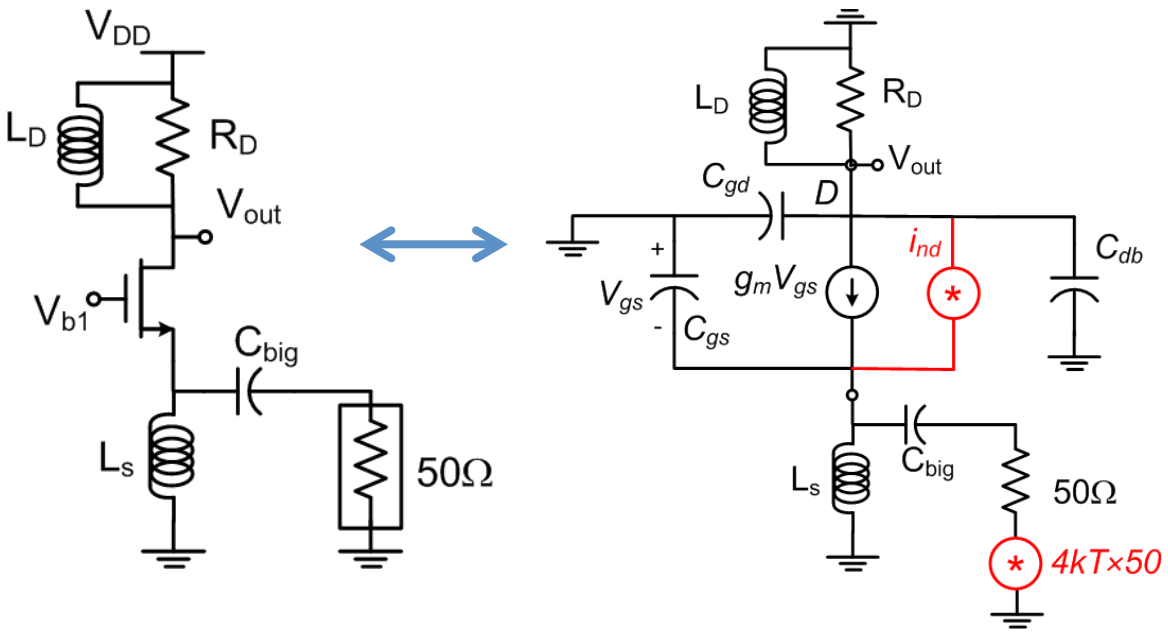
- Flicker noise (i_{nf}) is small at RF/mmWave and can be ignored.
- r_g noise (V_{nrg}) can be made small through good layout.
  - Multiple fingers, doubly-contacted gate, multiplicity layouts.
- Gate induced noise (V_{ng}) is correlated with i_{nd}.

LNA Requirements



- Good Noise Figure (NF).
- High gain.
- Input matching to 50Ω.
- Linearity.
- Low power consumption.
- Robustness to PVT.

Common-Gate LNA



Input match

$$\frac{1}{g_m} = 50\Omega,\ \omega L_s = \frac{1}{\omega C_{gs}}$$

Gain

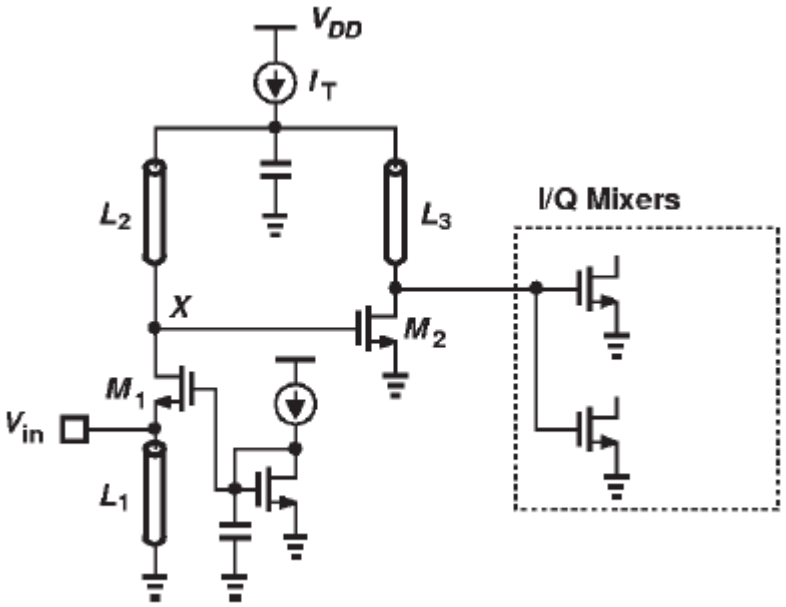
$$A_v = g_m R_D = \frac{R_D}{50\Omega}$$

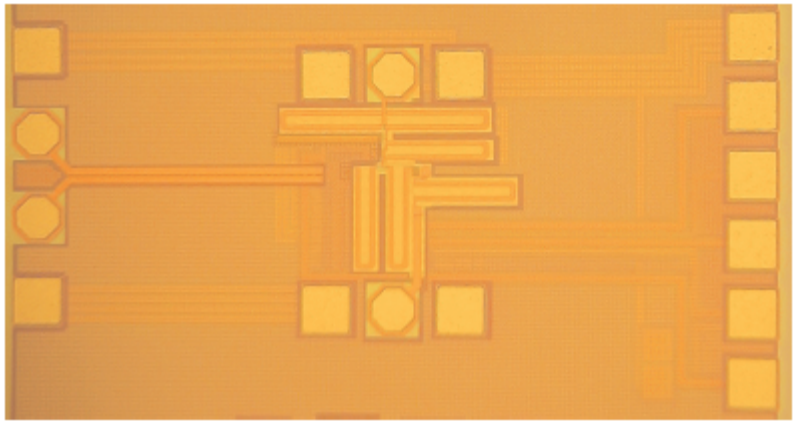
Noise Figure

$$NF = 1 + \gamma g_{d0} \times 50\Omega$$
$$\approx 1 + \gamma g_m \times 50\Omega$$
$$\approx 1 + \gamma$$

- $1/g_m$ input impedance at source used to achieve input match.
- Poor noise performance as device g_m is constrained by input match requirement.
  - $1+\gamma$ = 2-3 (3-5dB) in deep sub-micron CMOS.
  - Need 50Ω input imp. w/o the noise of a 50Ω resistance.

A Common-Gate LNA at 60GHz*

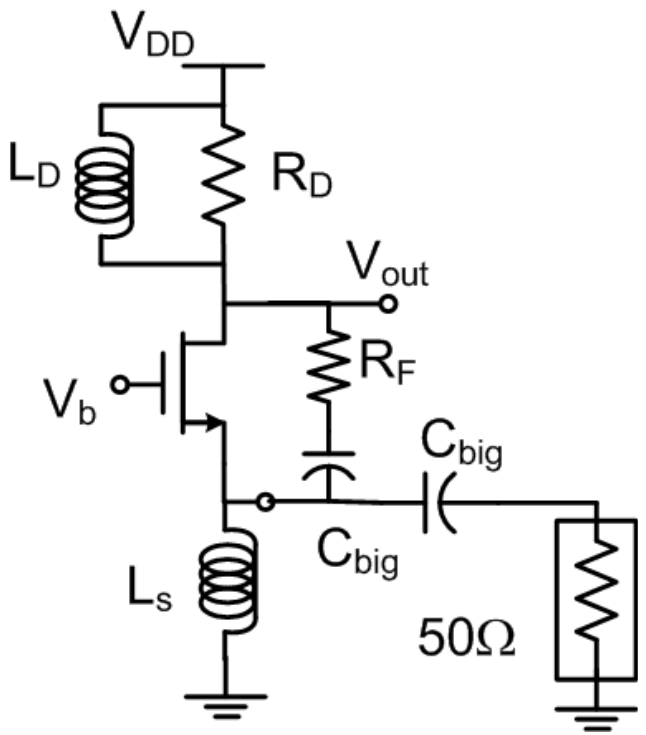




- B. Razavi, "A 60GHz Direct-Conversion CMOS Receiver," ISSCC 2005.
- Simulated NF is 4.5dB (measured RX NF is 12.5dB).
- Power dissipation = 4mA ×1.2V = 5mW.
- 130nm CMOS technology.

* Figures are the property of the IEEE

CG-LNA with Resistive Feedback



Input match

$$\frac{R_D + R_F}{g_m R_F + 1} = 50\Omega, \omega L_s = \frac{1}{\omega C_{gs}}$$

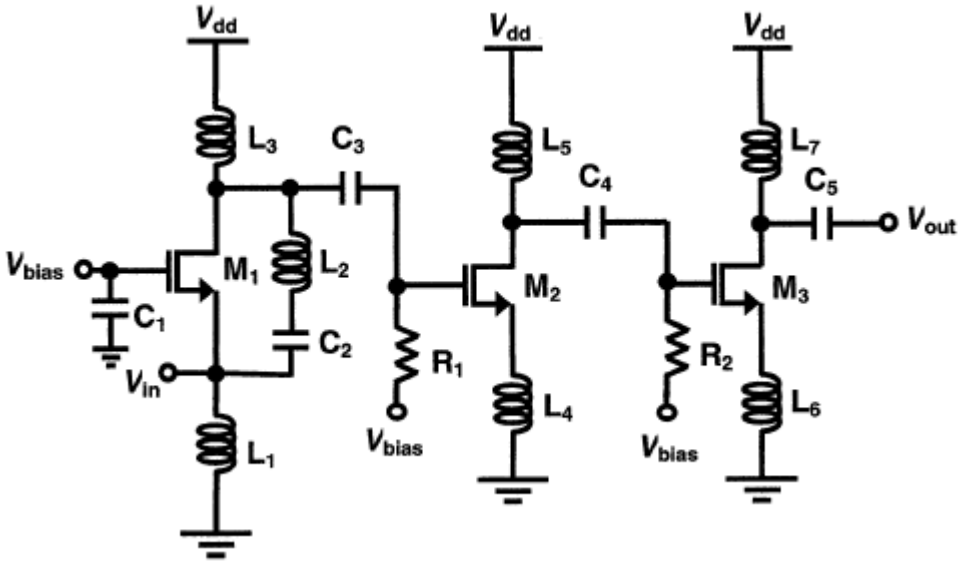
Noise Figure

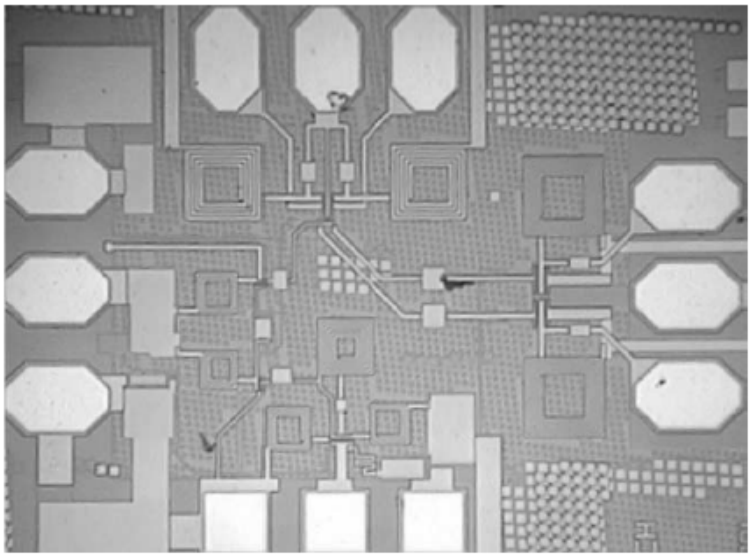
$$NF = 1 + \gamma g_m \times 50 \frac{R_F^2}{(R_D + R_F)^2} + \frac{50}{R_F} \frac{R_F^2}{(R_D + R_F)^2}$$

$$\approx 1 + \frac{\gamma}{g_m \times 50} \text{ if } g_m \times 50 >> 1$$

- g_m can be increased beyond 20mS while achieving input match.
- NF improves as g_m is increased.
  - Analysis takes into account i_{nd} and noise of R_F.

A 24GHz Implementation in 0.18μm*

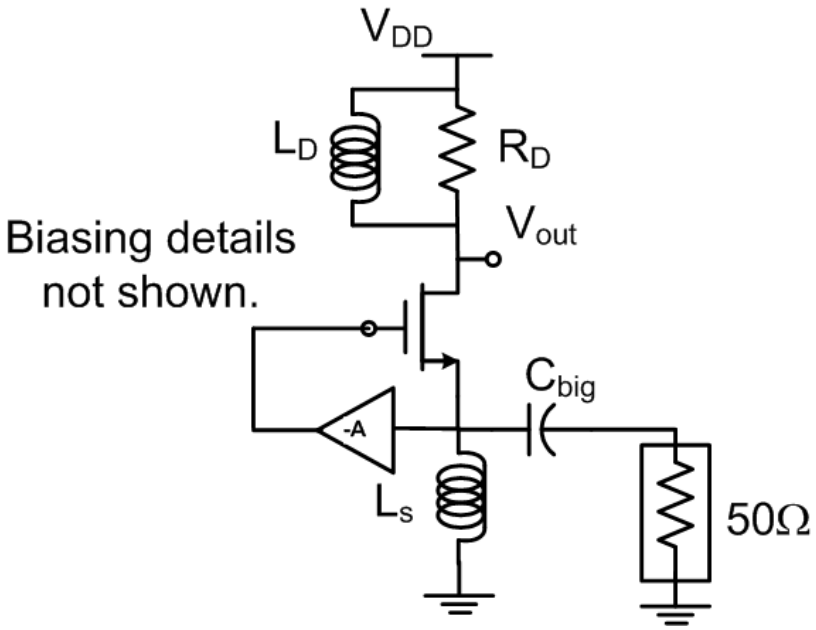




- Guan and Hajimiri, "A 24-GHz CMOS Front-End," JSSC.
- Feedback resistor is realized from the parasitic loss of a feedback inductor (L_2) that resonates substrate capacitance.
- Front-end NF=7.7dB, LNA NF=6dB (sim.), CG-R_F 1st stage NF=4.8dB.
- LNA P_{dc}=24mW.

* Figures are the property of the IEEE

Common-Gate with Gm-Boosting



Input match

$$\frac{1}{g_m(A+1)} = 50\Omega, \omega L_s = \frac{1}{\omega(A+1)C_{gs}}$$

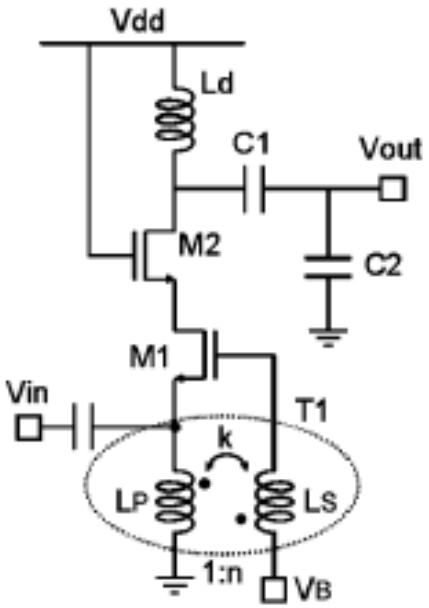
Noise Figure

$$NF \approx 1 + \frac{\gamma}{A+1}$$

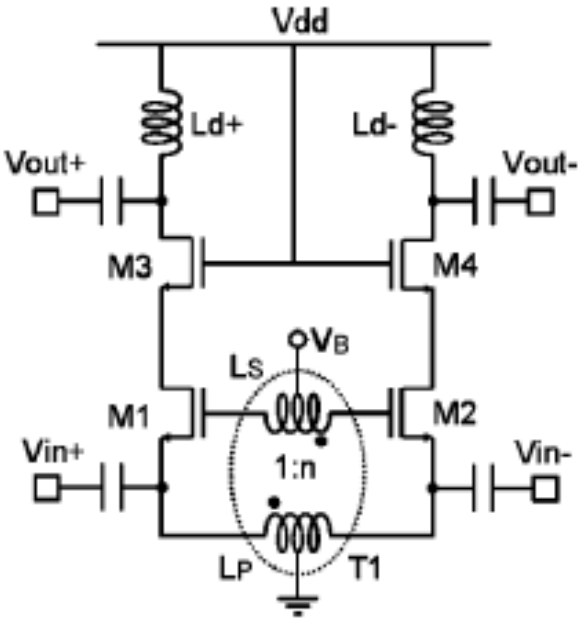
- Amplification from source to gate boosts g_m, enables a smaller g_m to be used to implement input matching.
  - NF reduces by *A+1*.
  - Noise of boosting amplifier must be taken into account.
- Not really explored at mmWave …

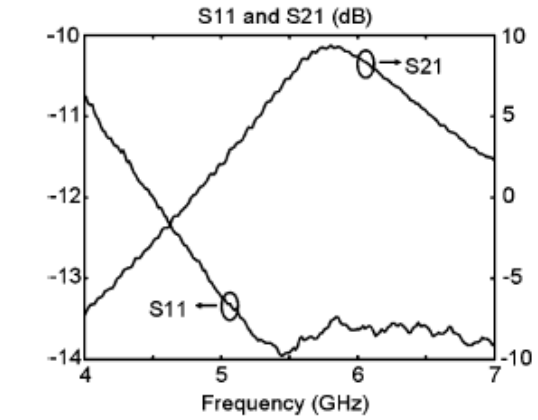
Diff. CG-LNA with Gm-Boosting*

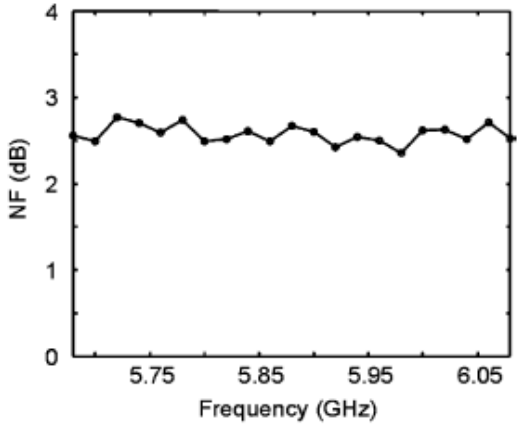
Single-Ended



Differential



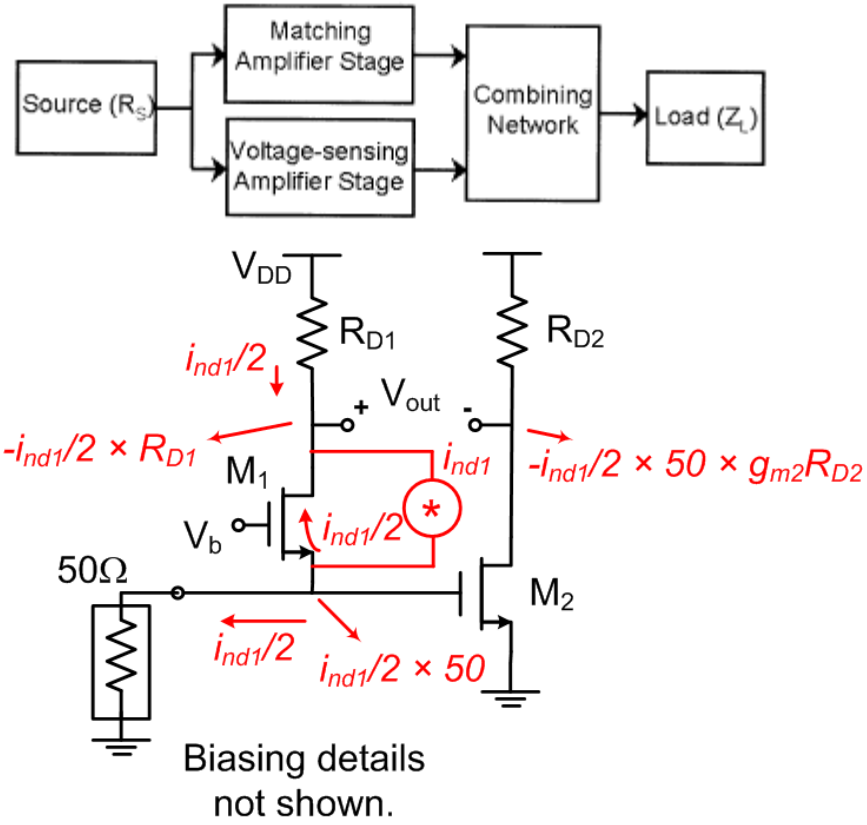




- Xiaoyong Li *et al,* "Gm-Boosted Common-Gate LNA and Differential Colpitts VCO/QVCO in 0.18-μm CMOS," JSSC.
- NF=2.5dB, IIP3=7.6dBm @ P_{dc}=3.4mW.

* Figures are the property of the IEEE

Thermal-Noise Canceling LNA



Input match

$$\frac{1}{g_{m1}} = 50\Omega$$

Noise-Canceling Condition

$$R_{D1} = 50 \times g_{m2} \times R_{D2}$$

$$g_{m1}R_{D1} = g_{m2}R_{D2}$$

Noise-Figure

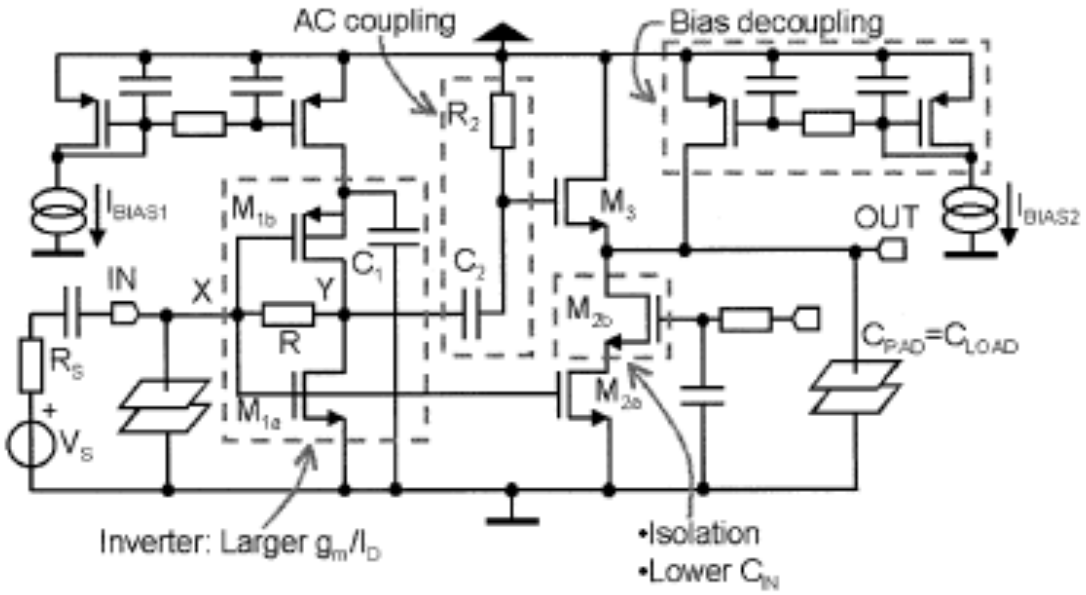
$$NF = 1 + \frac{\gamma}{g_{m2} \times 50}$$

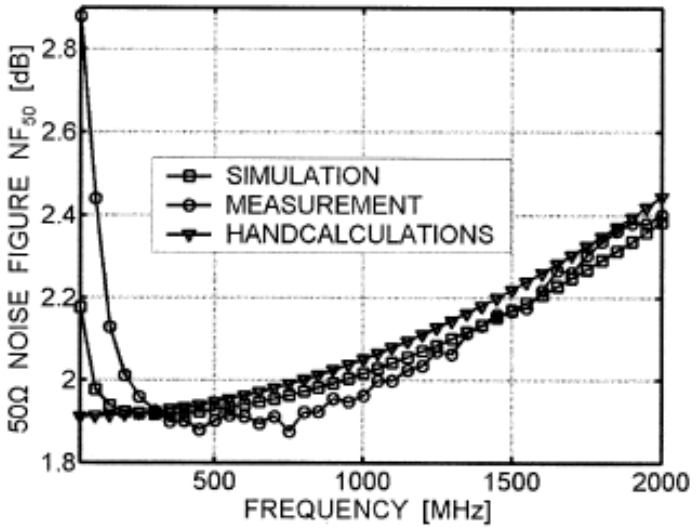
Noise of R_{D1}, R_{D2} and bias circuitry not accounted for.

Not constrained by input matching.

- Voltage sensing stage senses the noise of matching amplifier stage and subtracts it at the output, while adding the signal.
- NF is limited by the sensing stage, loads and bias circuitry.
- Implicit single-ended-to-diff. conversion in the example above.

RF Implementation*

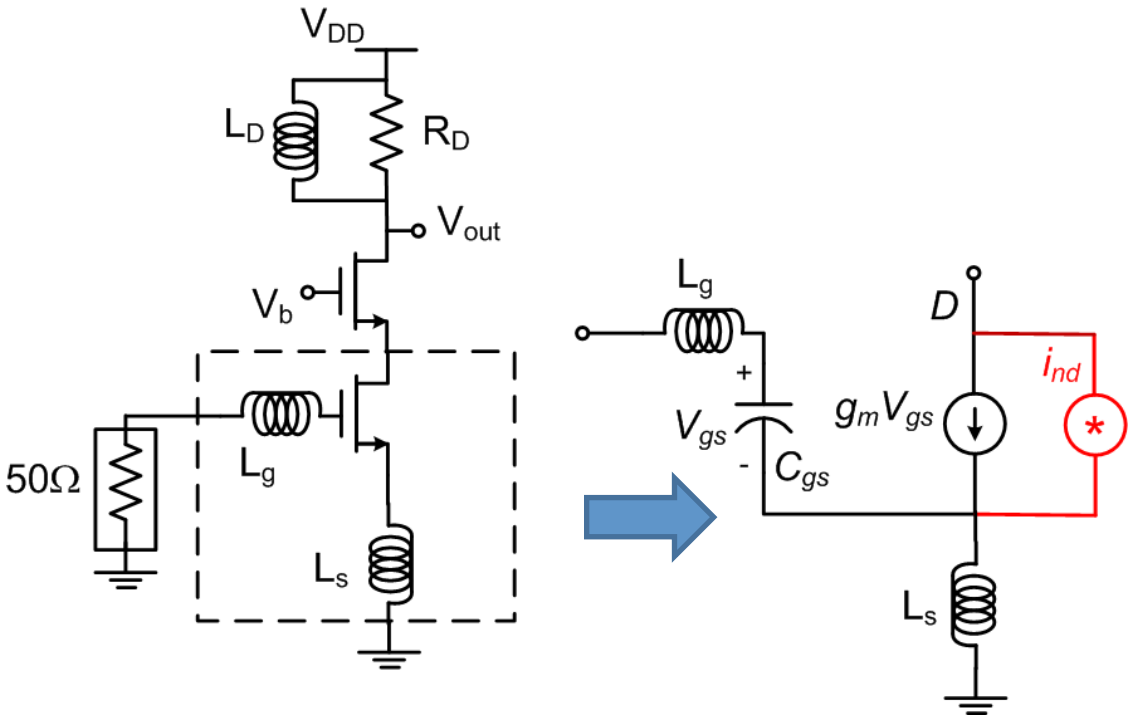




- Bruccoleri et al "Wide-Band CMOS Low-Noise Amplifier Exploiting Thermal Noise Canceling," JSSC.
- Matching stage is an inverter amplifier with shunt feedback.
- M2a, M2b and M3 act as the sensing amplifier and adder.
- IIP2=12dBm, IIP3=0dBm.
- Not explored yet for mmWave ….

* Figures are the property of the IEEE

L_s-Degenerated Common-Source LNA



Input match

$$\frac{g_m L_s}{C_{gs}} = 50\Omega$$

$$\omega(L_s + L_g) = \frac{1}{\omega C_{gs}}$$

Noise Figure

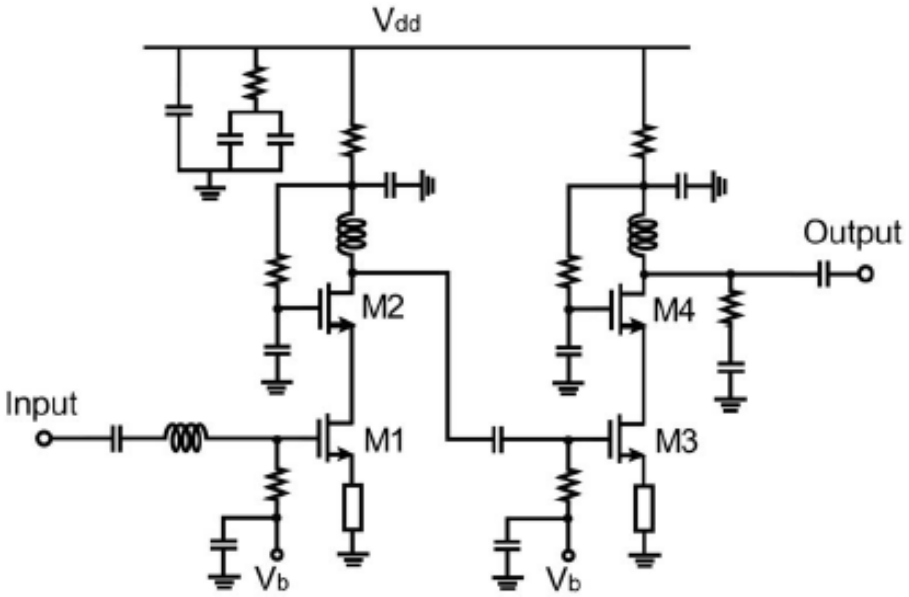
$$NF = 1 + \gamma g_m \times 50\left(\frac{\omega_0 C_{gs}}{g_m}\right)^2$$

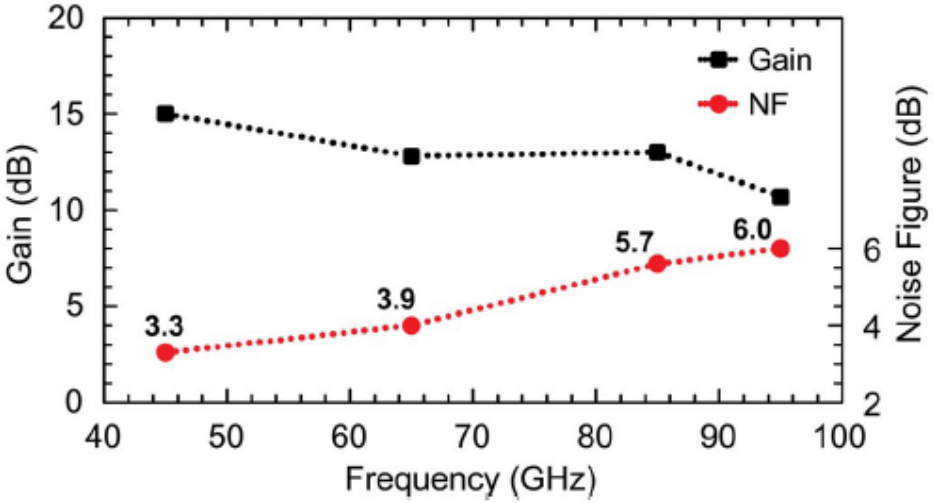
$$\approx 1 + \gamma g_m \times 50\left(\frac{\omega_0}{\omega_T}\right)^2$$

NF is reduced with increasing ω_T

- Inductor degeneration creates a real part to the input impedance without significantly degrading Nf_{min}.
- Shaeffer et al, "A 1.5-V, 1.5-GHz CMOS Low Noise Amplifier, " JSSC.

mmWave Implementations*



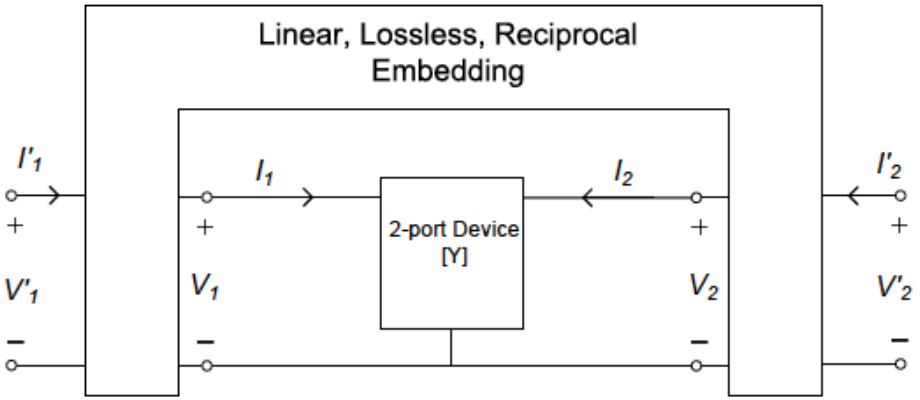


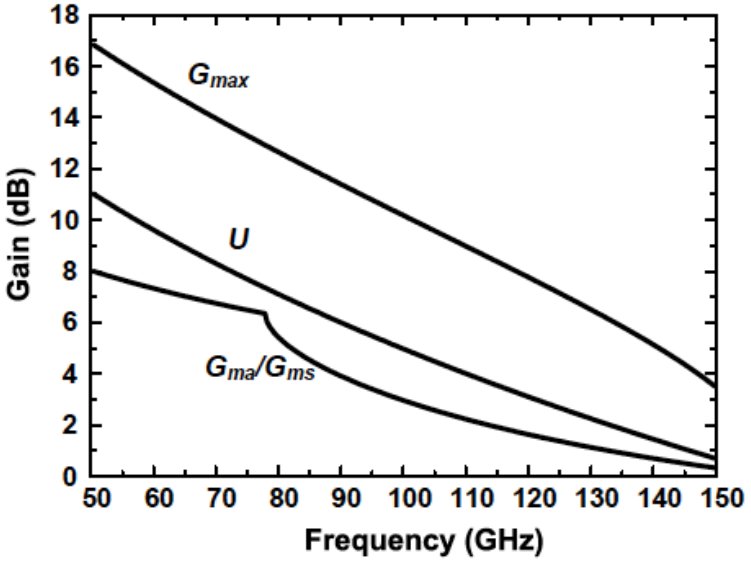
Prototypes implemented at 45GHz, 65GHz, 85GHz and 95GHz in 45nm SOI.

- Ozgur Inac et al, "Millimeter-Wave and THz Circuits in 45-nm SOI CMOS," CSICS 2011.
- This is, by far, the most widely-used LNA topology at mmWave frequencies.

* Figures are the property of the IEEE

What is Maximum Achievable Gain?*



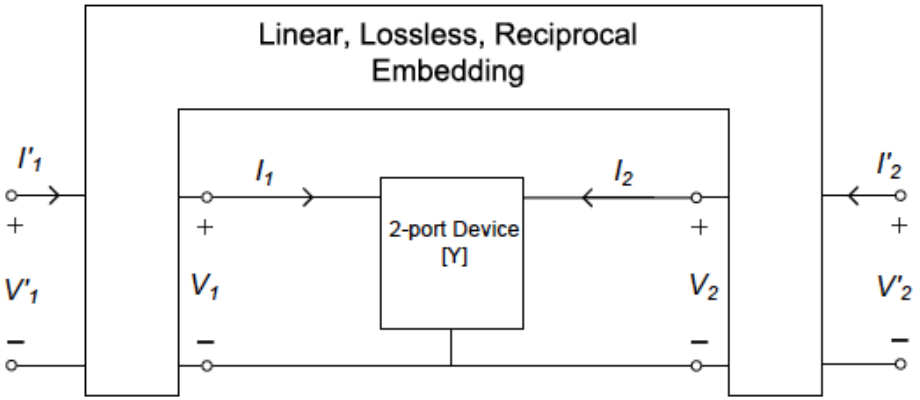


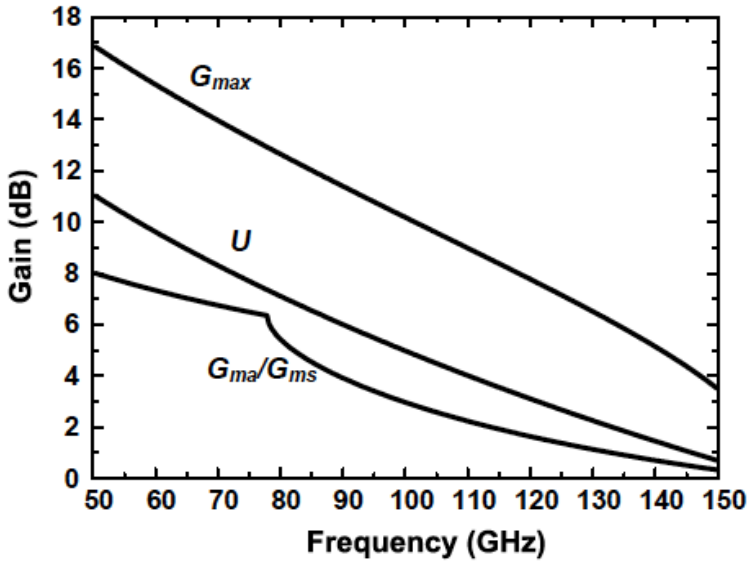
$$G_{max} = (2U - 1) + 2\sqrt{U(U-1)} \simeq 4U$$

- U (Mason's Unilateral Gain) is the Gma when feedback is used to unilateralize the device.

- **G_{max} is the maximum achievable gain when feedback is used under the constraint of unconditional stability.**

What is Maximum Achievable Gain?*





$$G_{max} = (2U - 1) + 2\sqrt{U(U-1)} \simeq 4U$$

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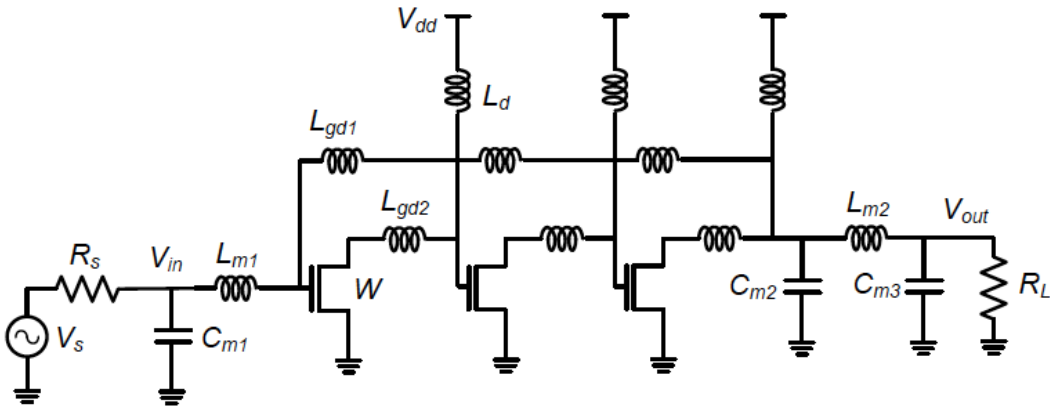
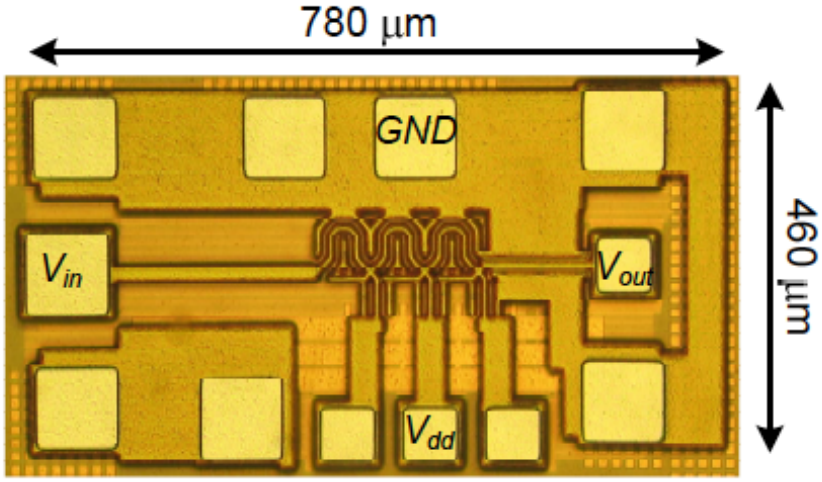
* Figures are the property of the IEEE

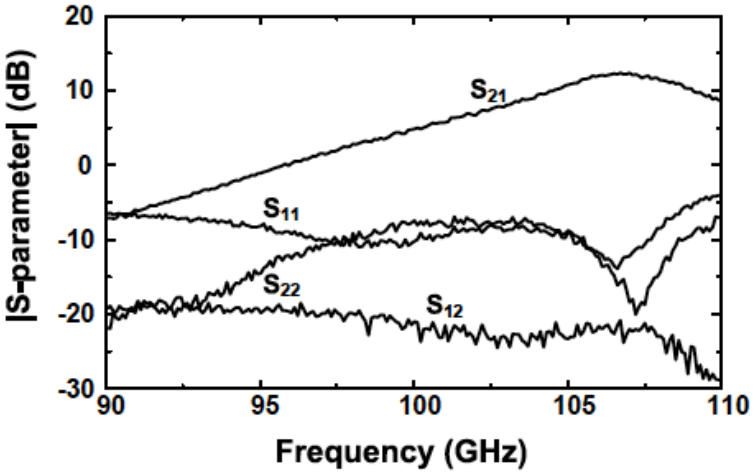
A 107GHz Amplifier in 130nm CMOS*





- A 107GHz amplifier achieves 12.5dB gain very close to f_{max} (~130GHz in 130nm CMOS).

- Momeni, O.; Afshari, E., "A high gain 107 GHz amplifier in 130 nm CMOS," in *2011 IEEE CICC*, no., pp.1-4, Sept. 2011.

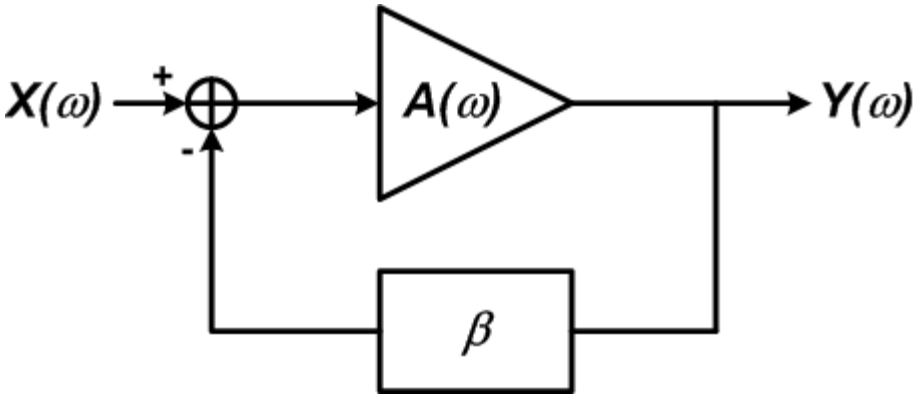


* Figures are the property of the IEEE

Outline

- Brief History of RF/mmWave in CMOS
- Active and Passive Device Modeling
- Low-Noise Amplifier Design
- **Oscillators and VCOs**
- Power Amplifiers
- Multiple-Antenna Systems

Oscillator Basics



$$\frac{Y(\omega)}{X(\omega)} = \frac{A(\omega)}{1 + A(\omega)\beta}$$

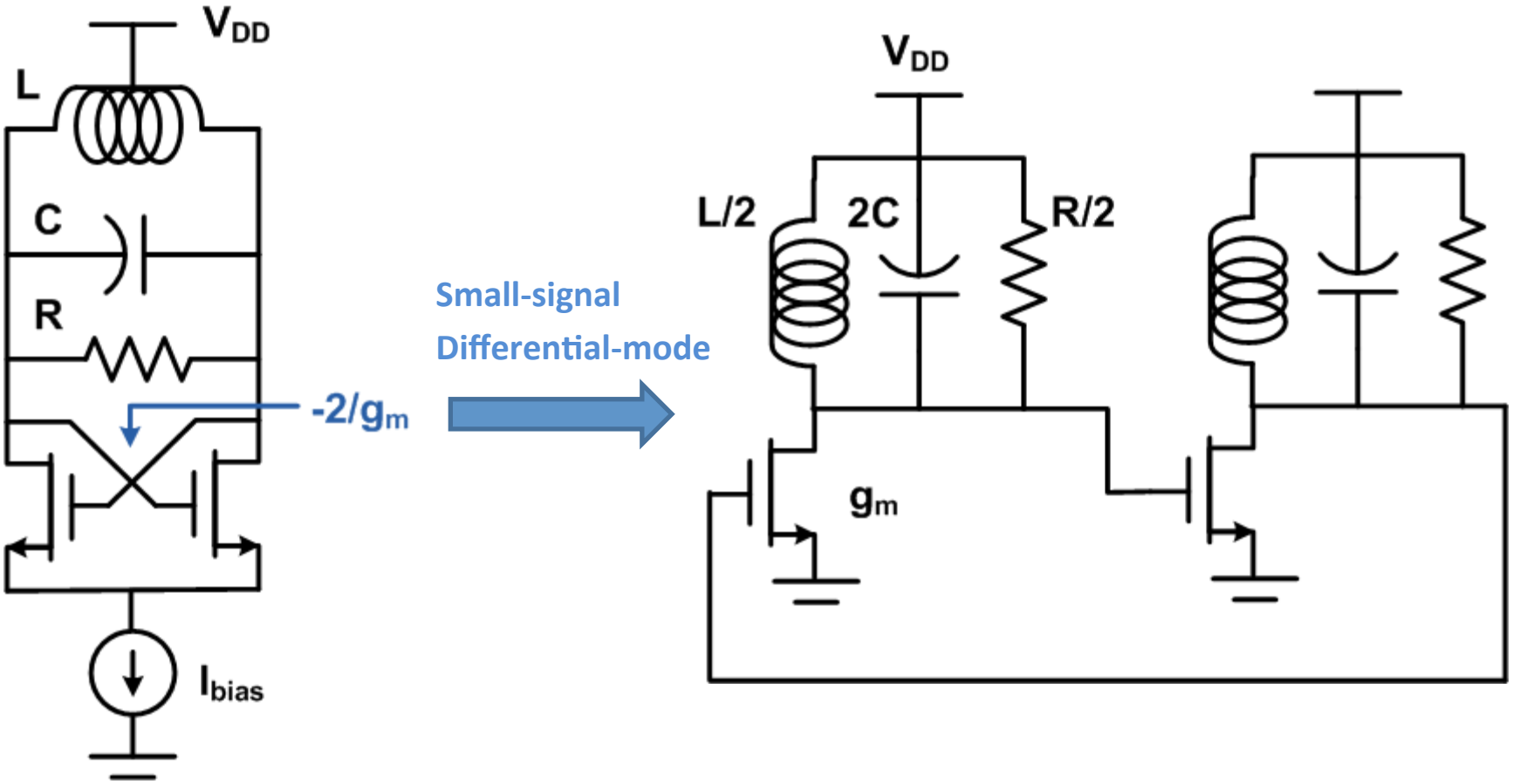
Barkhausen Criteria:

$$\left|A(\omega)\beta\right| > 1$$

$$\angle A(\omega)\beta = 180^{o}$$

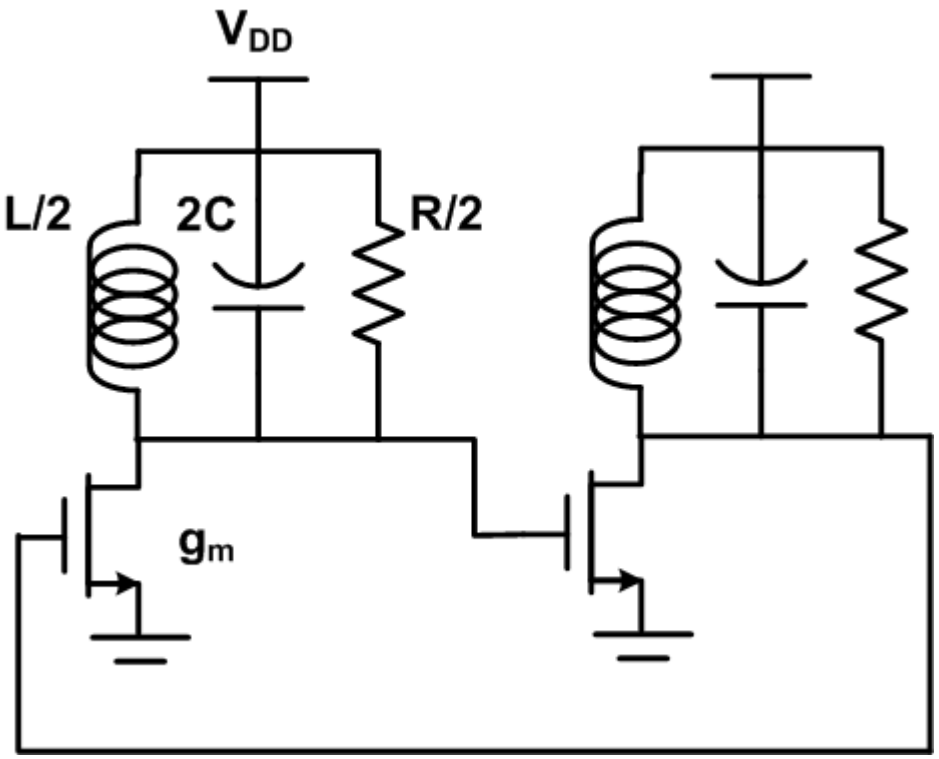
- Magnitude condition is often called *startup gain*.
- Phase condition usually sets the frequency of oscillation.
- In simulation, one usually needs to provide a "kick" to start the oscillation. In life, noise is usually sufficient.

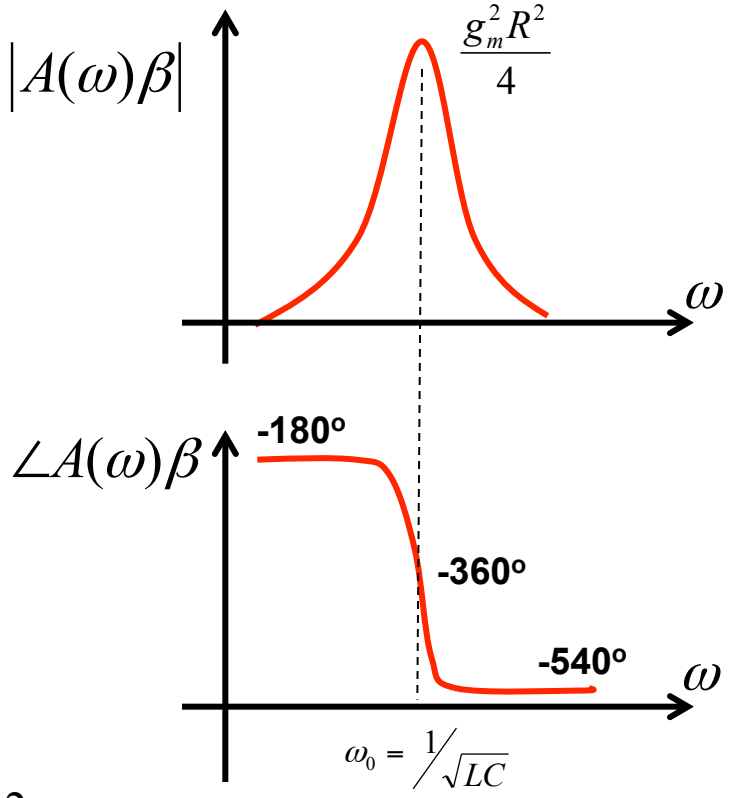
Cross-coupled Oscillator (XCO)



- Can be viewed as a negative-resistance oscillator.
- Can also be viewed as two tuned amplifiers in feedback.
- Parasitic R arises from ind. loss (and capacitor loss at mmWaves)

Startup Condition



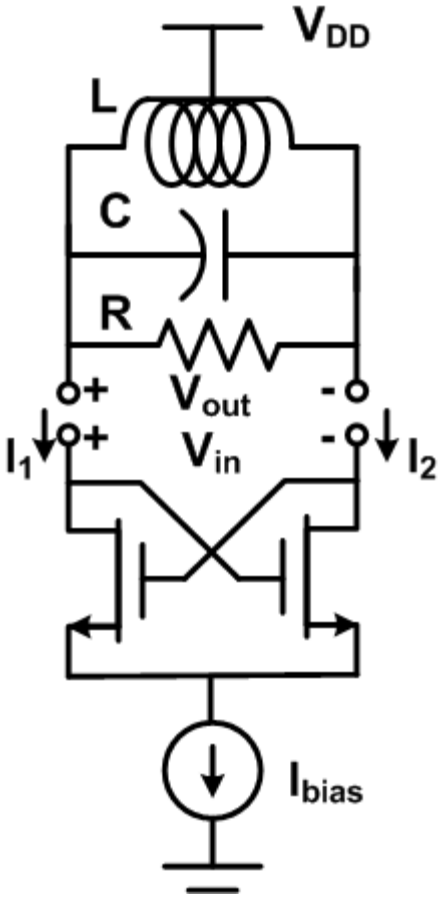


$$A(\omega)\beta = g_m^2 \frac{-\omega^2 L^2}{4(1 + j\omega L/R - \omega^2 LC)^2} = 1$$

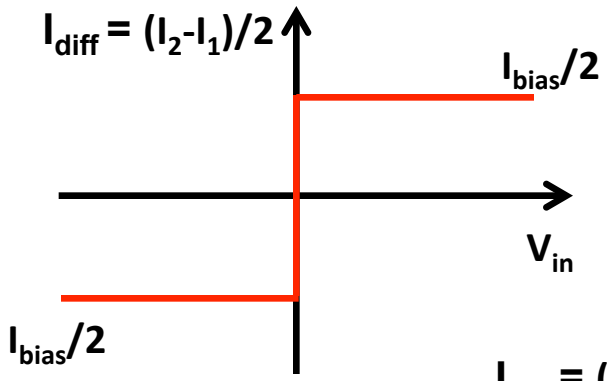
$$g_m R \geq 2$$

$$\omega_0 = 1/\sqrt{LC}$$

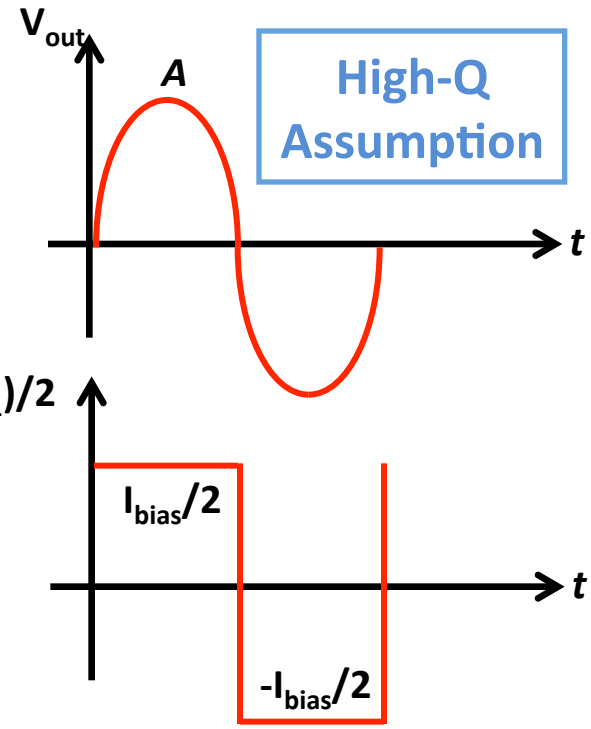
Oscillation Amplitude



Hard-switching Differential Pair Model



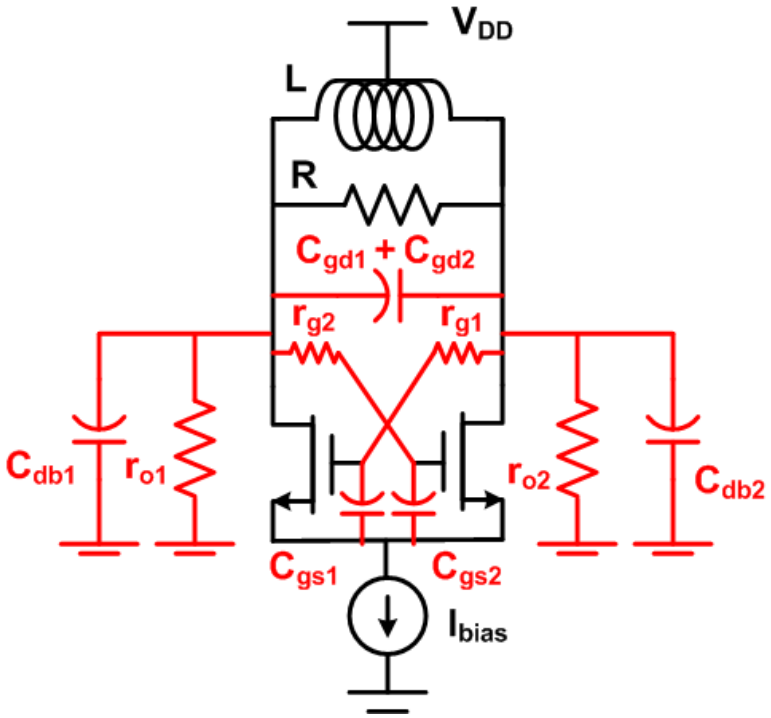
Voltage and Current Profiles



$$A = \underbrace{\frac{4}{\pi}\frac{I_{bias}}{2}}_{\text{Fundamental component of square wave current}} \times \underbrace{R}_{\text{RLC impedance at } \omega_0} = \boxed{\frac{2}{\pi} I_{bias} R}$$

- *A* can be increased to $2V_{DD}$ before it is clipped by the rails.

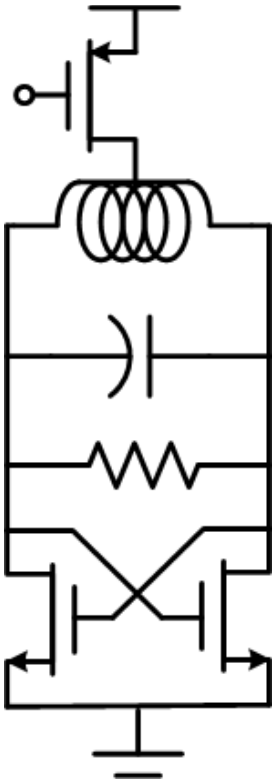
High-Frequency Parasitics



- At mmWave frequencies, device parasitic capacitances are sufficient to resonate with the L (C_{tank}~ $2C_{gd}$ +C_{db}/2+C_{gs}/2).
- Parasitic losses in the device reduce loaded Q of the resonator.
  - Note that use of small-signal device parasitics is only relevant for startup and not large-signal operation.

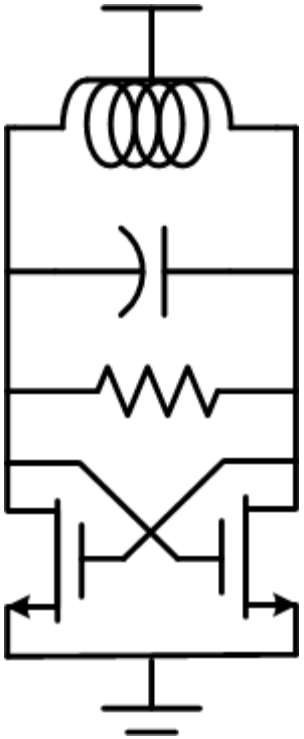
Variants

pMOS-Biased



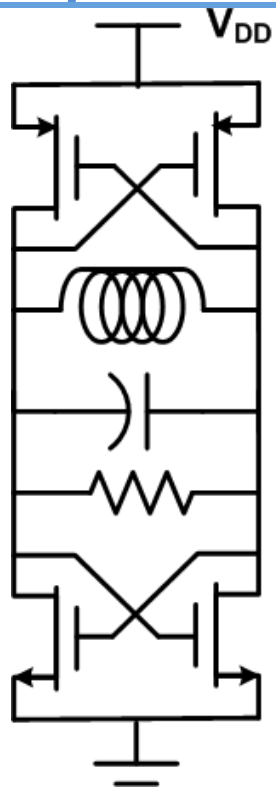
+ pMOS tail current source produces less 1/f noise.

VDD-Biased



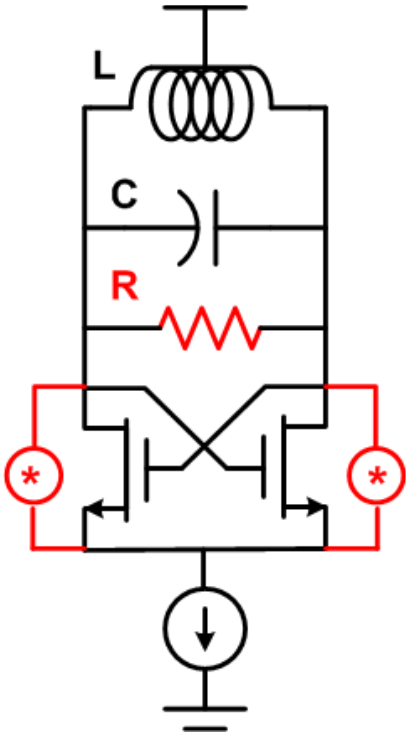
+ Tail current source headroom/ noise eliminated.
- Oscillator bias current, amplitude and noise performance are affected by PVT.

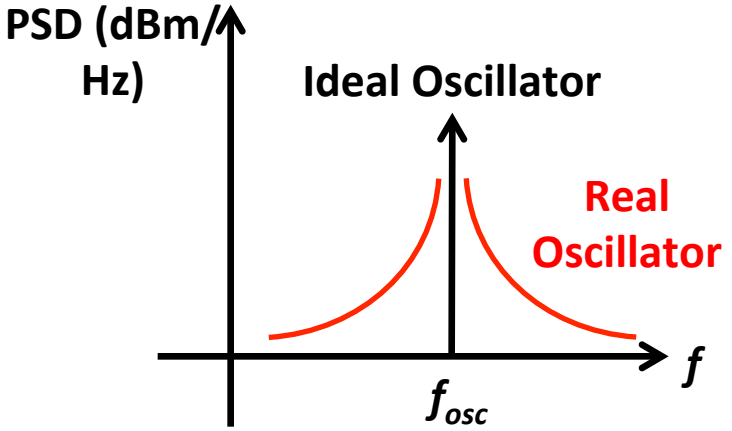
Complementary

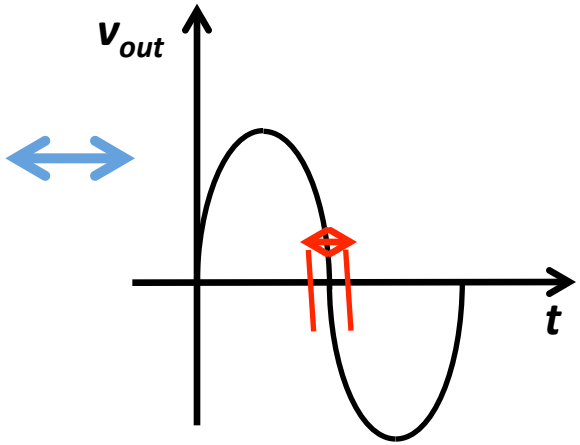


+ Increased amplitude for same bias current.
+ Superior 1/f noise performance.
- Lower maximum amplitude (Diff. peak =V_{DD}).
- f_{osc} limited by pMOS f_T/f_{max}.

Phase Noise – What is it?

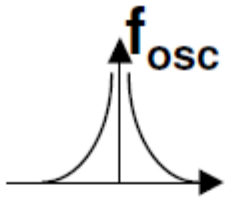






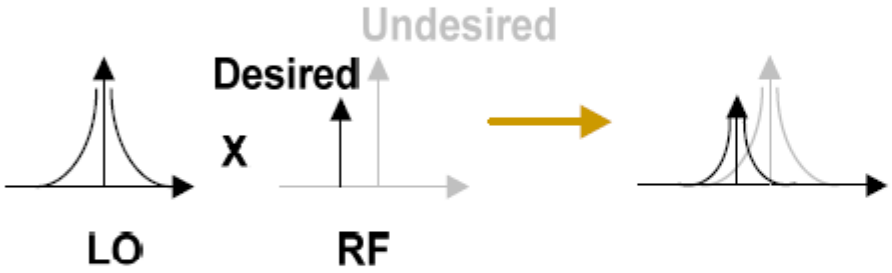
- Real oscillators exhibit phase noise.
  - Spreading of the spectrum in the frequency domain/jitter in the time domain.
- Causes of phase noise:
  - Noise of the active devices.
  - Finite Q of the passive LC resonator.

Phase Noise – Why Important?

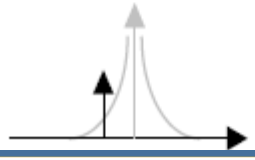


Skirts in freq. domain

Jitter accumulates in time domain



Reciprocal Mixing in RX

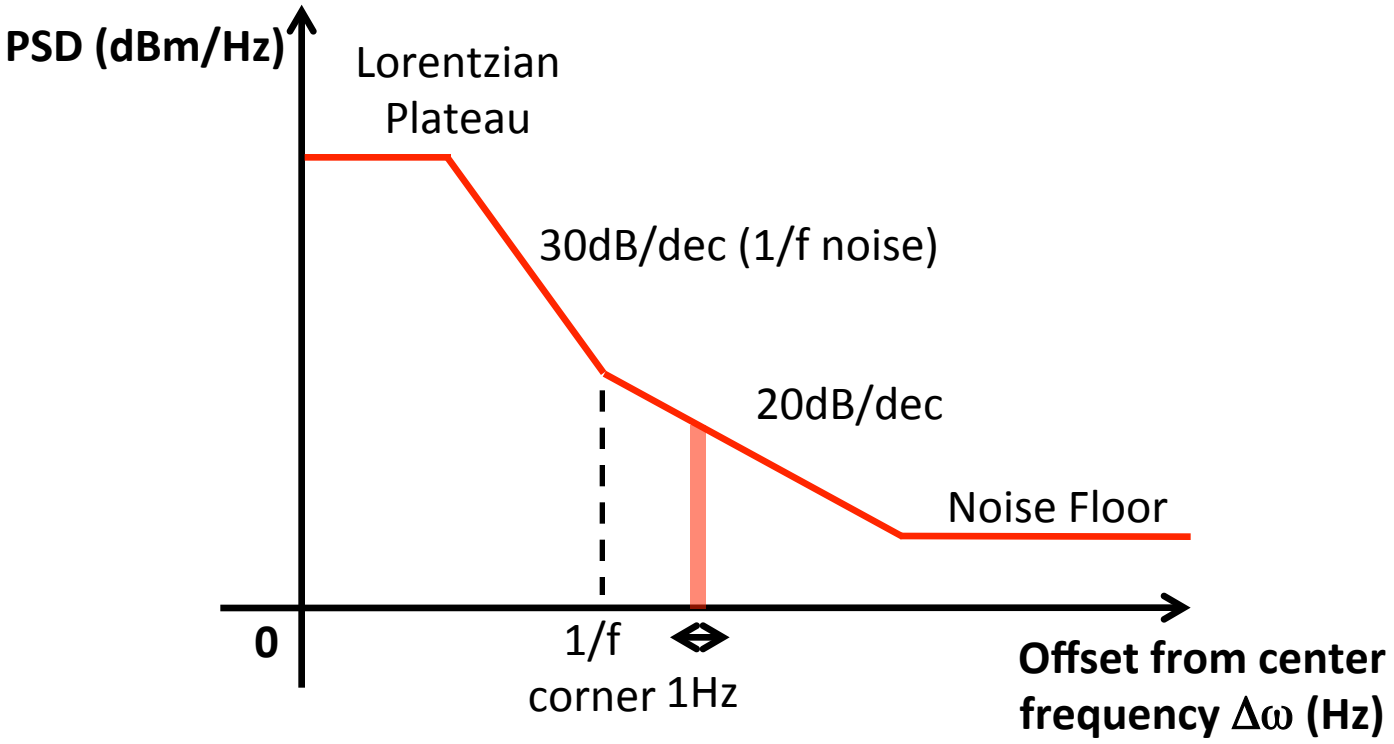


Interference in TX

Recovered Clock

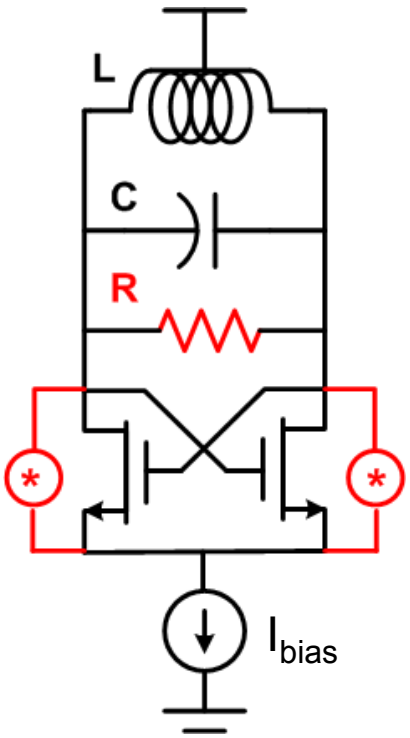
Jitter in CDR

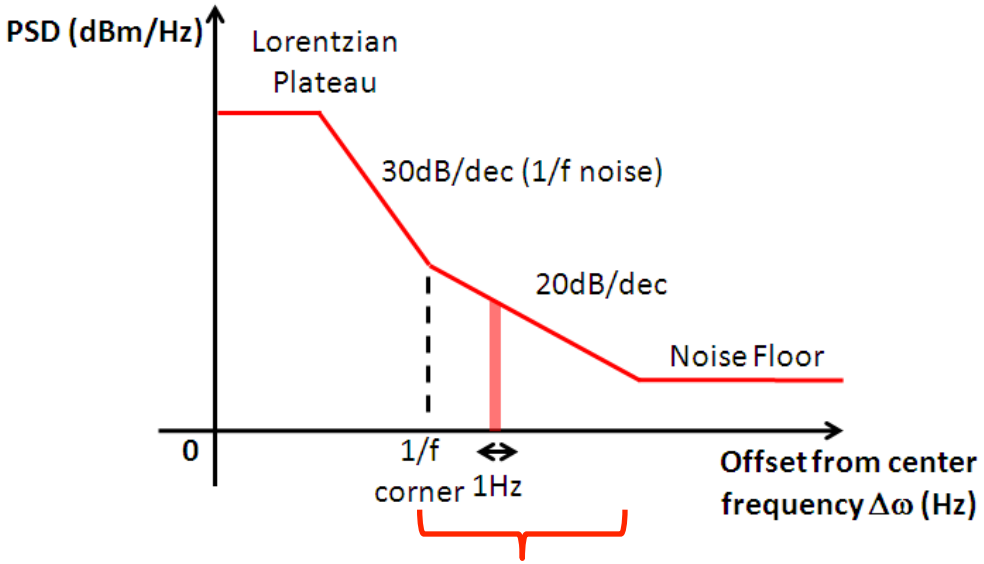
Phase Noise Definition



$$\text{SSB Phase Noise } L(\Delta\omega) = \frac{\text{Power in 1Hz BW at offset } \Delta\omega}{\text{Total Carrier Power}} \text{ in dBc/Hz}$$

Phase Noise in XCOs





$$L(\Delta\omega) = 10\log_{10}\left(\frac{\pi^2 kT\gamma}{4I_{bias}^2 RQ^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right)$$

- Derived using the Hajimiri Linear-Time-Variant phase noise theory.
- Design trade-offs:
  - Q↑: R↑, I_{bias}↓. PN gets linearly better as does P_{dc}!
  - I_{bias}↑, C↑, L↓, R↓: PN gets linearly better at the expense of P_{dc}.

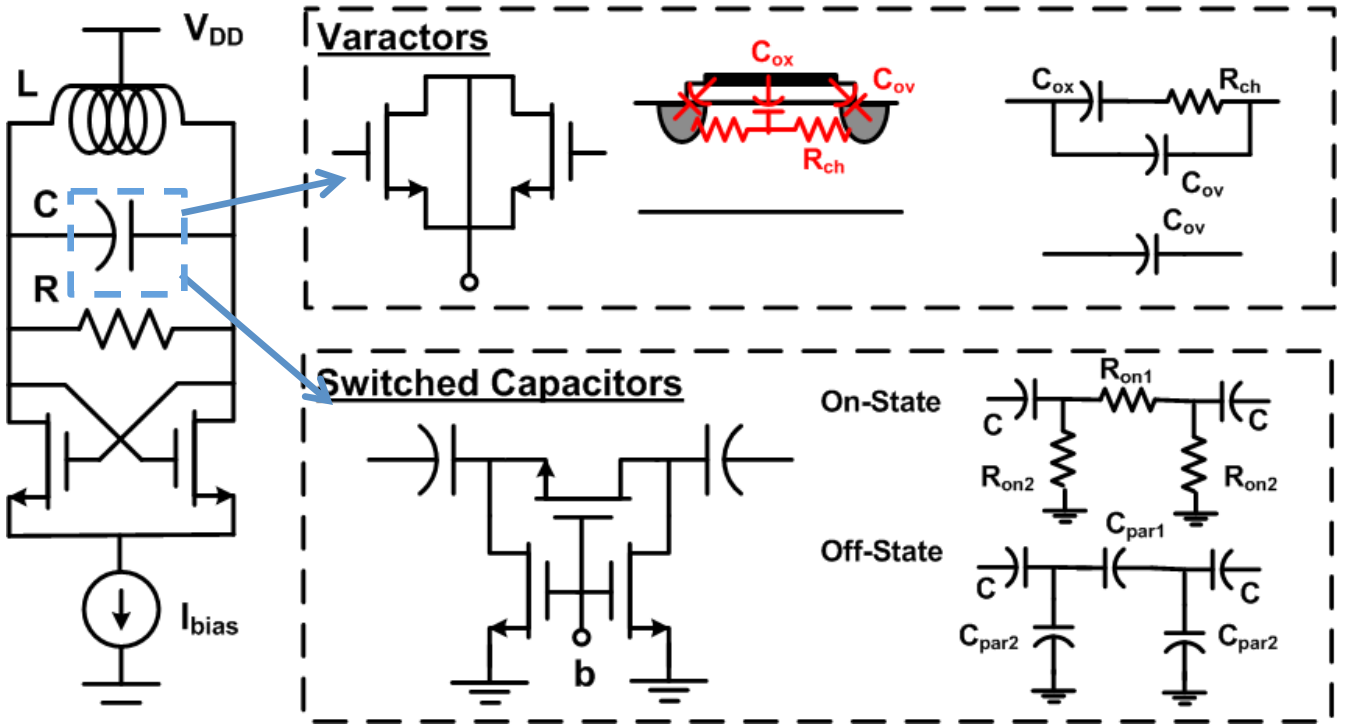
Phase Noise: Additional Reading

- A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," JSSC.
- T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," JSSC.
- D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," JSSC.

More mathematically-formal treatments of phase noise:

- F. Kaertner, "Analysis of white and $f^{-\alpha}$ noise in oscillators," Int. J. Circuits Theory Appl., vol. 18, pp. 485–519, 1990.
- A. Demir, "Analysis and Simulation of Noise in Nonlinear Electronic Circuits and Systems," Ph.D. dissertation, Univ. of California, Berkeley, CA, 1997.

Frequency Tuning



- Q vs tuning-range trade-off is implicit in both tuning mechanisms.
  - Larger varactor L improves C_{ox}/C_{ov} but degrades R_{ch}.
  - Larger switch size improves R_{on} but degrades C_{par}.
- Varactors also introduce AM-to-PM noise conversion.
  - Use switched capacitors for coarse-tuning.

Refs on VCO Tuning

- A. D. Berny et al, "*A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration*," JSSC : discusses Q vs tuning range trade-offs in switched capacitors *and* oscillator amplitude control .
- Changhua Cao et al, "*Millimeter-wave voltage-controlled oscillators in 0.13-µm CMOS technology*," JSSC: discusses varactor design for mmWave VCOs.
- Ka Chun Kwok et al, "*A 23-to-29 GHz Transconductor-Tuned VCO MMIC in 0.13 µm CMOS*," JSSC: discusses a transconductor-based tuning scheme that avoids varactors.

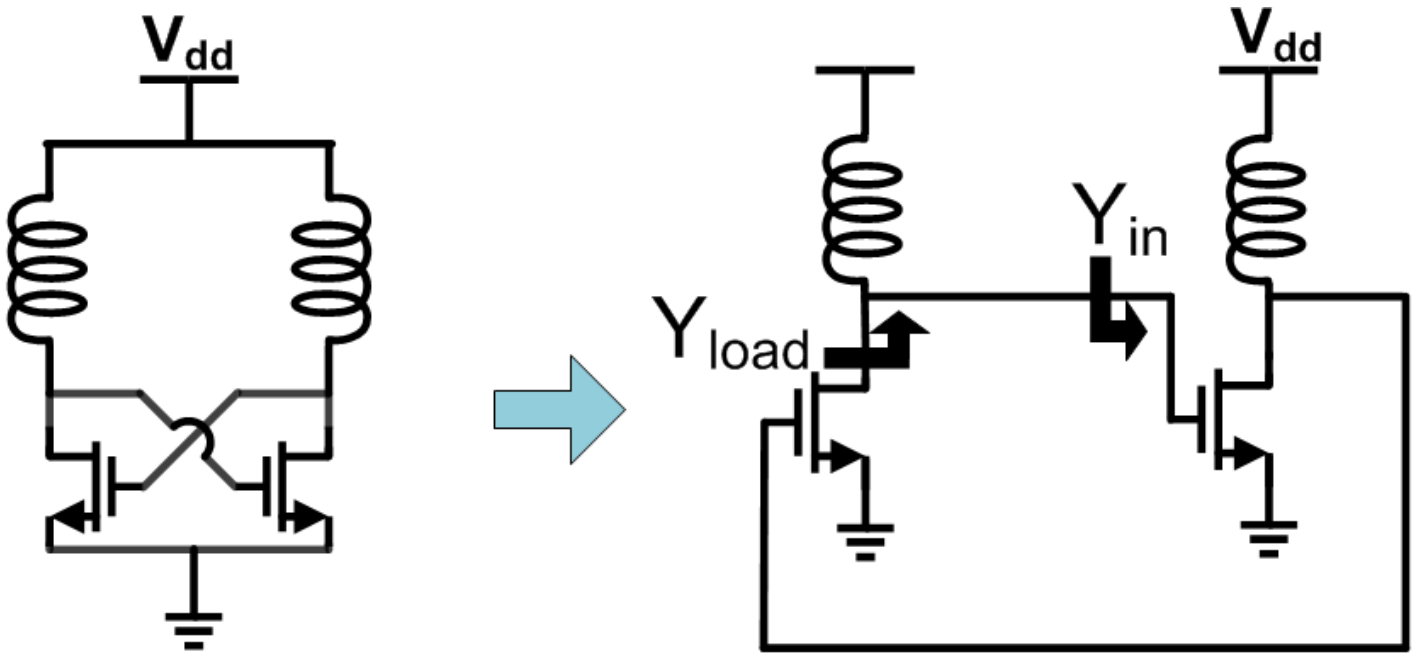
FOM and some SOA VCOs

$$PFTN = 10\log\left[\frac{kT}{P_{DC}}\left(\frac{f_{tune}}{\Delta f}\right)^2\right] - L(\Delta f)$$

Normalizes for DC power and frequency tuning

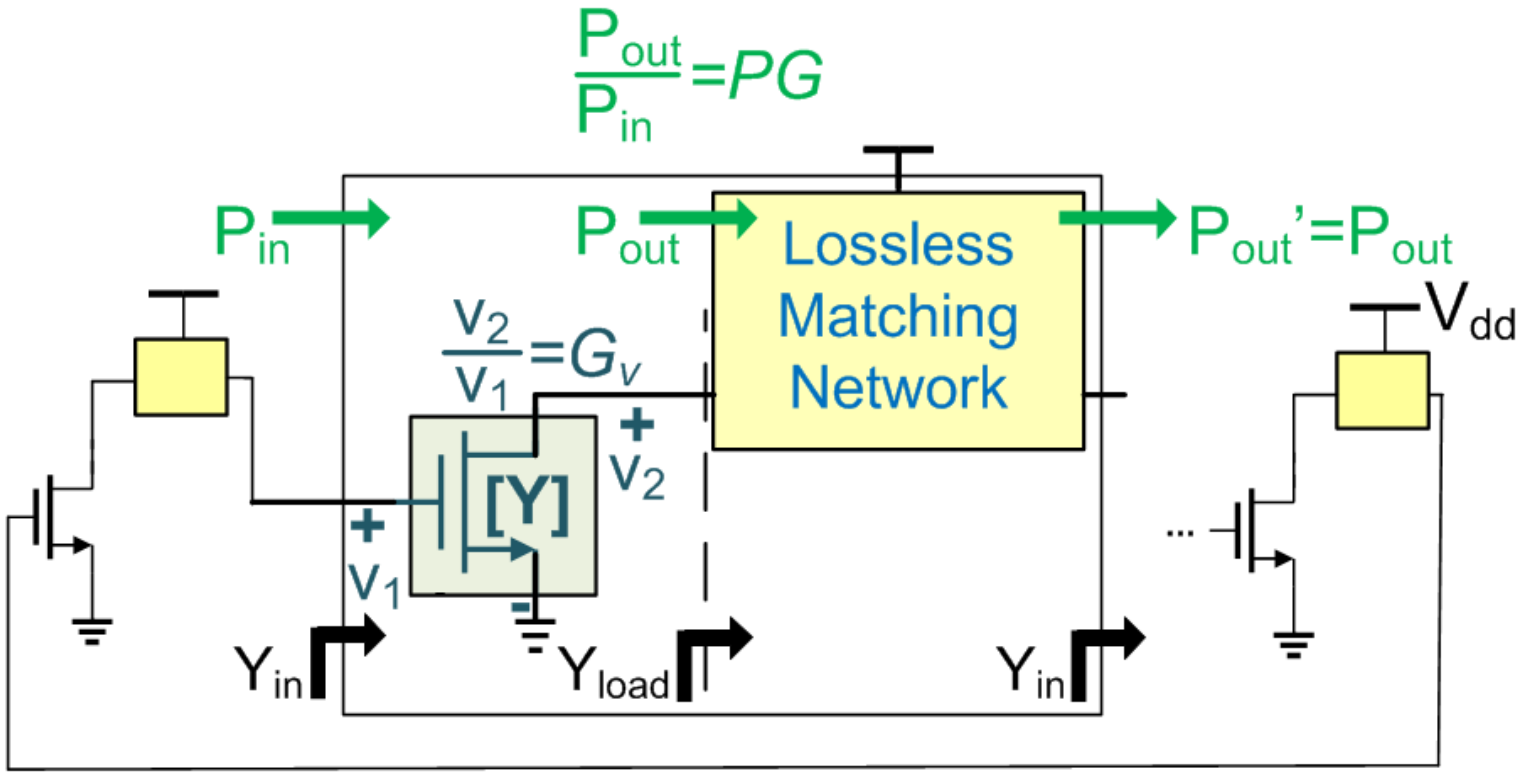
Previous Work	Technology	Topology	Freq. (GHz)	TR (%)	P_{DC}(mW)	Phasenoise (dBc/Hz)	PFTN(dB)
A.Berny JSSC.2005	CMOS 0.18µm	Switched-Cap LC-VCO	1.2~2.4	73	2.6-10	-104.7~-126.5 @600kHz	5.0-8.5
Z.Safarian JSSC.2009	CMOS 0.13µm	Coupled-Inductor LC-VCO	1.3~6	130	4.3-9.1	-112~-120 @1MHz	4-13.5
A.Tanabe JSSC.2011	CMOS 90nm	Variable-Inductor LC-VCO	10~20	67	5.2-7.1	-84~-103 @1MHz	4.2-9
K.Kwok JSSC.2007	CMOS 0.13µm	Transconductor-Tuned VCO	23~29	23.6	43	-92.6~-106.1 @1MHz	2.1-5
N.Fong JSSC.2003	CMOS SOI 0.13µm	Switched-Cap LC-VCO	3~5.6	62	2-3	-114.6~-120.8 @1MHz	3~4.2
D.Hauspie JSSC.2007	CMOS 0.13µm	Active-core Switching LC-VCO	3.1-5.2	48	3.2-9.2	-114.6~-119.0 @1MHz	2.0-3.0

XCO Limitation for High-mmWave



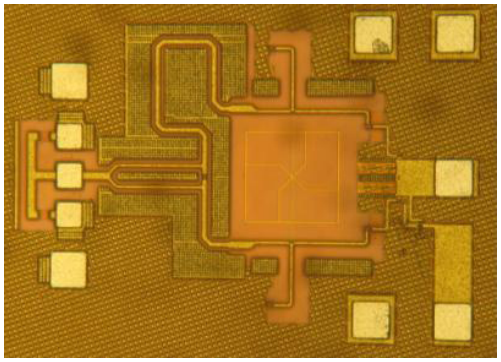
Cross coupled oscillator (XCO) does not maximize the power transfer across an amplifier stage.

Maximum-Gain Ring Oscillator

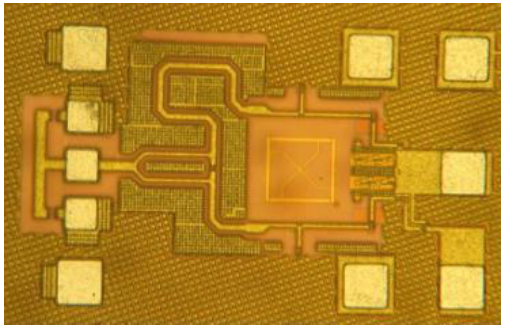


- Conjugate match Y_{load} to maximize power gain across a stage of the ring oscillator.
- Ratio G_v completely defines all quantities in the system (Y_{in}, Y_{load}, and hence, *PG*).

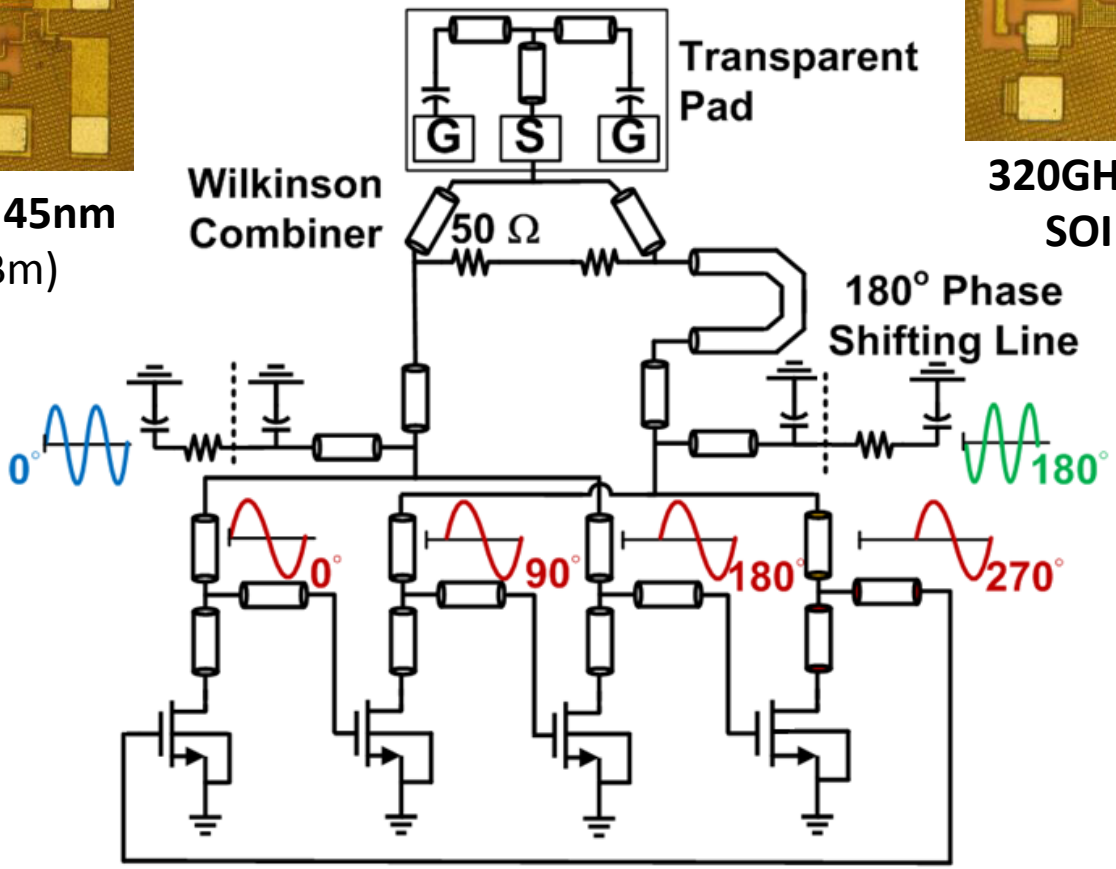
220/320GHz Sources in 45nm SOI*



220GHz source in 45nm SOI (P_{out}=-14dBm)

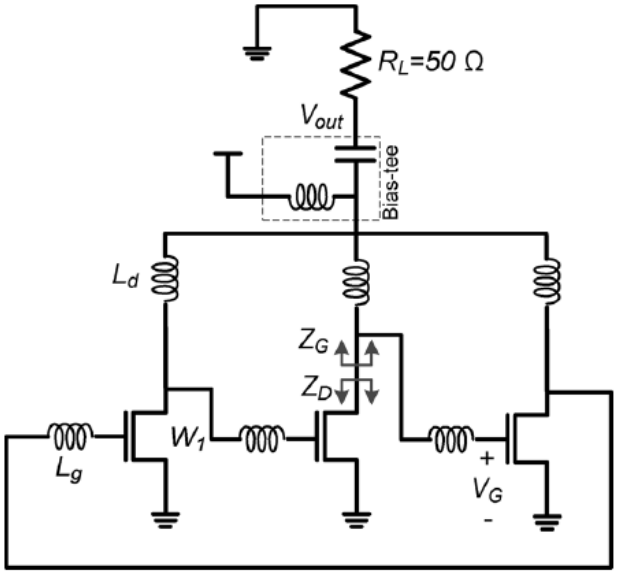


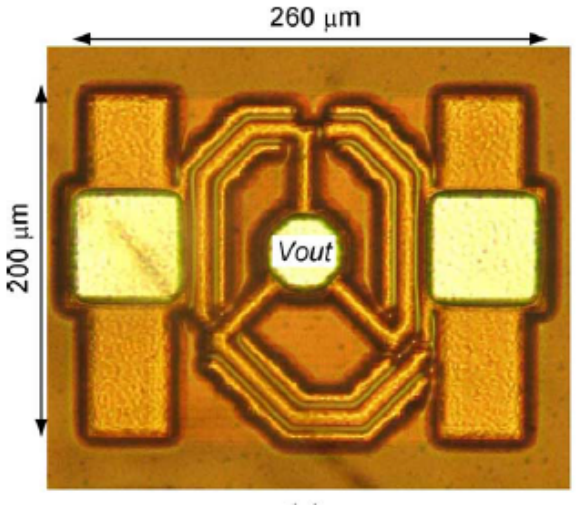
320GHz source in 45nm SOI (P_{out}=-20dBm)

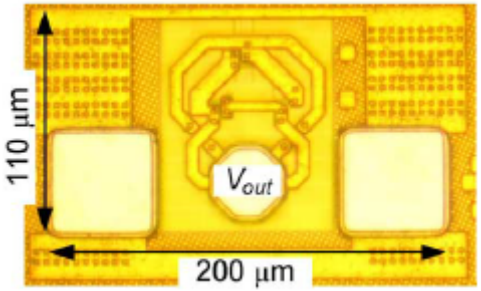


*J. Sharma and H. Krishnaswamy, "216-and 316-GHz 45-nm SOI CMOS Signal Sources Based on a Maximum-Gain Ring Oscillator Topology," T-MTT.

High Power Terahertz Oscillators*



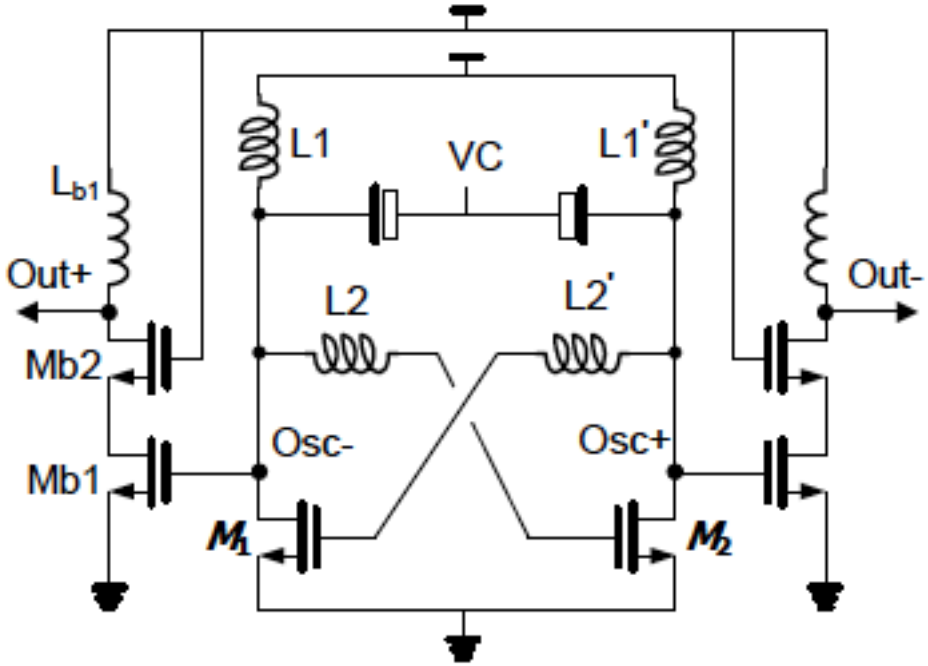


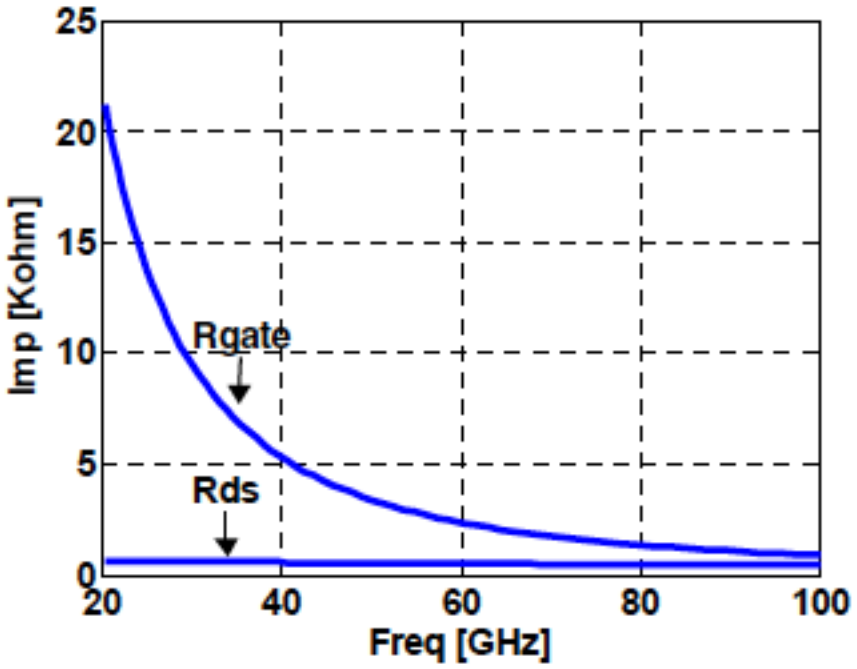


- -7.9dBm of output power has been demonstrated at 482GHz (f_{osc}~160GHz) in 65nm CMOS and -17dBm of output power has been shown at 256GHz (f_{osc}~85GHz) in 130nm CMOS.
- Momeni, O.; Afshari, E., "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," in *IEEE JSSC*, vol.46, no.3, pp.583-597, March 2011

* Figures are the property of the IEEE

Power Matching in LC Oscillators*

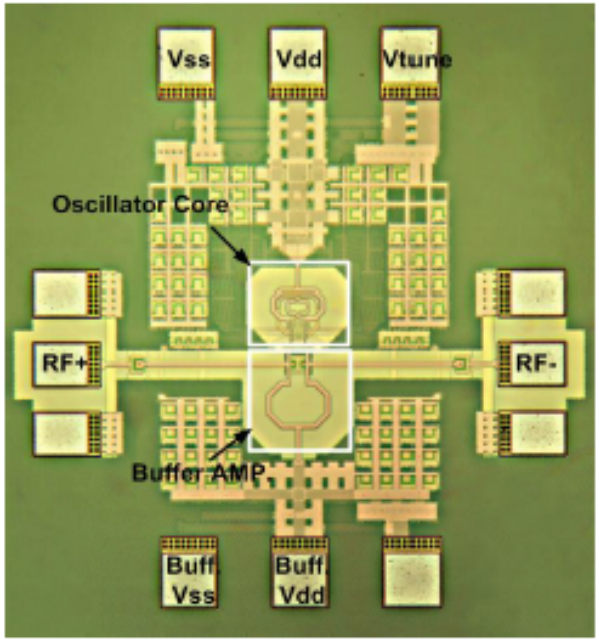


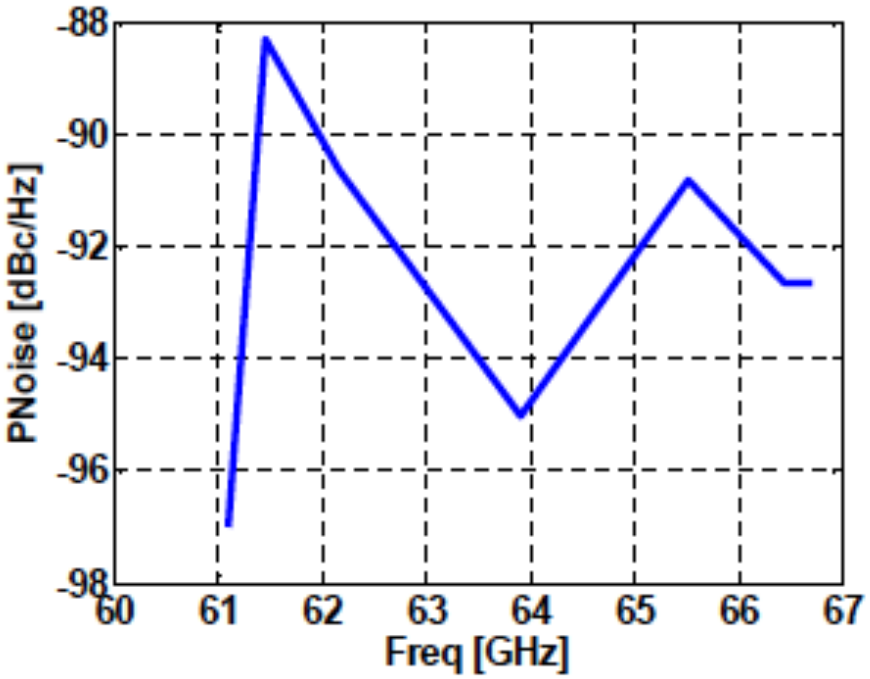


- In general, a cross-coupled VCO can be viewed as two tuned amplifiers in cascade, but with a single inductor used as a matching element between the stages.
- An inductive divider matching network allows power matching between the gate of the following stage and the drain of the previous stage, improving startup gain.

* Figures are the property of the IEEE

Power Matching in LC Oscillators*





- A 60GHz VCO in 90nm CMOS achieves better than -95dBc/Hz at 1MHz offset for an FoM of -186dBc/Hz, indicating phase noise benefits as well.
- Lianming Li; Reynaert, P.; Steyaert, M., "A low power mm-wave oscillator using power matching techniques," in *2009 IEEE RFIC*, pp.469-472, 7-9 June 2009

* Figures are the property of the IEEE

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- Active and Passive Device Modeling
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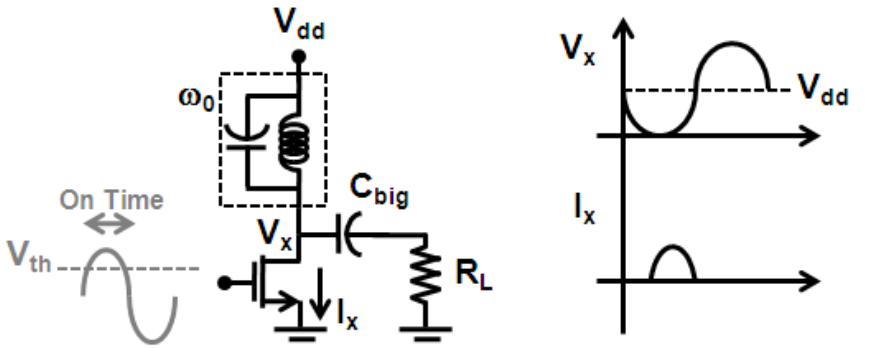
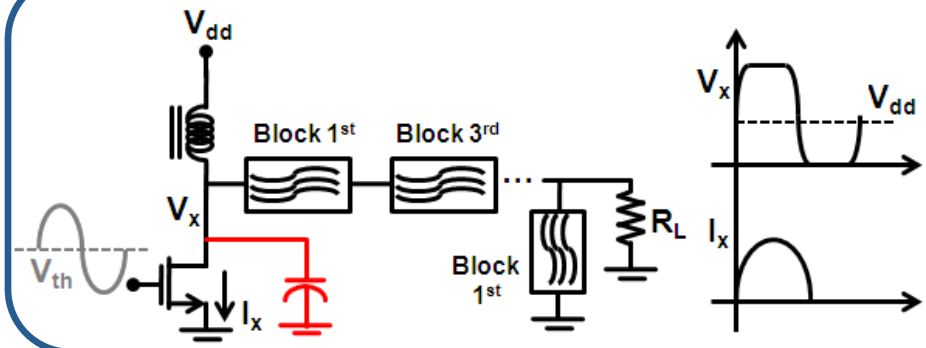
- Multiple-Antenna Systems

PA Overview



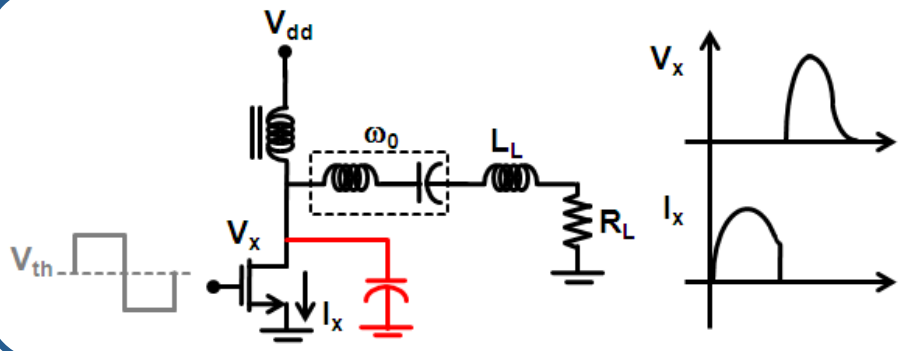
Classes A, AB ,B and C

- Transistor is used as a voltage-dependent current source with varying conduction angle.
- Drain/collector voltage is forced to a sinusoid by the fundamental frequency filter on the output side.
- Maximum drain efficiency ranges from 50% (Class A) – 100% (deep Class C) at the expense of output power for a given peak current.



Class F

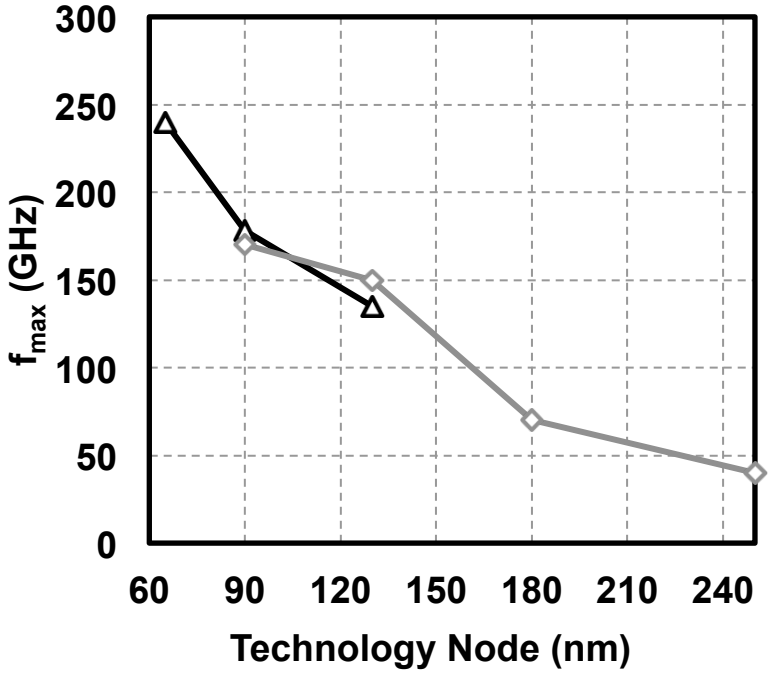
- Harmonic filtering is employed to shape the drain/collector voltage to approach a square wave.
- With enough harmonics, drain efficiency approaches 100%. Output power also increases due to square wave nature of the drain voltage.
- No clear way to incorporate the device's output capacitance in the design.

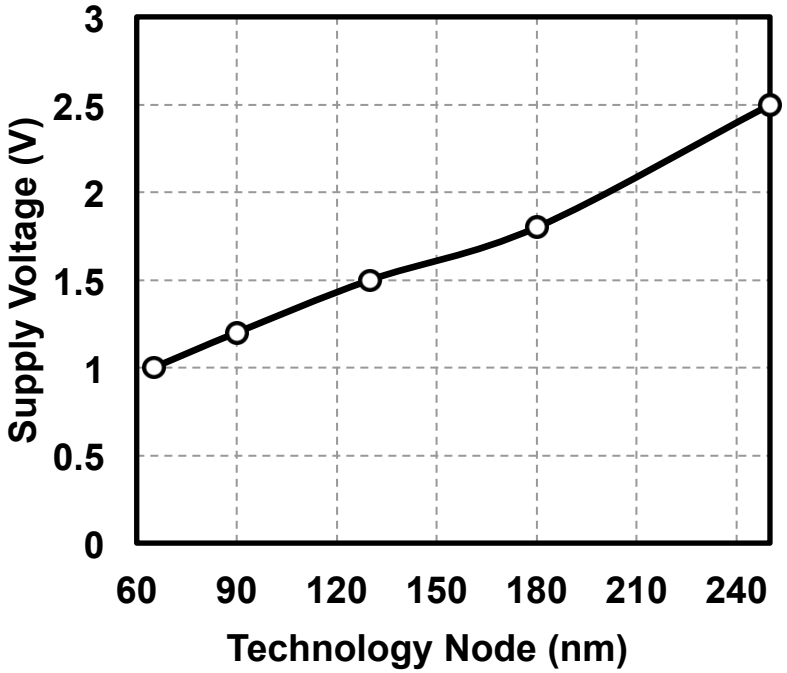


Classes D and E

- Transistor is used as a switch – large device sizes and hard input drive – which enforces no VI power drop across it.
- Class D (not pictured) not feasible at mm-Wave frequencies due to the need for high speed pull-up device.
- Device's output cap. is incorporated into the design and the output network ensures ZVS switching for η_{drain}=100%.
- Requires a linearizing architecture.

CMOS Technology Scaling



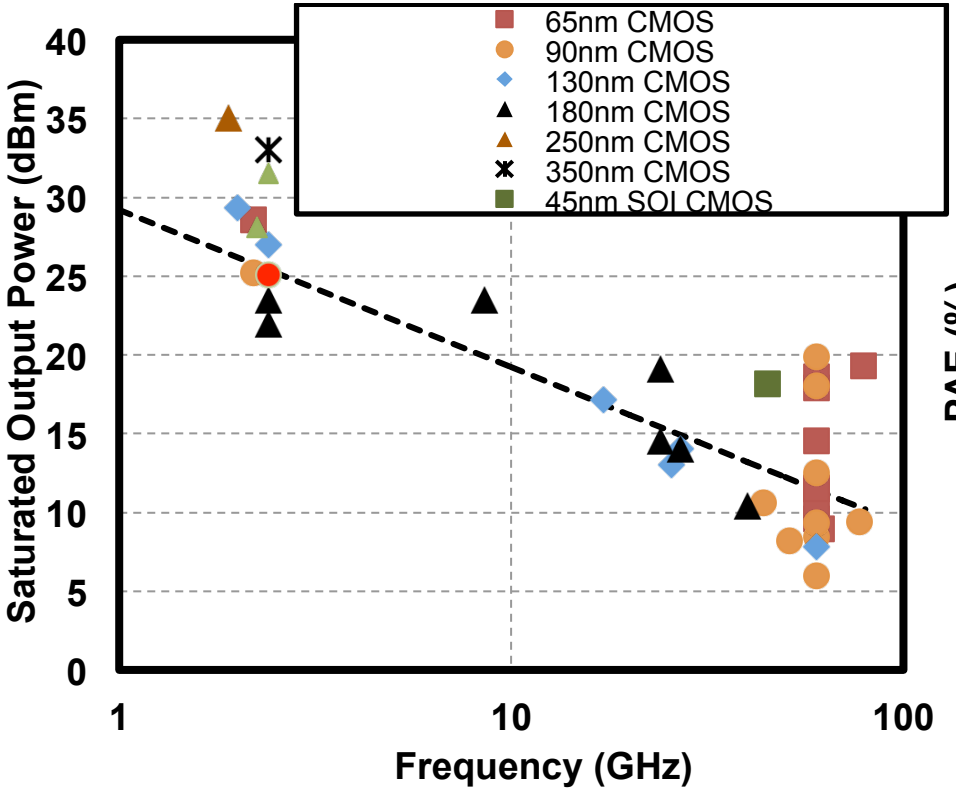


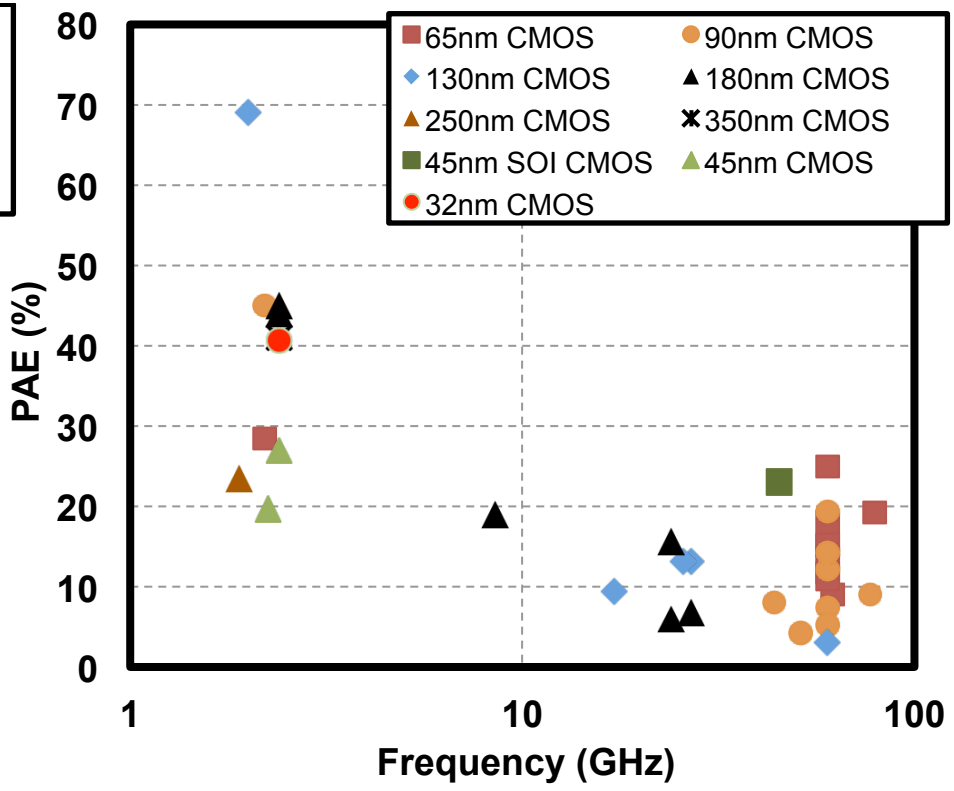
$$f_{\max} V_{DD}^2 \approx 250\ \text{GHz-V}^2$$

Assuming a PA operates at $f_{max}/3$ and drives 50Ω with no transformation

$$P_{out} \approx \frac{250\ \text{GHz-V}^2}{3f} \times \frac{1}{2 \times 50\Omega} \approx \frac{830}{f\,(\text{in GHz})}\ \text{mW}$$

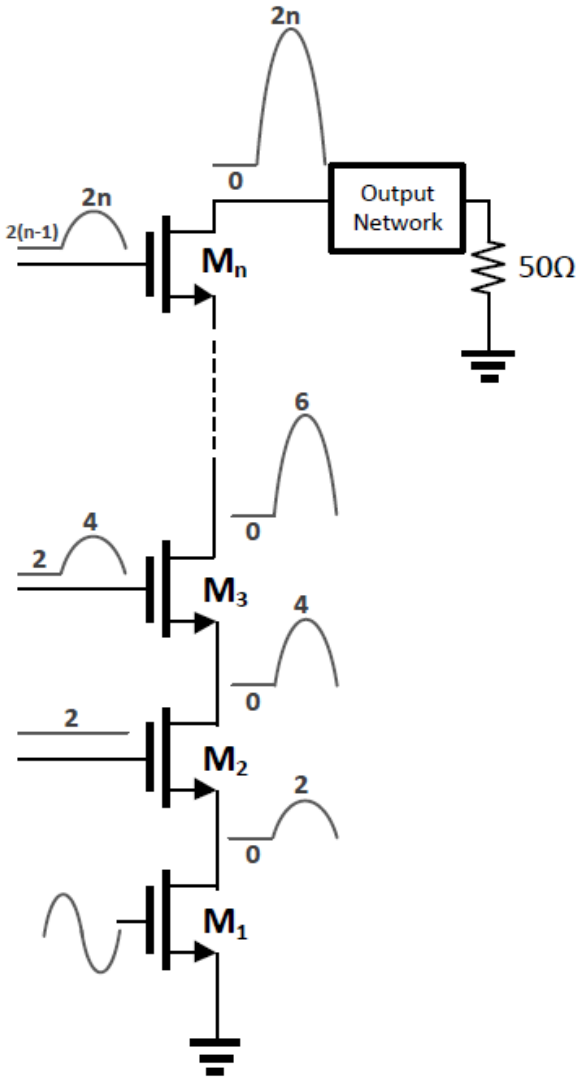
SoA in RF/mmWave CMOS PAs





- Operation at mmWave frequencies requires scaled technologies with low breakdown voltages, limiting the output power.
- Efficiency is limited by active and passive losses, and a reliance on linear, inefficient PA classes due to limited active device gain.

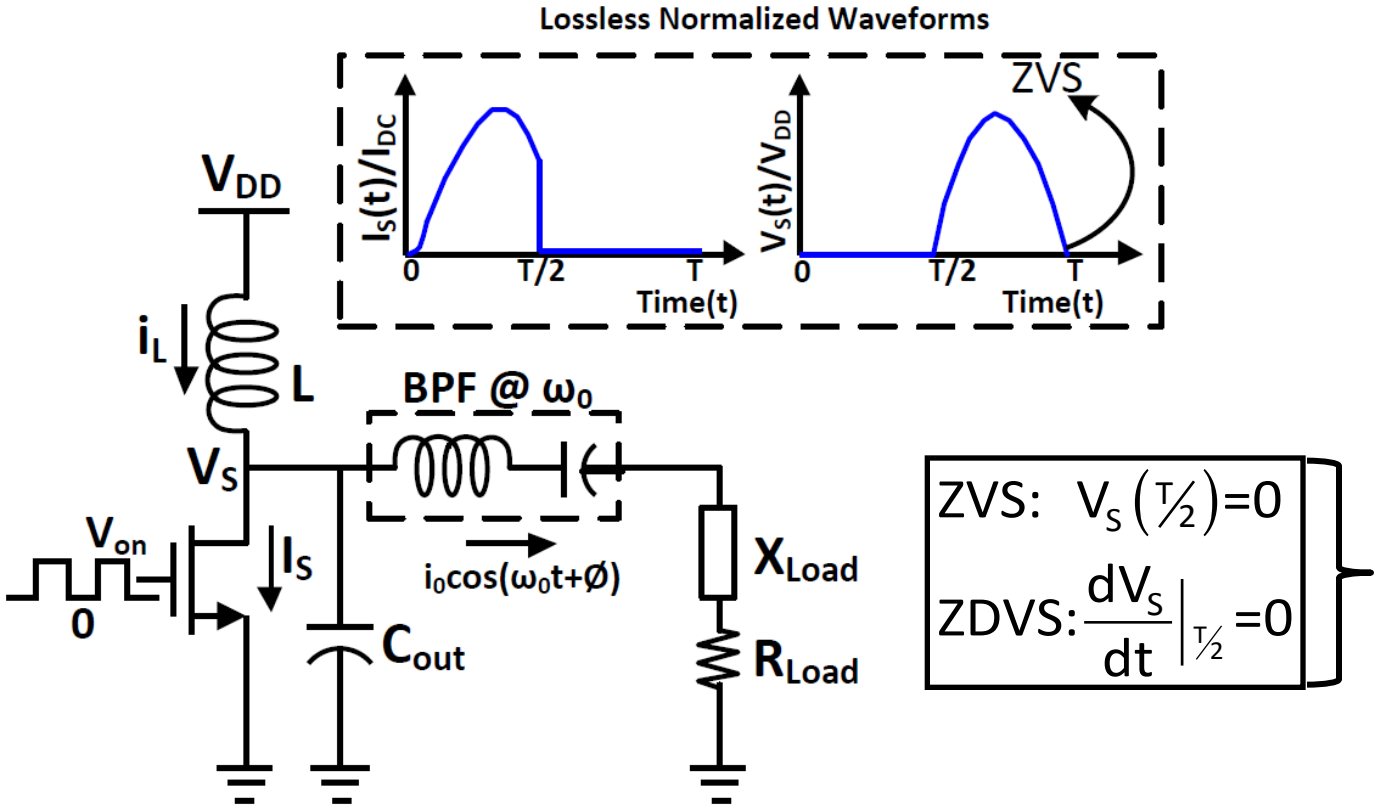
Device Stacking in CMOS PAs



- Stacking increases output swing, eliminates the need for output matching to reach a desired output power level.
- If only the bottom device is driven, gain increases, thereby improving PAE.
- **Does stacking beat the fundamental Johnson Limit trade-off associated with a single CMOS device?**
  - How does the speed of a stacked device (efficiency of a stacked PA) compare to that of a single device?

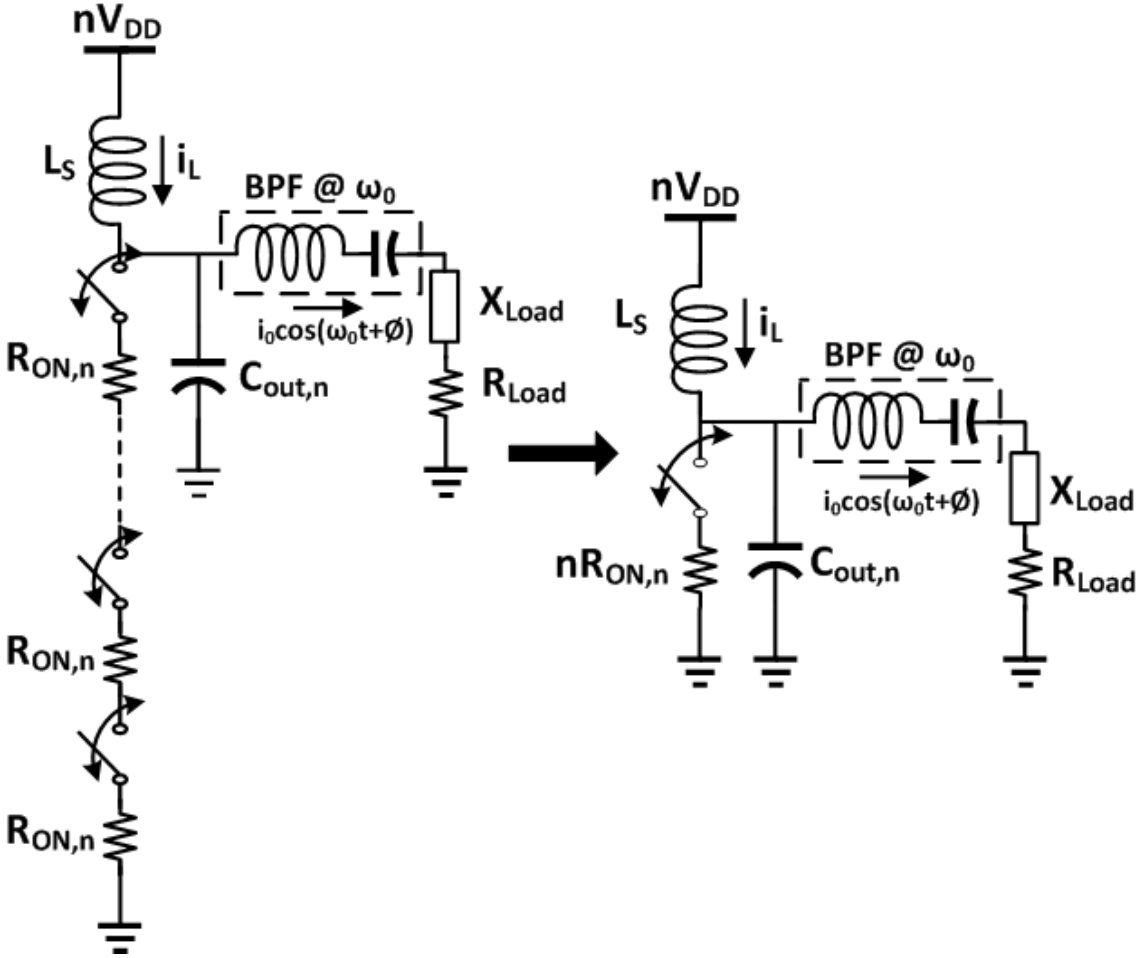
Stacked millimeter-wave nonlinear switching power amplifiers are an open area of research .

Conventional Class-E PA Design



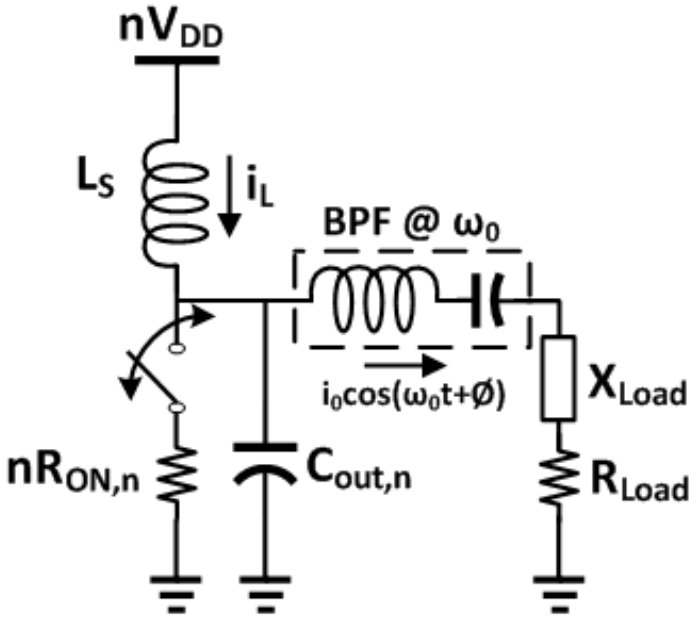
- Conventional Class E design enforces Zero Voltage Switching (ZVS) and Zero-Derivative of Voltage (ZdVS) for ideally 100% efficiency.
- This approach is sub-optimal when the switch and passive components contribute significant loss.

Loss-Aware mmWave Stacked Class-E



The stacked devices are assumed to behave like a single switching device with a linearly larger R_{on} and V_{dd}.

Loss-Aware mmWave Stacked Class-E



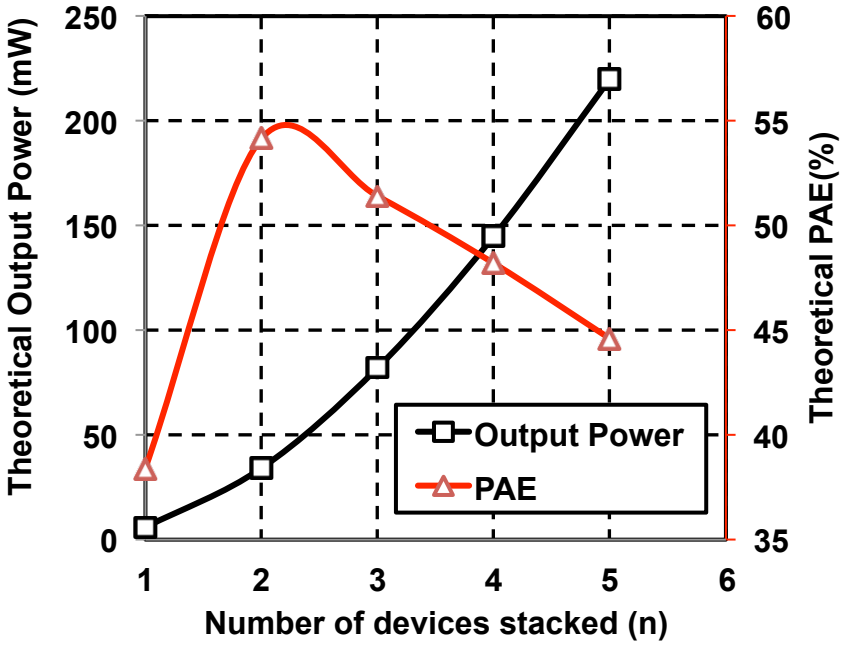
HIGHLIGHTS OF ANALYTICAL FORMULATION*

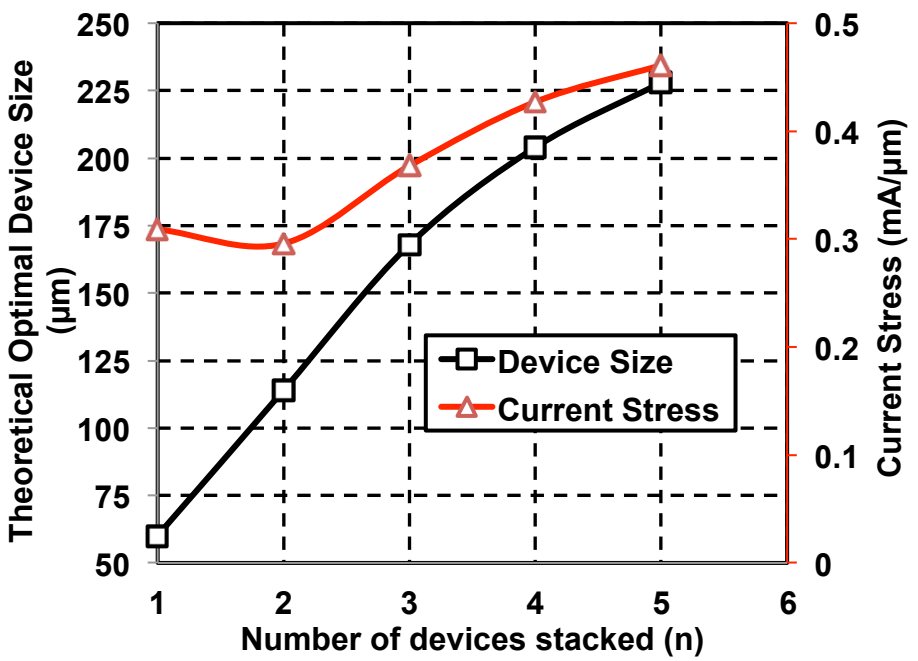
- Takes finite choke inductance (L_s) into account.
- Takes the effect of switch R_{ON} into account formally (but assumes $R_{ON} << 1/\omega C_{out}$).
- Takes into account passive loss.
- Takes into account input drive power.
- Load impedance is not chosen for Class E switching conditions (ZVS/ZdVS) but rather are varied to optimize PAE.
- Analytical equivalent to load-pull simulations.
- Provides a starting point for design optimization.

Loss-Aware mmWave stacked Class-E design methodology formally takes into account several mmWave non-idealities.

*Anandaroop Chakrabarti and Harish Krishnaswamy, "An Improved Analysis and Design Methodology for RF Class-E Power Amplifiers with Finite DC-feed Inductance and Switch On-Resistance," *ISCAS 2012*.

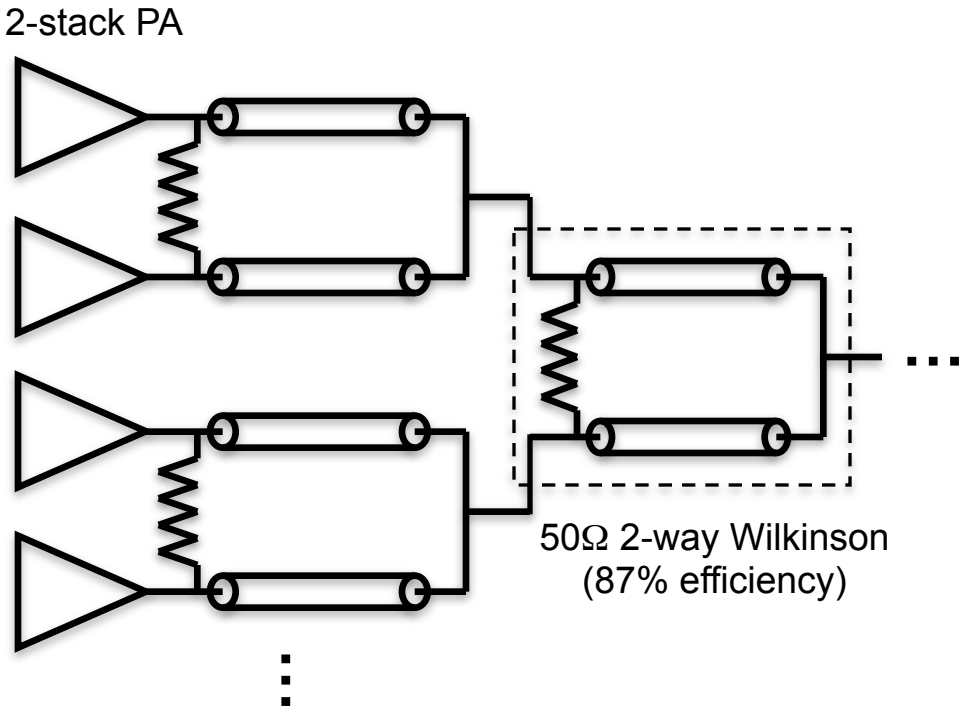
45GHz Stacking Roadmap in 45nm SOI

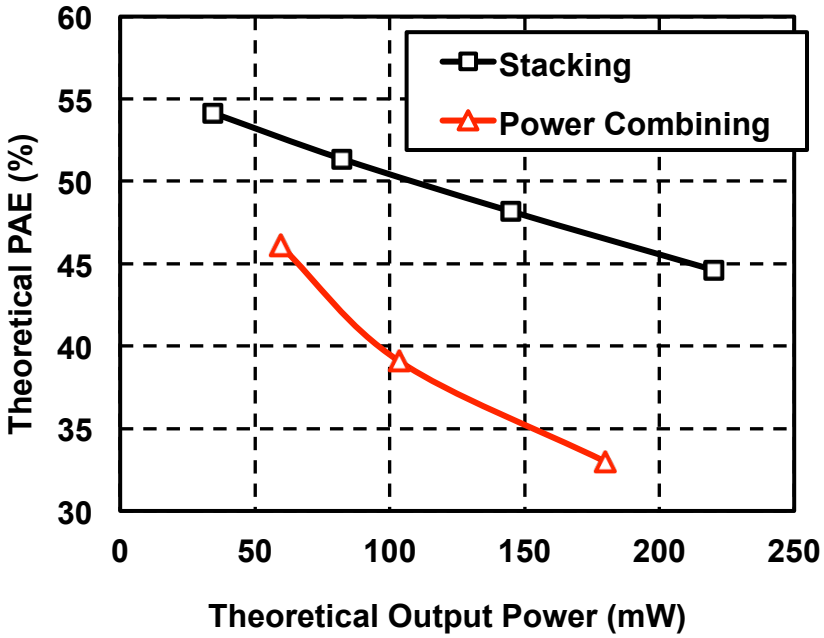




- Load impedance is constrained to 50Ω to avoid impedance transformation.
- This analysis represents the *technology-driven fundamental limits* on the output power and PAE that can be achieved using Class-E PAs at mmWave frequencies.
- Optimal device size increases, requiring careful, low-loss device layouts.
- Current stress also increases with stacking, setting an upper limit.

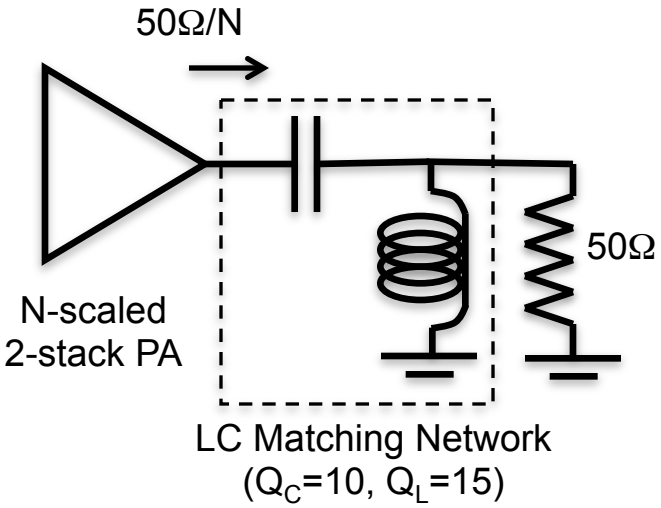
Stacking versus Power Combining

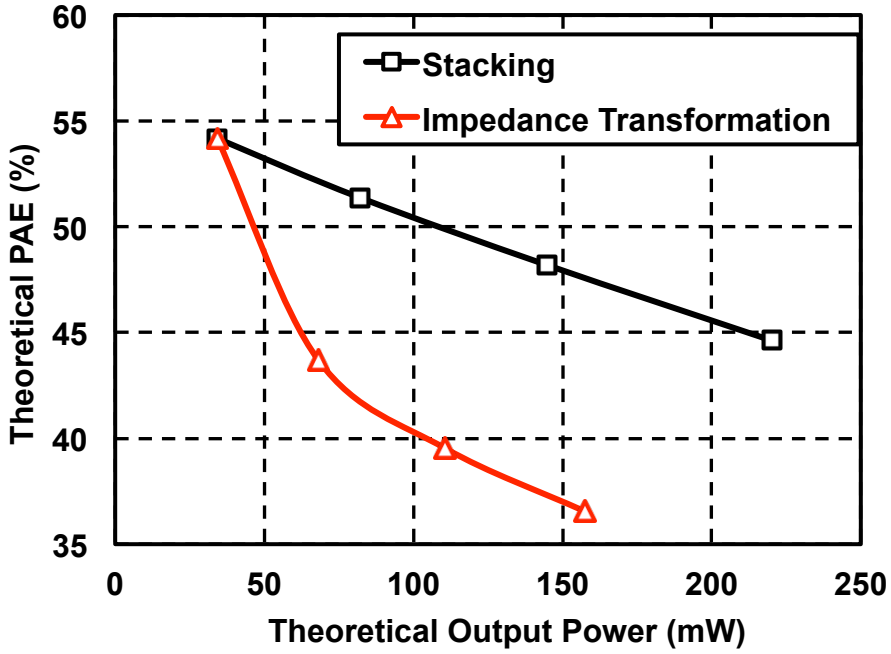




- Series stacking is compared with the power combining of multiple 2-stack Class-E-like PAs using a Wilkinson tree.
- Series stacking enables significantly higher efficiency for the same output power level.

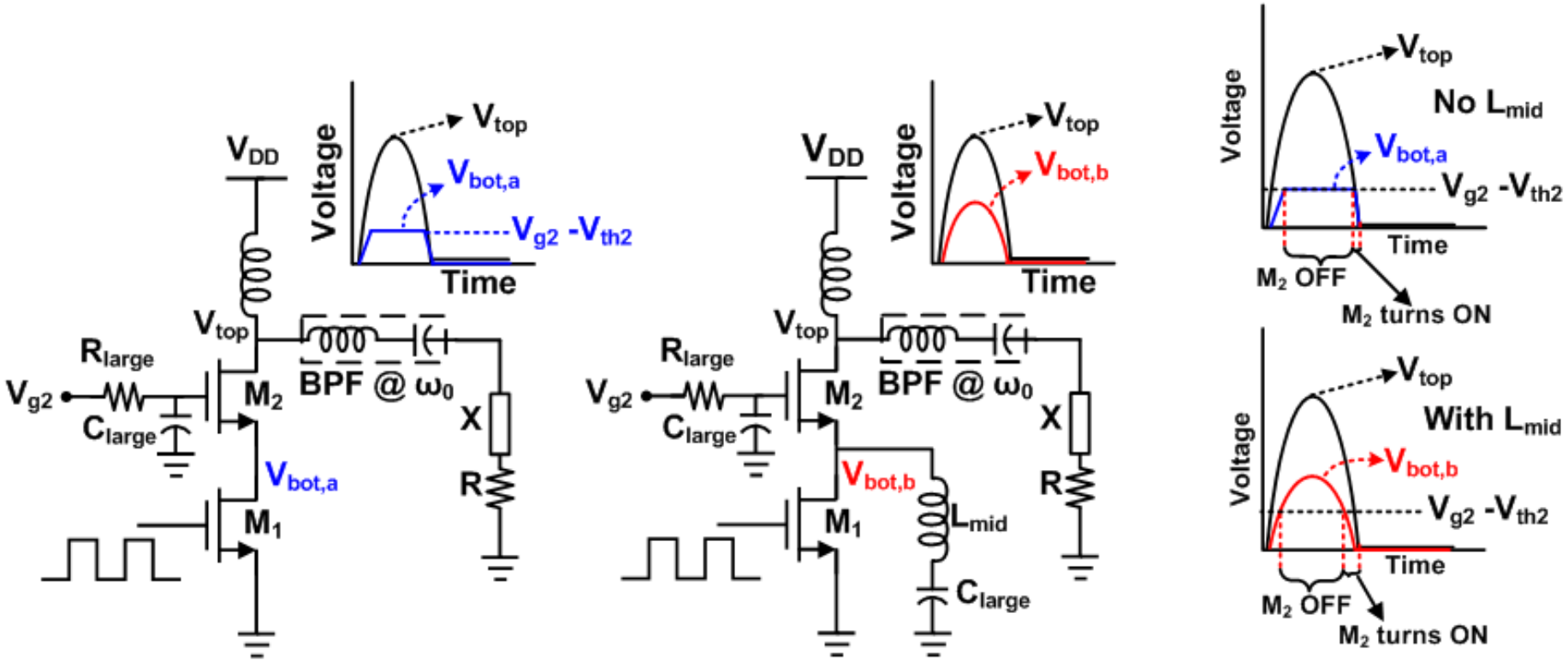
Stacking vs. Impedance Transform





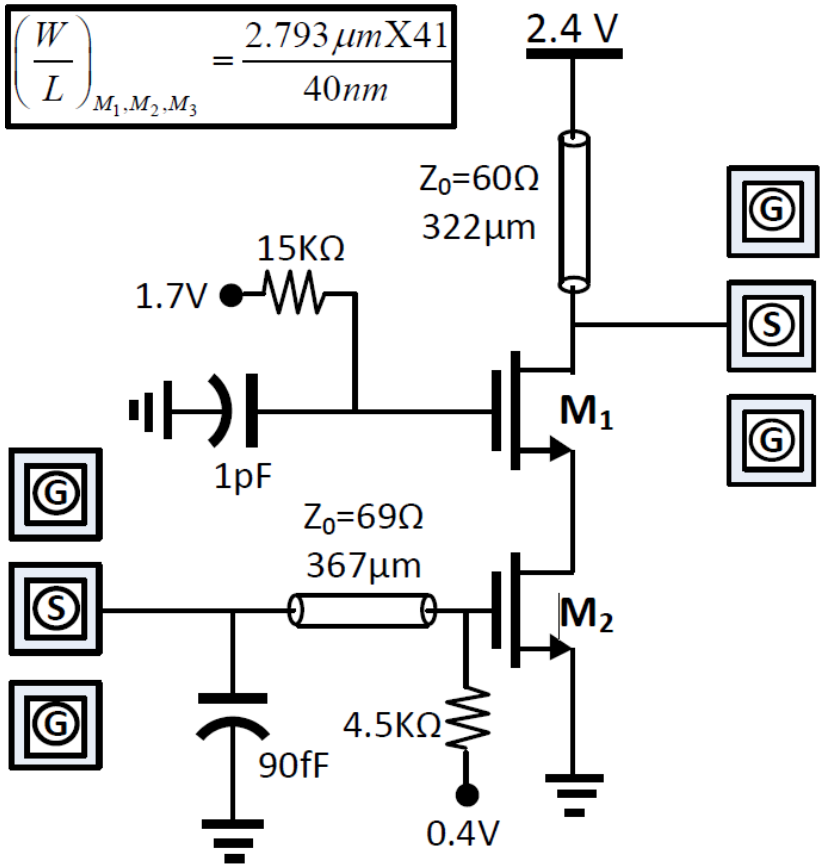
- Series stacking is compared with the use of LC impedance transformers in conjunction with scaled 2-stack Class-E-like PAs.
- Series stacking enables significantly higher efficiency for the same output power level.

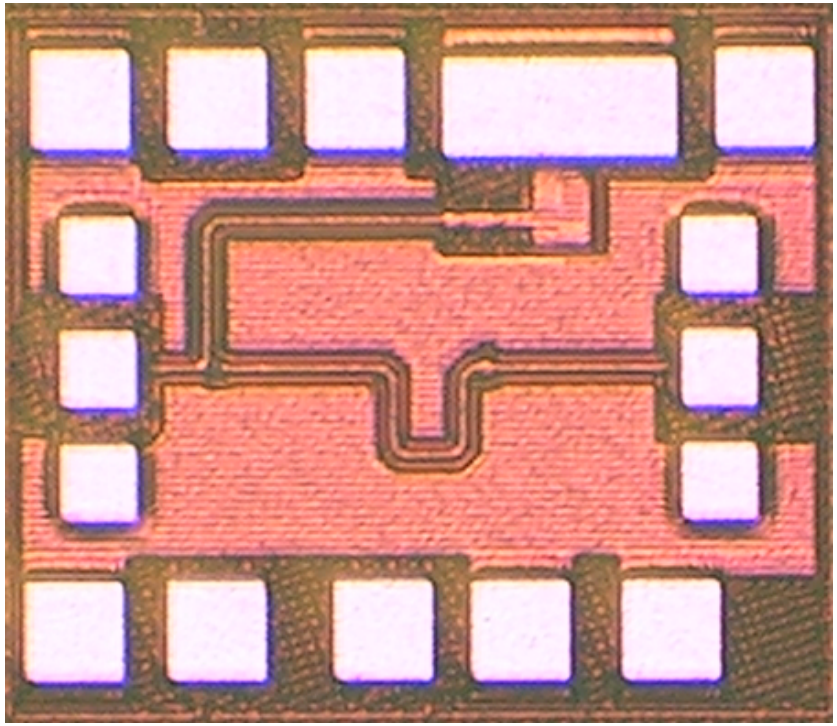
Intermediary Node Inductive Tuning



- Inductive tuning promotes Class-E-like swings at the intermediary node but creates a trade-off with loss, as the stacked device turns on early during the OFF cycle.

2-stacked 45nm SOI Class E PA



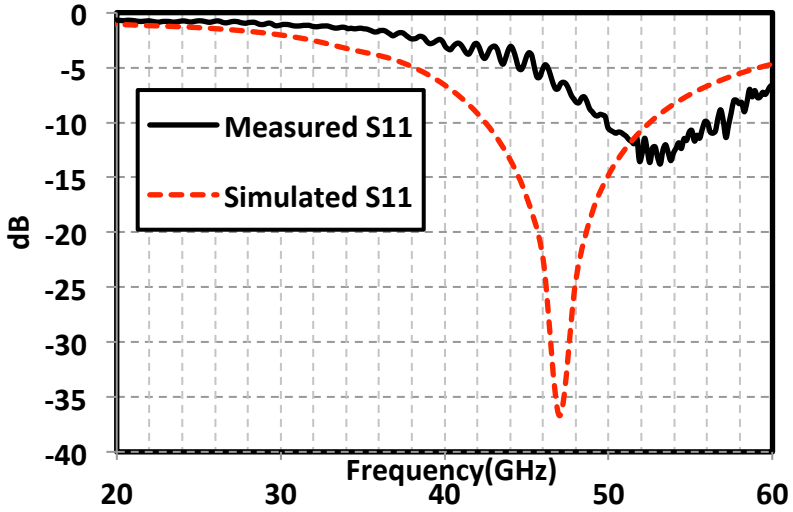


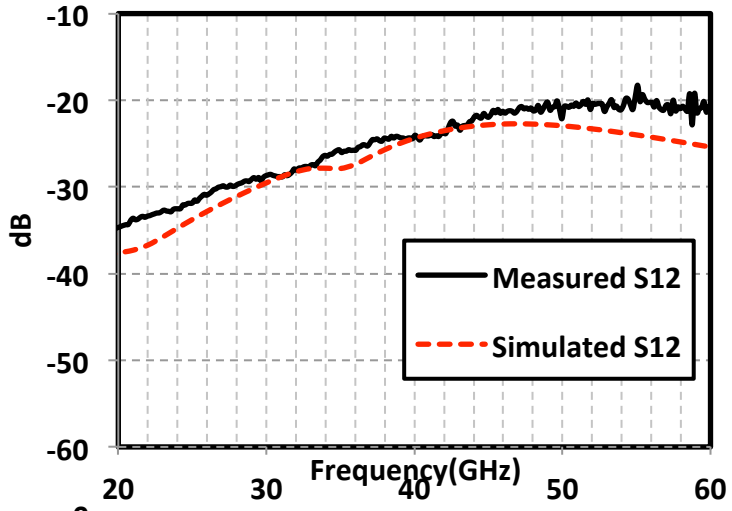
Single-Ended 2-stacked Class E PA designed based on the Loss-Aware Millimeter-Wave Stacked-Class-E design methodology.

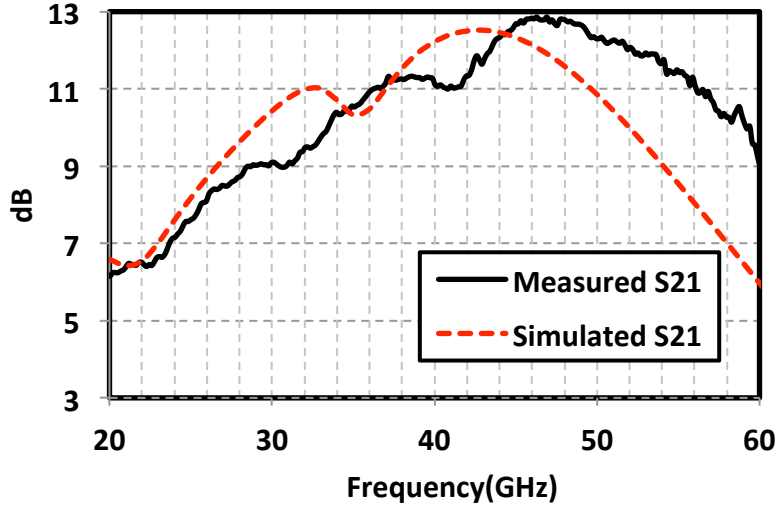
Anandaroop Chakrabarti and Harish Krishnaswamy, "High Power, High Efficiency Stacked mmWave Class-E-like Power Amplifiers in 45nm SOI CMOS," *2012 IEEE CICC*.

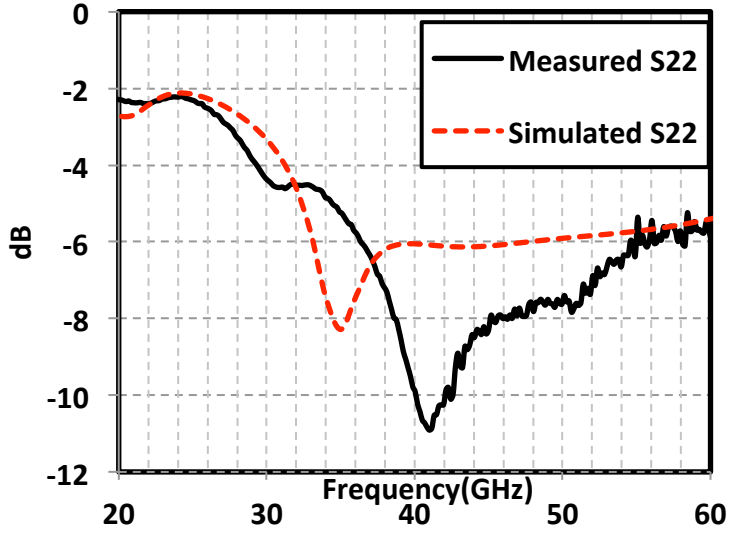
2-stack Class E PA S parameters

$V_{g,bot}$ = 0.4 V, $V_{g,top}$ = 1.4 V, V_{DD} = 2.4 V

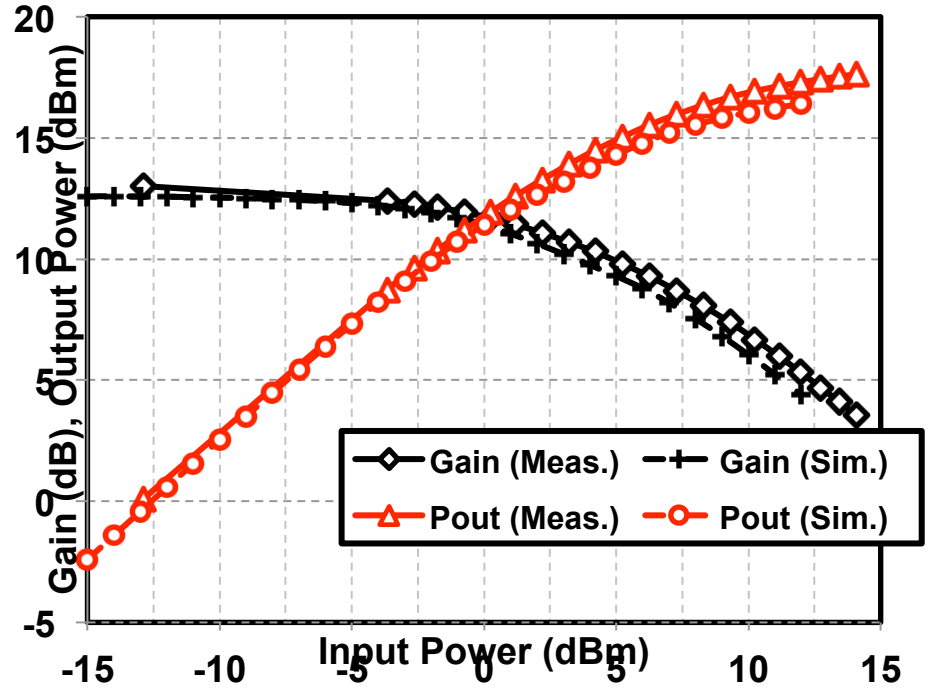


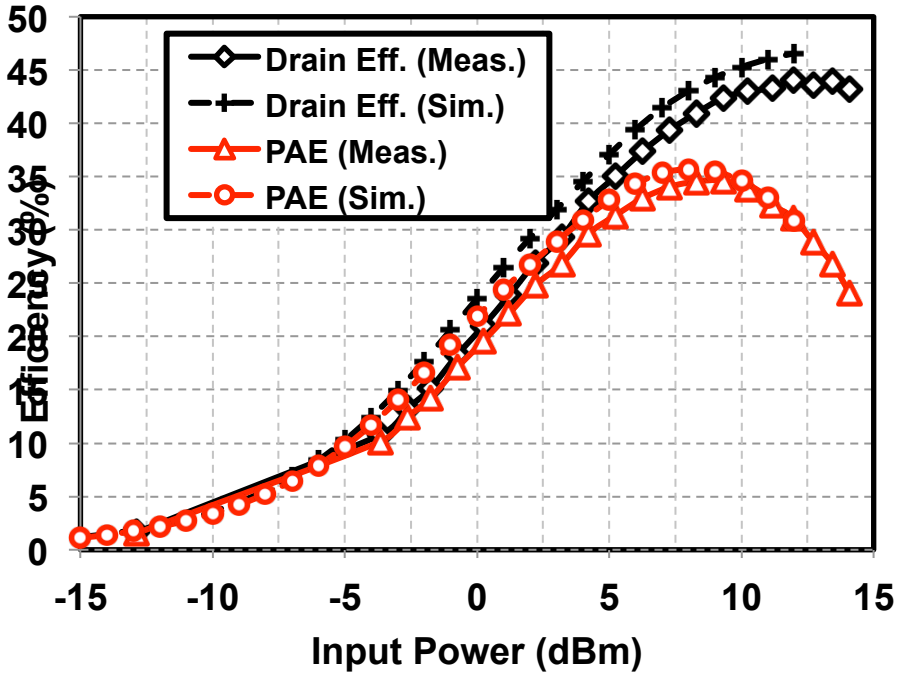






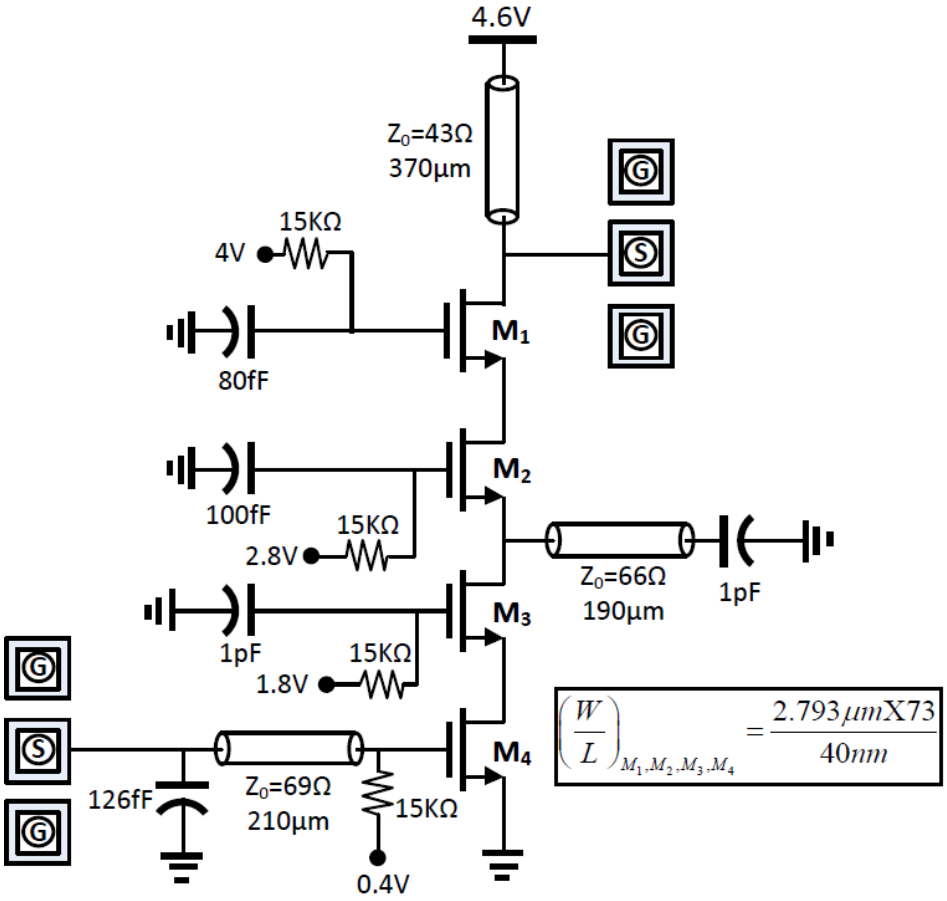
2-stack Large-Signal @ 47GHz

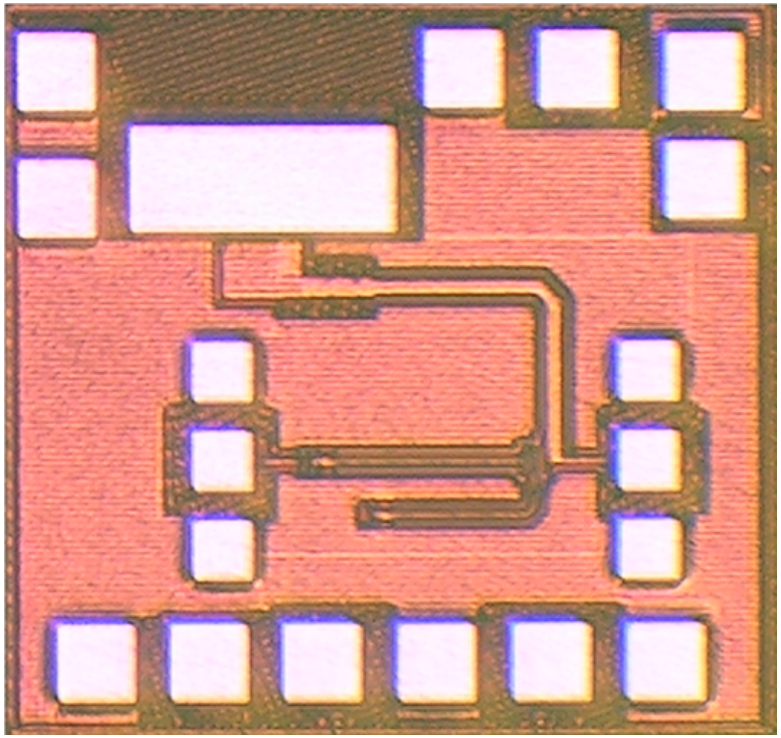




Performance Metric	Simulated Performance	Measured Performance
Center Frequency	45 GHz	47 GHz
Sat. Output Power	16.4 dBm	17.6 dBm
Power Gain	12.6 dB	13 dB
Drain Efficiency (η)	43 %	42.4 %
PAE_{MAX}	35.7 %	34.6 %

4-stacked 45nm SOI Class E PA

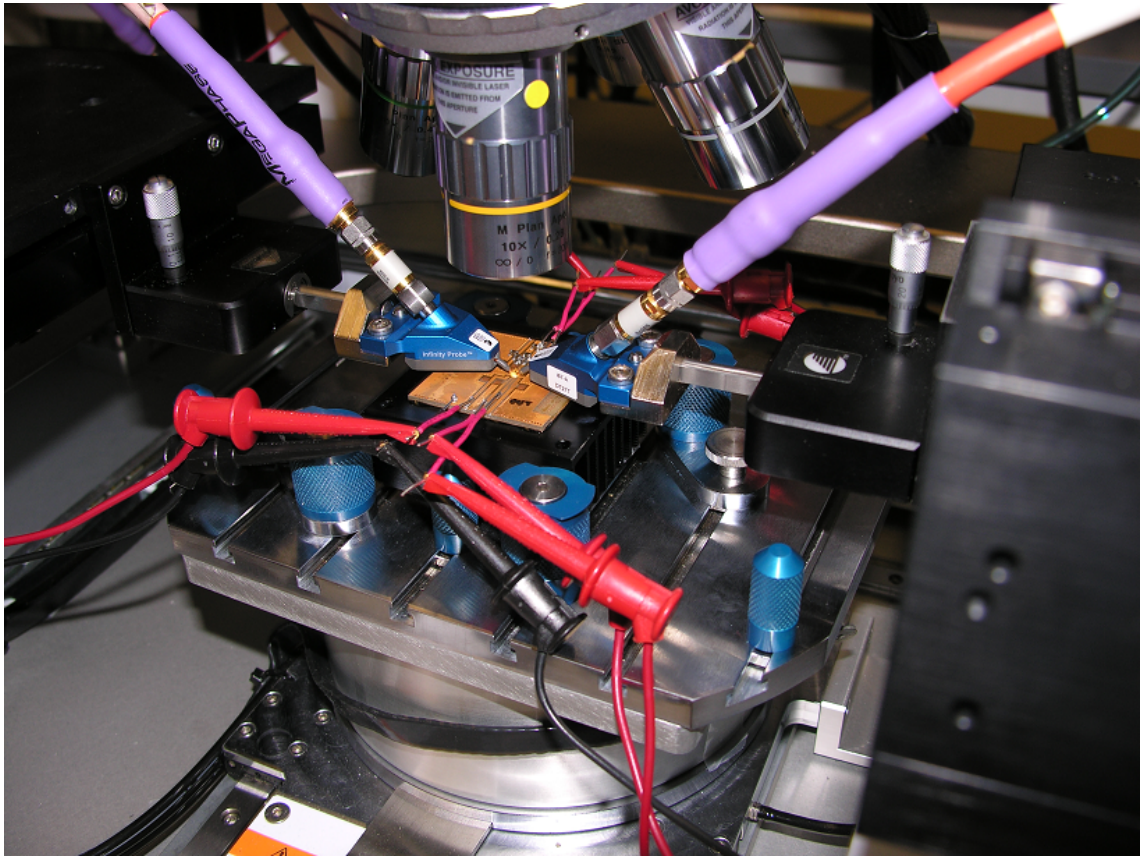




Single-Ended 4-stacked Class E PA designed based on the Loss-Aware Millimeter-Wave Stacked-Class-E design methodology.

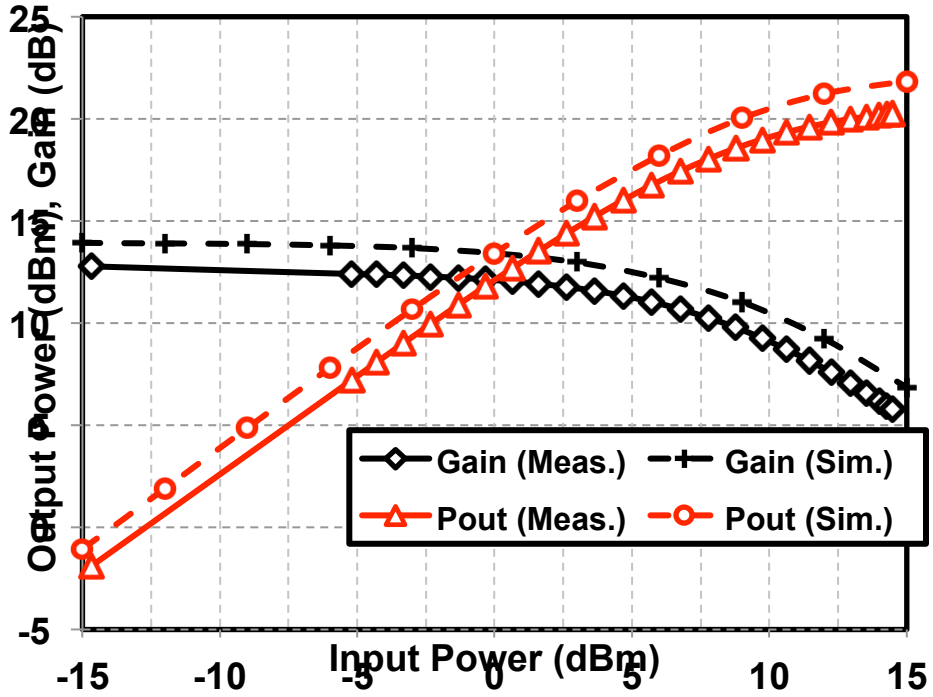
Anandaroop Chakrabarti and Harish Krishnaswamy, "High Power, High Efficiency Stacked mmWave Class-E-like Power Amplifiers in 45nm SOI CMOS," *2012 IEEE CICC*.

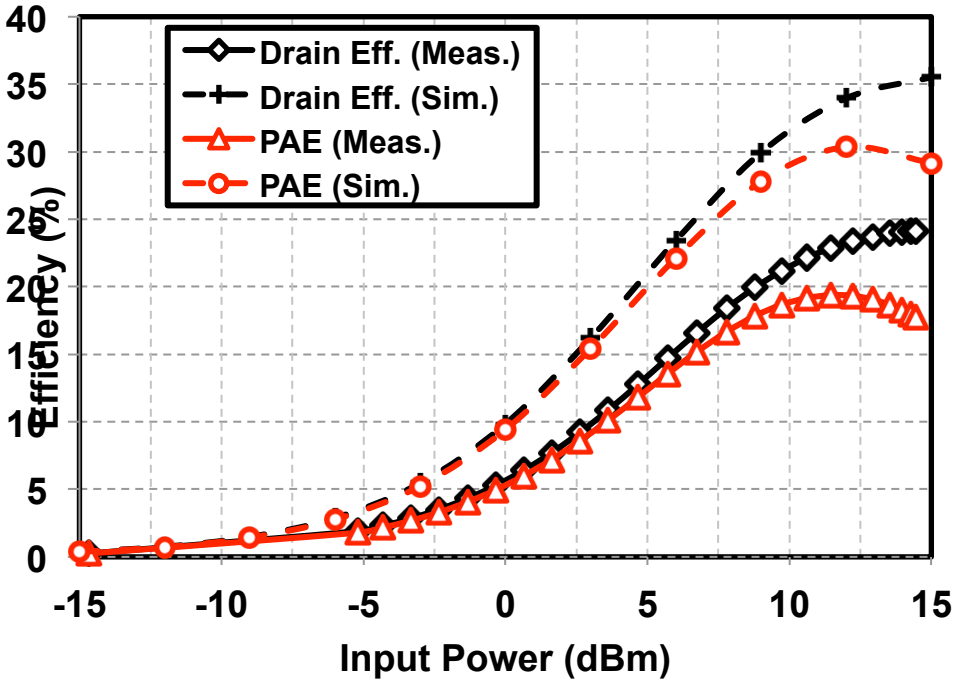
Measurement Setup



PA is mounted on a PCB, which is mounted on a heat sink with thermally-conductive heat-sink compound. A fan is used for forced-air cooling.

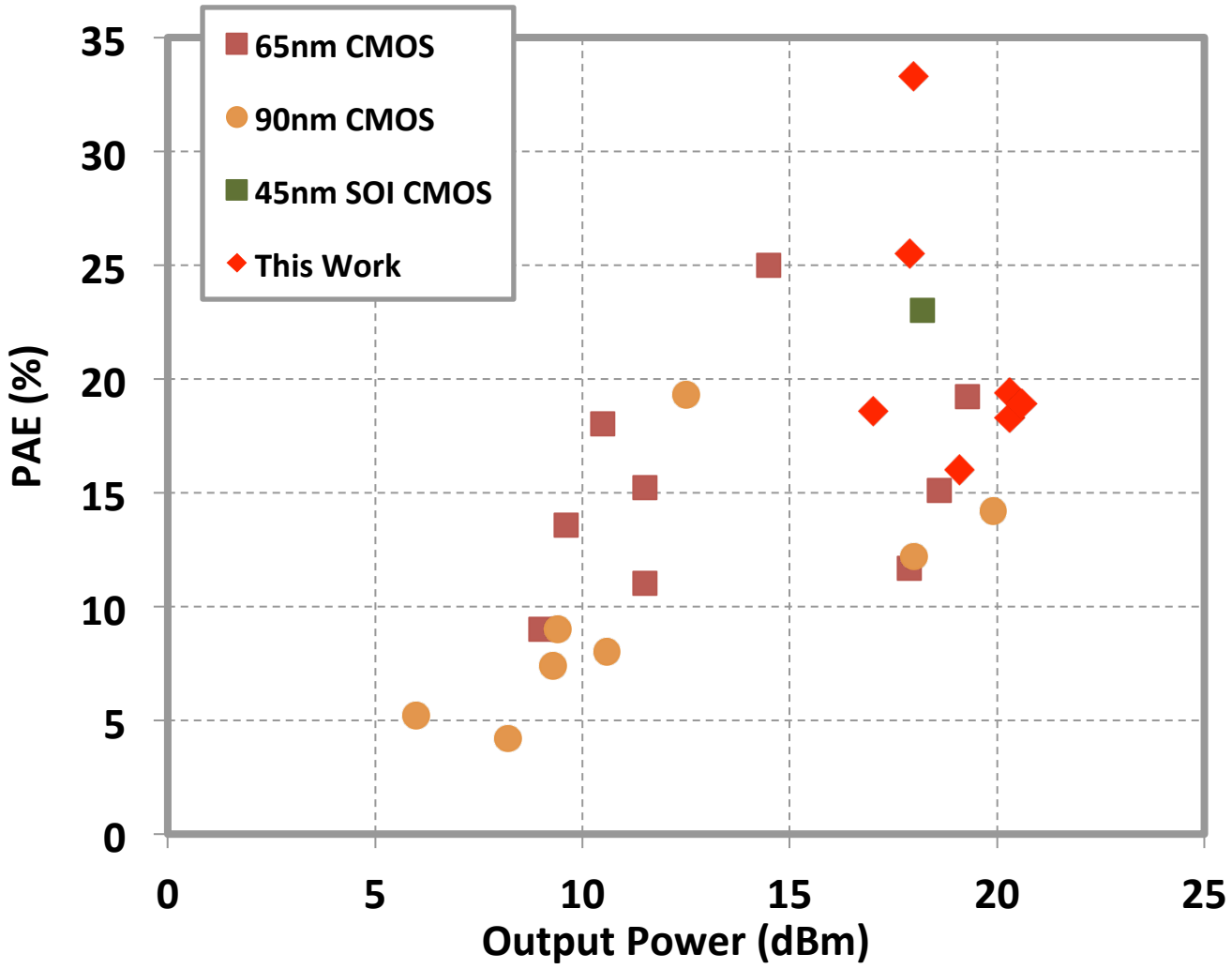
Large-Signal Performance





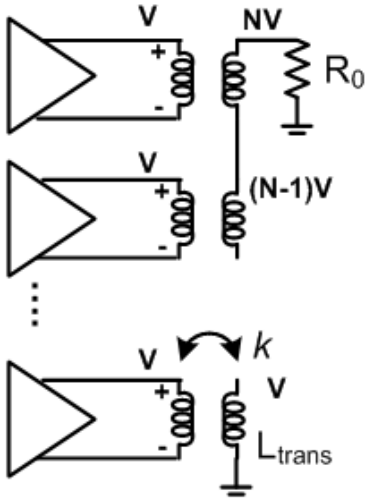
Performance Metric	Simulated Performance	Measured Performance
Center Frequency	45 GHz	47.5 GHz
Sat. Output Power	21.9 dBm	20.3 dBm
Power Gain	13.9 dB	12.8 dB
Drain Efficiency (η)	34 %	22.9 %
PAE_{MAX}	30.4 %	19.4 %

Comparison to State of the Art



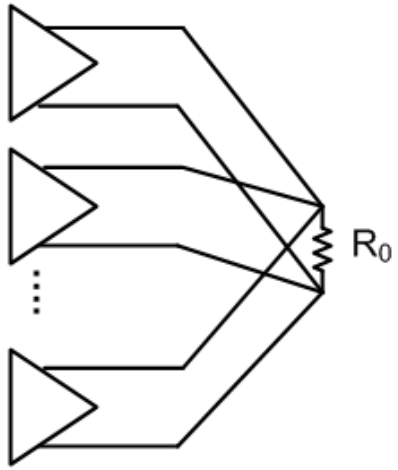
Conventional Power Combining

Transformer Combining



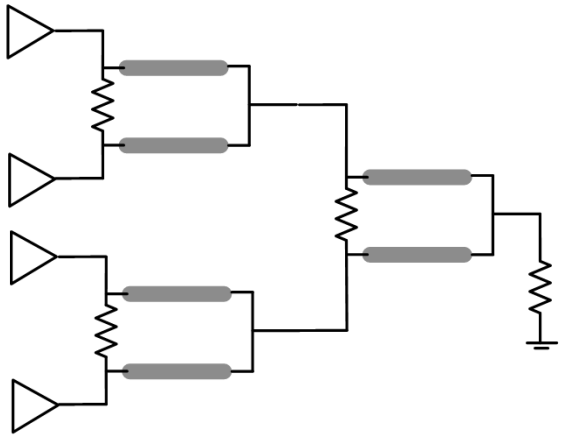
- Current remains constant, voltages are added.
- Nominal input impedance is R_0/N.
- In the presence of parasitics, PAs see asymmetric input impedance.

Current Combining



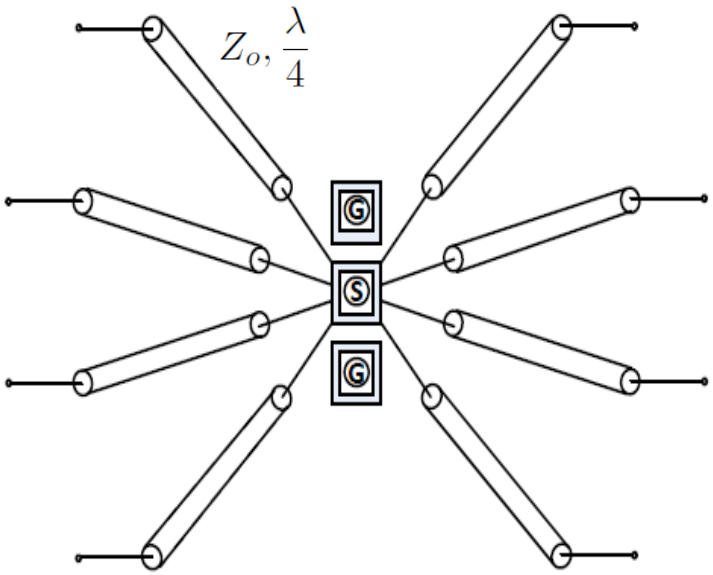
- Voltage remains constant, currents are added.
- Input impedance is R_0xN.
- Increased load reduces power generated by each PA – no power combining benefit.

Wilkinson Combining

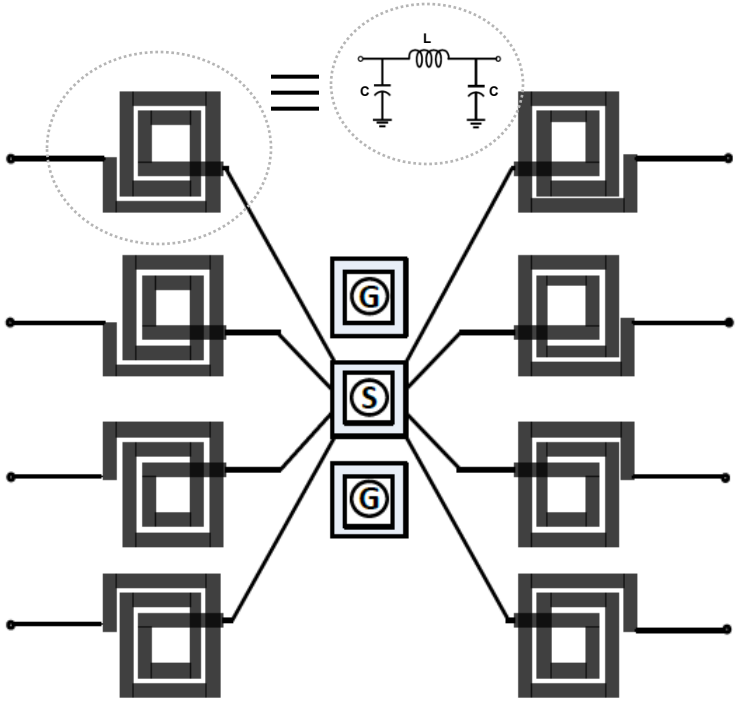


- Impedance remains constant along the combining tree.
- Cascading 2:1 Wilkinsons results in increased loss.
- N:1 Wilkinsons are challenging due to high Z_0 required.

Lumped Quarter-Wave Combiner



T-line-based λ/4 combiner
(n-way Wilkinson w/o isolation resistors)



Spiral based λ/4 combiner

$$Z_o(n) = 50\sqrt{n}$$

$$Z_o(8) = 141.421\Omega$$

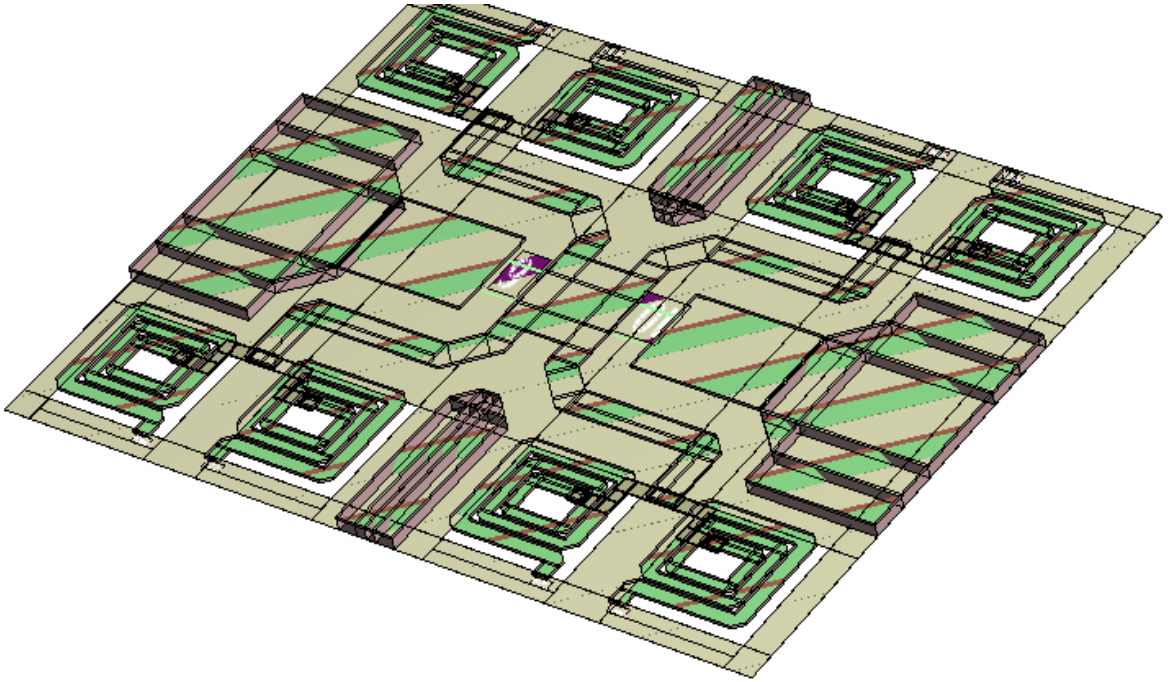
Cannot be achieved in an on-chip t-line.

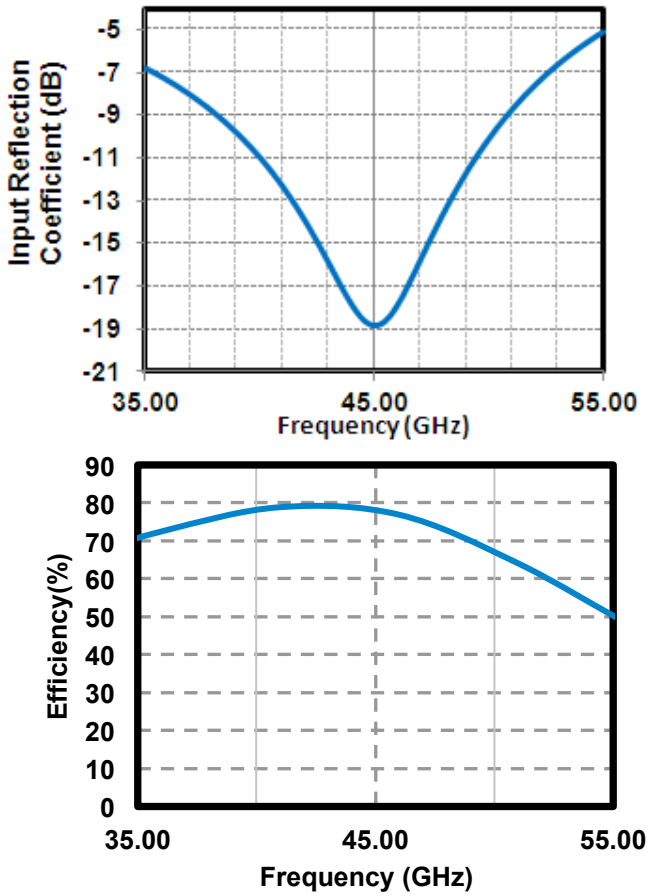
$$Z_o(n) = \sqrt{\frac{L(n)}{C(n)}};\ \omega = \frac{1}{\sqrt{L(n)C(n)}}$$

$$L(8)|_{45GHz} = 0.5nH\ ;\ C(8)|_{45GHz} = 25fF$$

Can be achieved in an on-chip spiral.

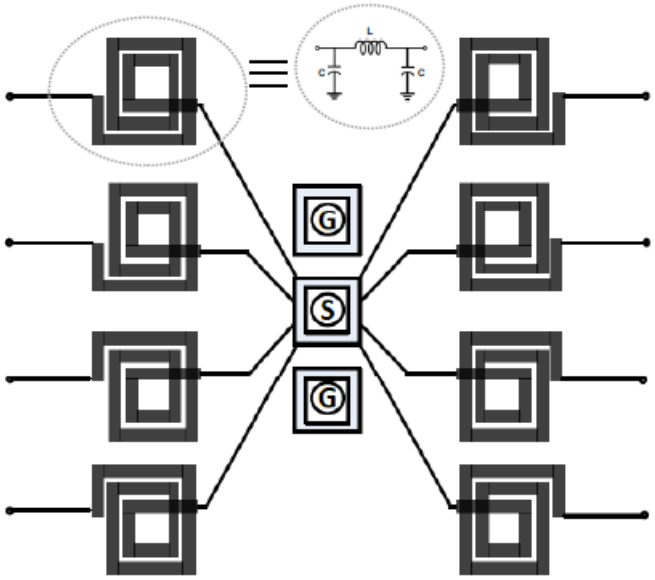
8-Way Combiner EM Simulation

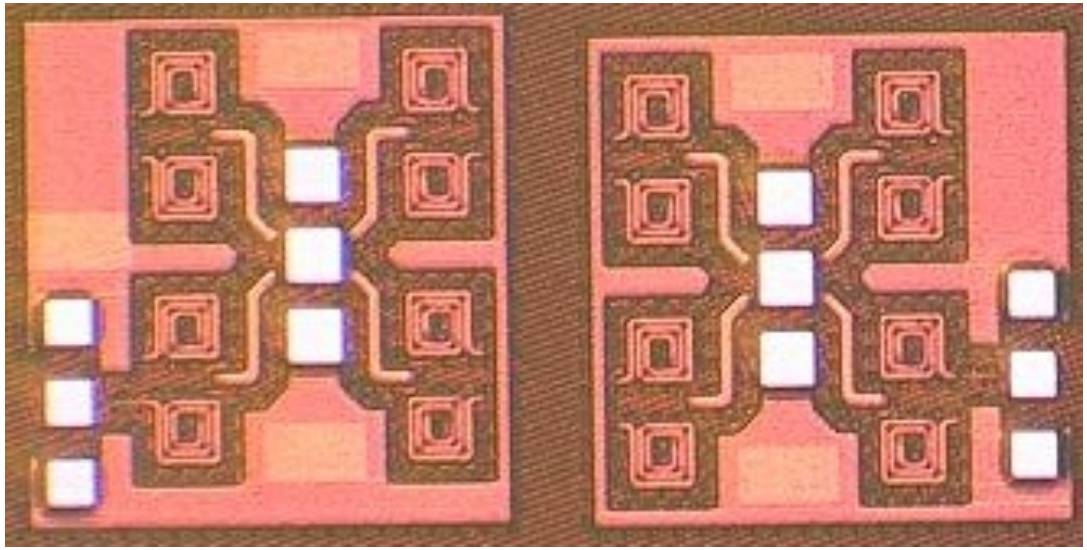




- T-line with Z_0 =140Ω for an 8-way combiner cannot be realized on chip but 0.5nH spiral with <25fF parasitic capacitance can.
- 8-way lumped λ/4 combiner achieves ~78% eff. with 50Ω input.

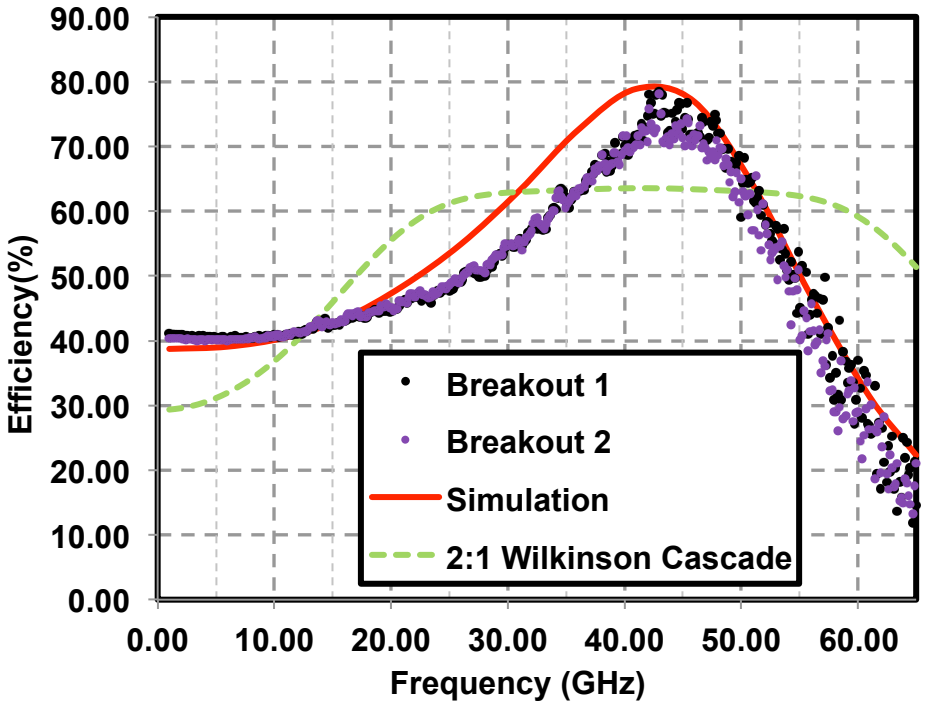
Lumped 8-Way Combiner Breakout





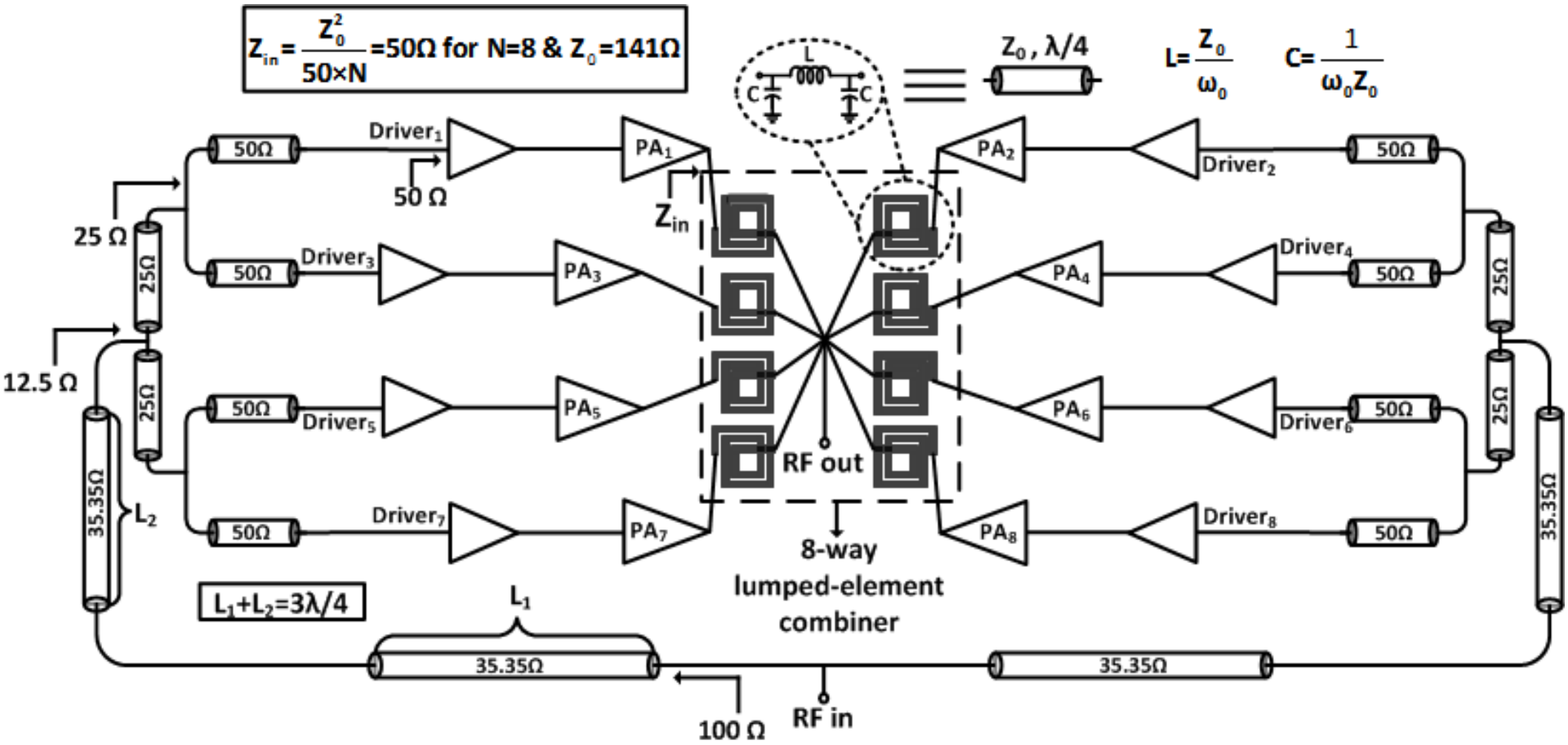
- Two separate combiner breakouts to test asymmetry between inputs.
- Separate spiral inductor breakout to test inductance, Q etc.

Combiner Performance

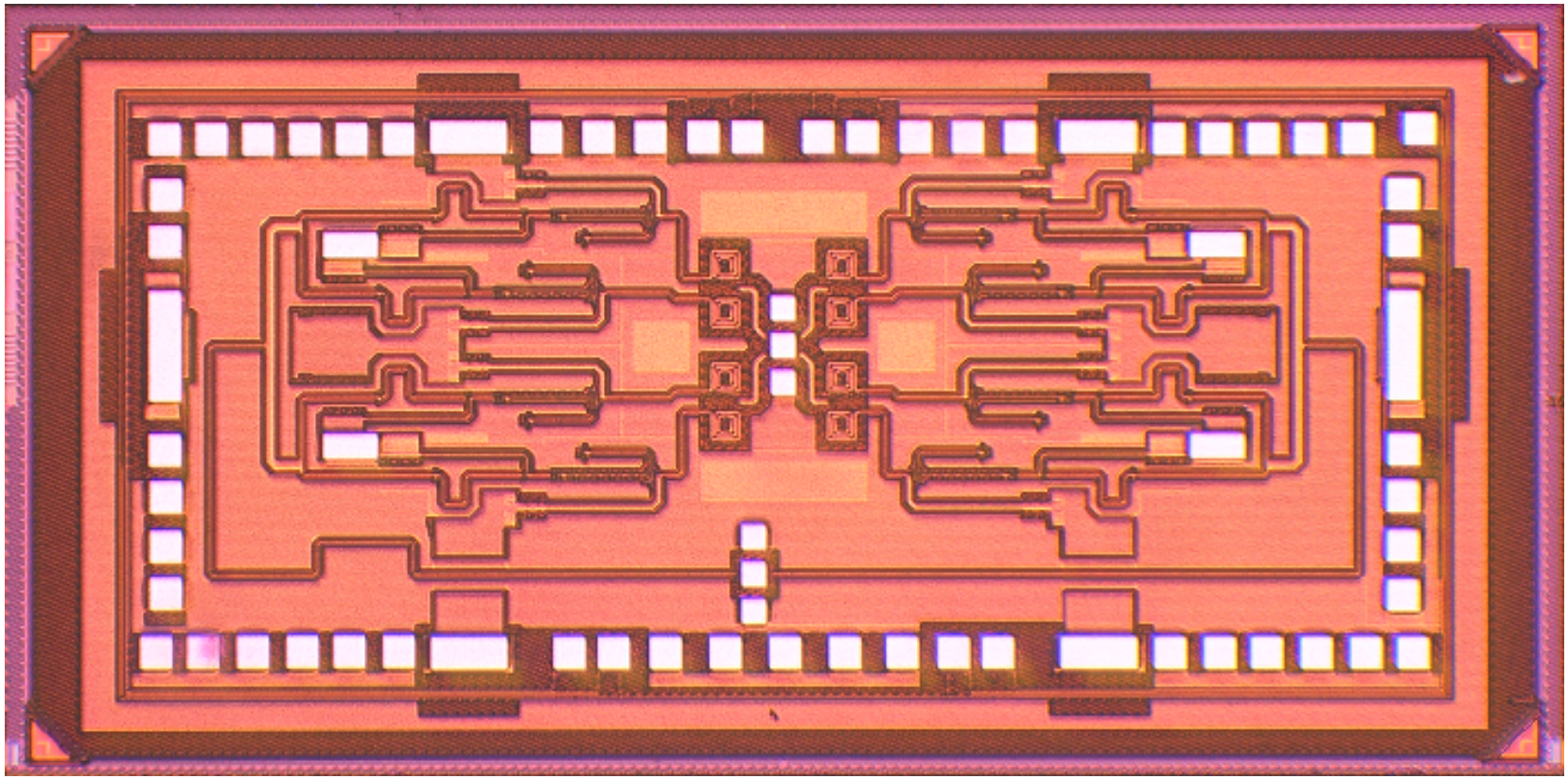


- Close correspondence with EM simulations.
- No significant asymmetry in combiner inputs seen.
- 72-75% efficiency is observed in measurement.
- 15% better than a 3-way cascade of 2:1 t-line Wilkinsons.

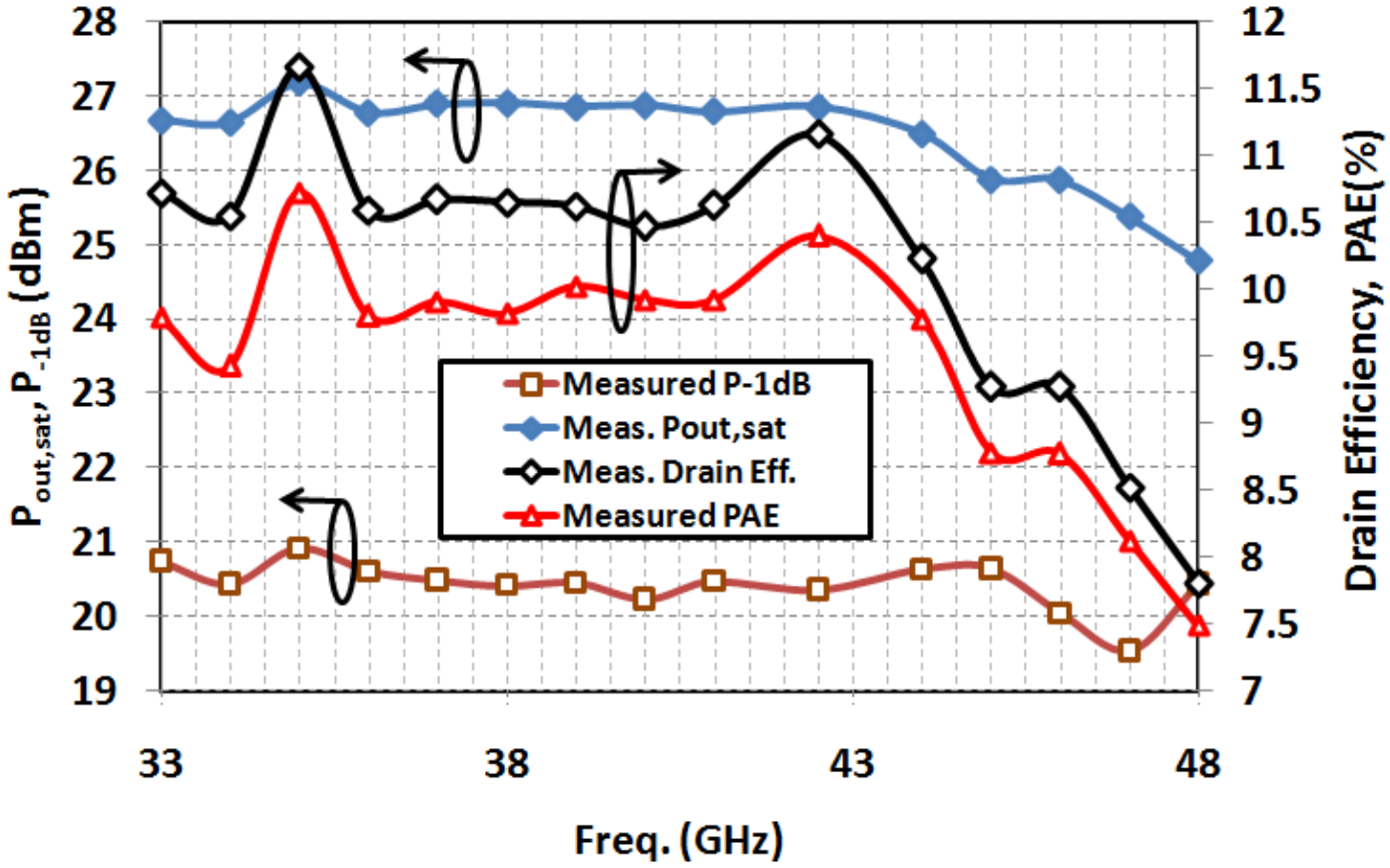
45GHz 45nm SOI Watt-Class PA



45GHz 45nm SOI Watt-Class PA



Watt-Class PA Performance



- **~27dBm (0.5W) of $P_{out,sat}$ is measured over a wide range.**
- -1dB flatness is observed in $P_{out,sat}$ and $P_{out,-1dB}$ from 33-46GHz.
- Measurement below 33GHz is limited by the setup.

Comparison to Prior Silicon PAs

Work	[1]	[2]	[3]	[4]	[5]	This Work
Technology	130nm SiGe	130nm SiGe	130nm SiGe	90nm CMOS	45nm SOI CMOS	45nm SOI CMOS
Frequency/-1dB BW	59-64GHz	58-62GHz	80-90GHz	60GHz◊	41.5-48.5GHz#	33-46GHz*
Peak Gain	20dB	18dB	8dB	20.6dB	>18dB	19.4dB
Peak P_{sat}	23.1dBm+	20dBm+	21dBm	19.9dBm	24.3dBmo	27.2dBm
Peak P_{-1dB}	Not Reported	13.1dBm	Not Reported	18.2dBm	N/R	21dBm
Peak PAE	6.3%	12.7%	Not Reported	14.2%	14.6%	10.7%
Peak Drain Eff.	Not Reported	15%	4%	Not Reported	21.3%	11.7%
Fully integrated?	Yes	Yes	Yes	Yes	Noo	Yes

* Measurement below 33GHz is limited by equipment.

o Does not have an on-chip choke inductor (biased using external bias-Ts) and assumes ideal 3dB external differential-to-single-ended converter.

Limited by input balun.

◊ Large-signal performance across frequency is not reported.

\+ Assumes ideal 3dB external differential-to-single-ended converter

[1] U. R. Pfeiffer et al, "A 23-dBm 60-GHz Distributed Active Transformer in a Silicon Process Technology," *IEEE T-MTT*.

[2] U. R. Pfeiffer et al, "A 20 dBm Fully-Integrated 60 GHz SiGe Power Amplifier With Automatic Level Control," *IEEE JSSC*.

[3] Ehsan Afshari et al, "Electrical Funnel: A Broadband Signal Combining Method," in *2006 IEEE ISSCC*.

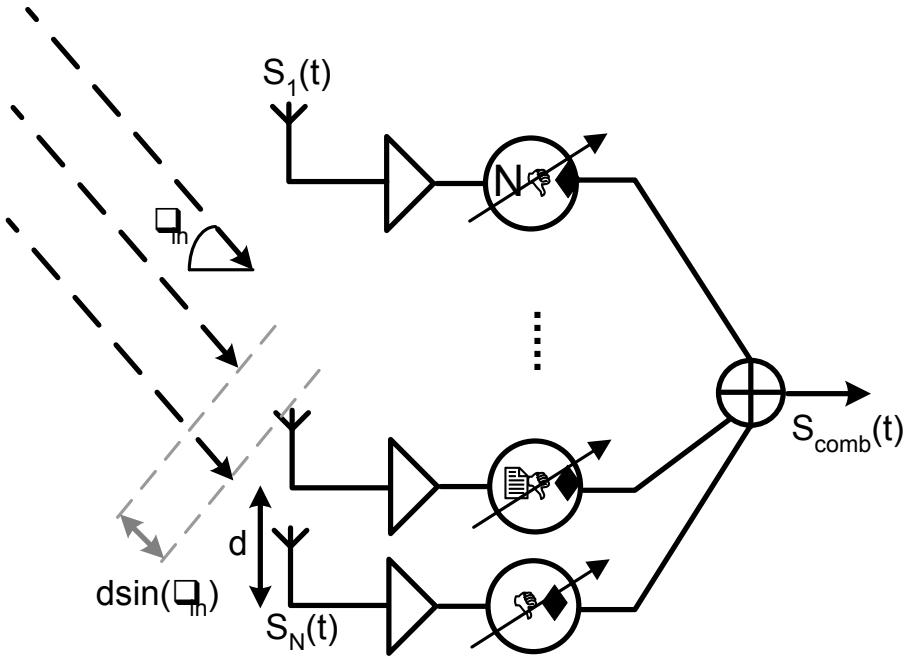
[4] Chi Y. Law et al, "A High-Gain 60GHz Power Amplifier with 20dBm Output Power in 90nm CMOS," in *2010 IEEE ISSCC*.

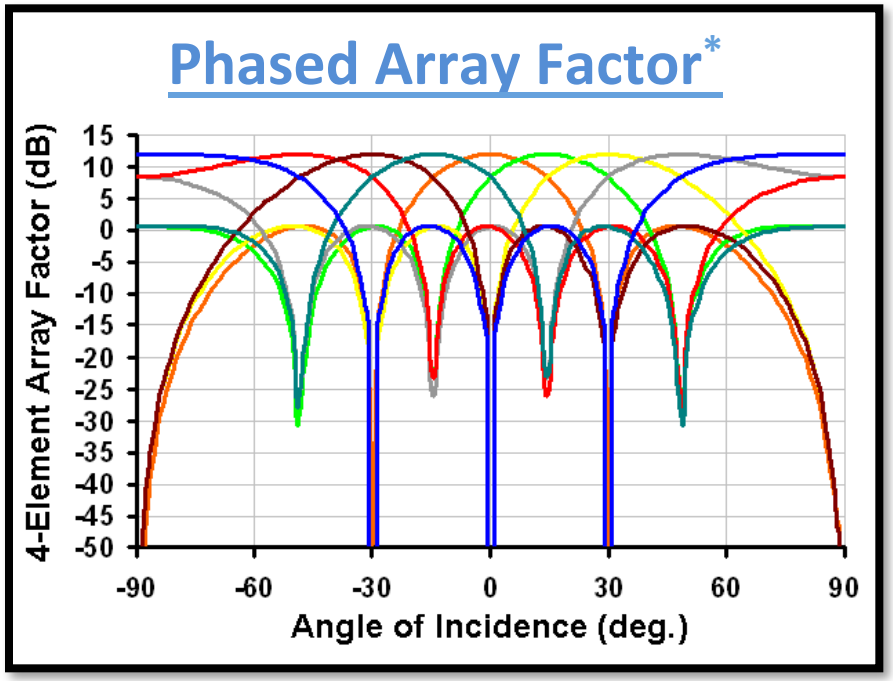
[5] A. Balteanu et al, "A 45-GHz, 2-bit power DAC with 24.3 dBm output power, >14 Vpp differential swing, and 22% peak PAE in 45-nm SOI CMOS," in *2012 IEEE RFIC Symposium*.

Outline

- Brief History of RF/mmWave in CMOS
- Active and Passive Device Modeling
- Low-Noise Amplifier Design
- Oscillators and VCOs
- Power Amplifiers
- **Multiple-Antenna Systems**

Phased Array Principle

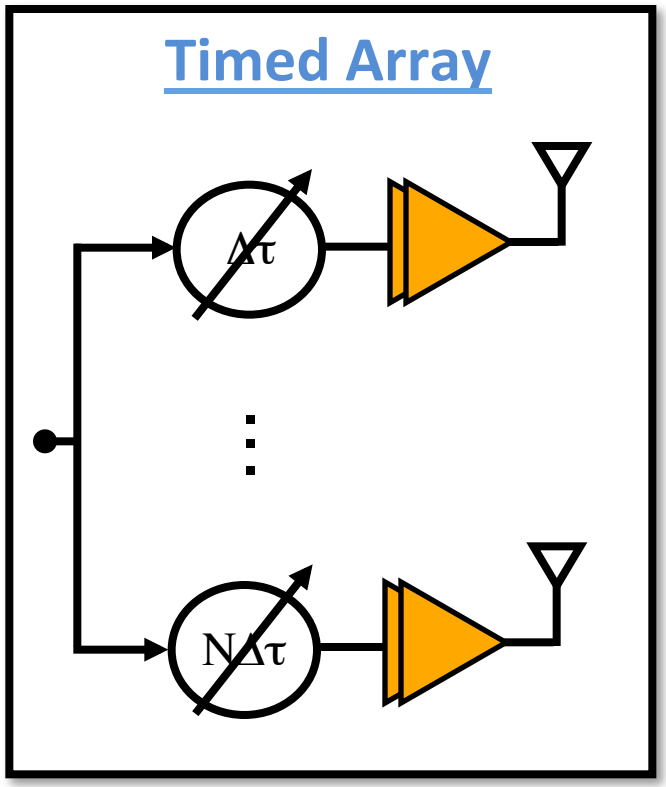


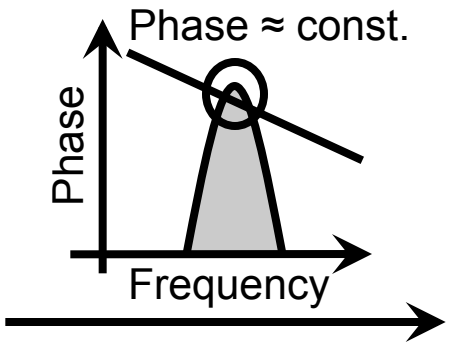


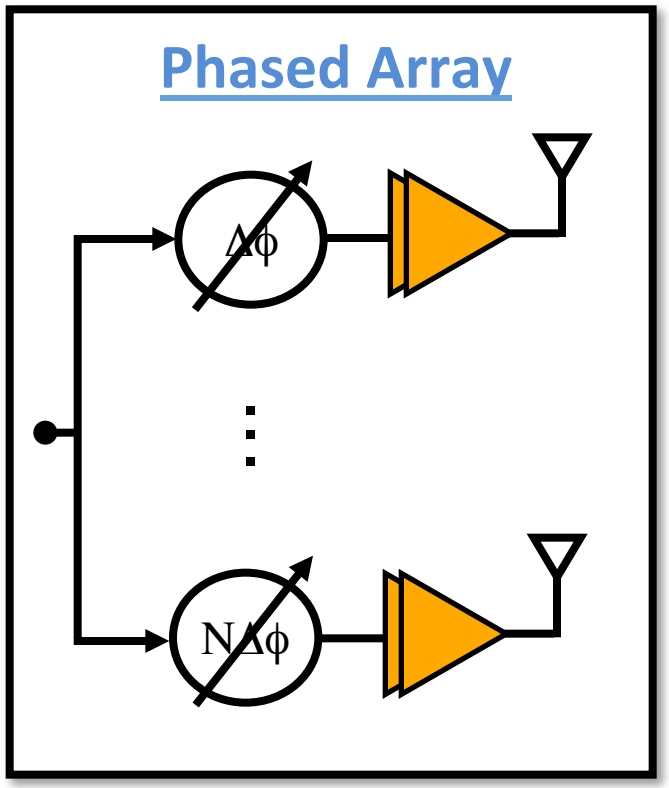
*For different $\Delta\tau$ values and d=λ/2

- Spatial interference cancellation.
- 10log(N) improvement in RX SNR.
- 20log(N) improvement in TX EIRP.

Phased Arrays vs. Timed Arrays





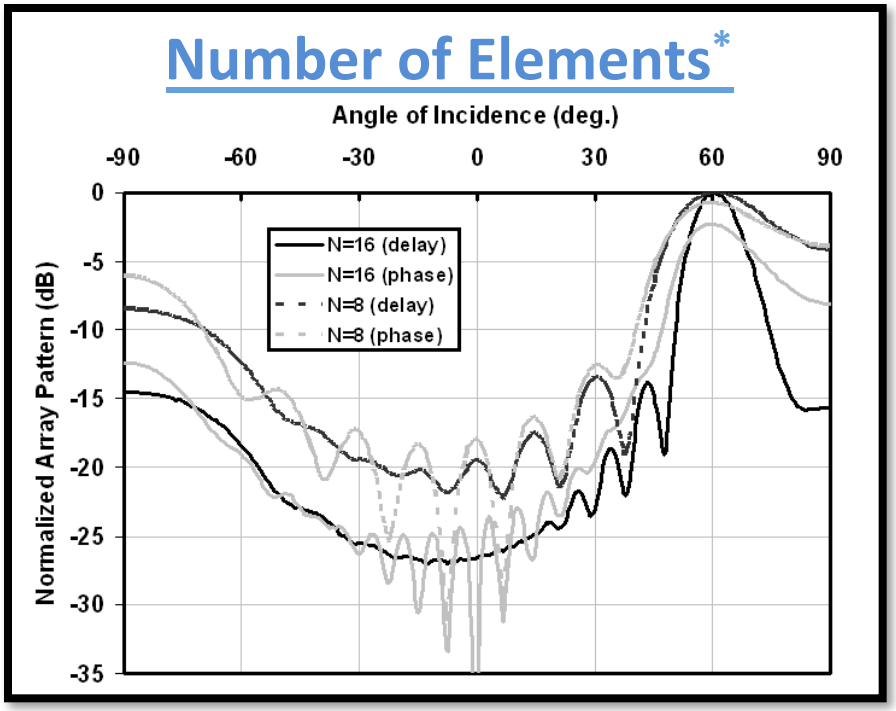


$$AF(\Delta\tau,\theta_{in}) = \left(\frac{\sin\frac{N\left(\omega\Delta\tau - \pi\sin\theta_{in}\right)}{2}}{\sin\frac{\left(\omega\Delta\tau - \pi\sin\theta_{in}\right)}{2}} \right)^2$$

$$AF(\Delta\phi,\theta_{in}) = \left(\frac{\sin\frac{N\left(\Delta\phi - \pi\sin\theta_{in}\right)}{2}}{\sin\frac{\left(\Delta\phi - \pi\sin\theta_{in}\right)}{2}} \right)^2$$

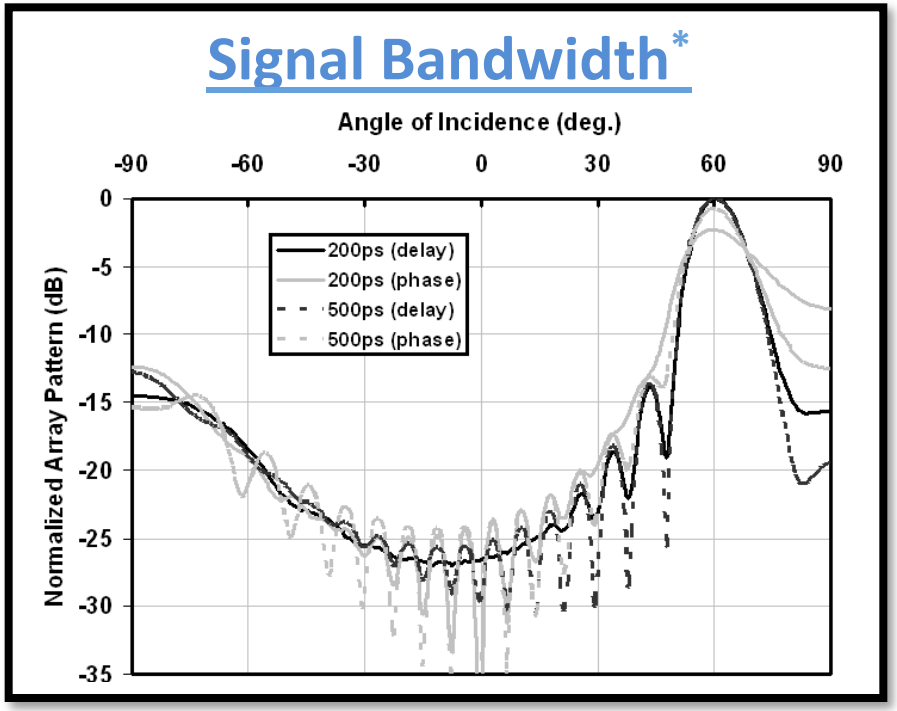
Phased-Array Approximation

Number of Elements*



*25.5GHz pulsed-sinusoids with pulse width 200ps

Signal Bandwidth*



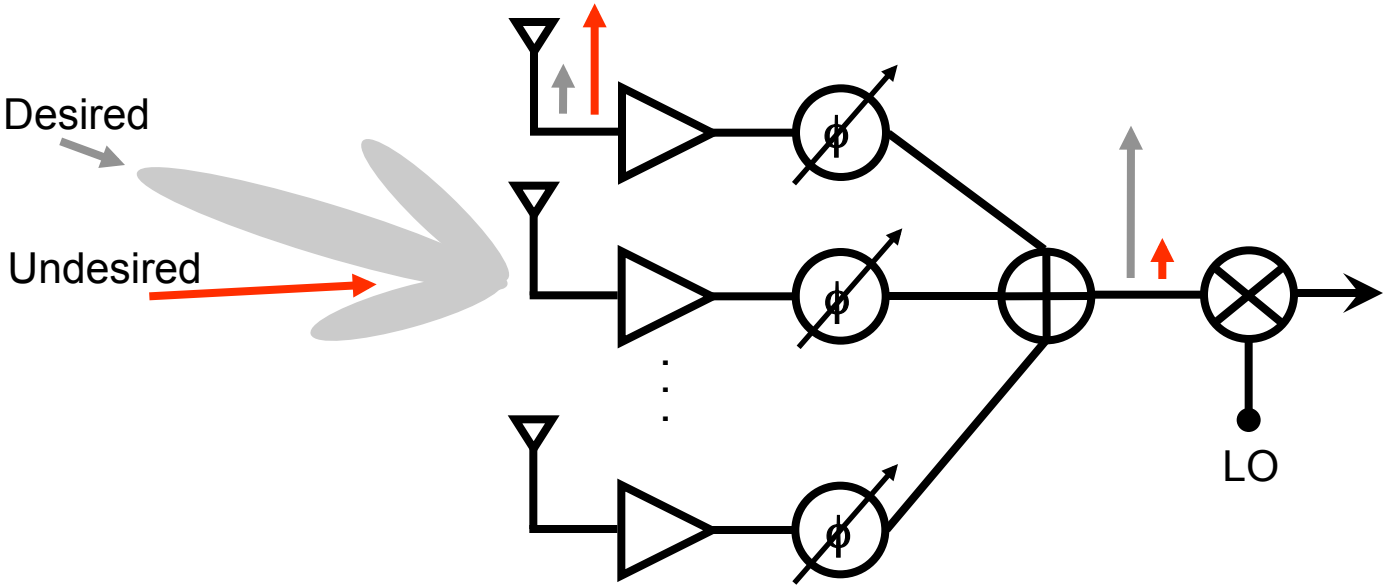
*16-elem. array using 25.5GHz pulsed-sinusoids.

The validity of the phase-delay approximation depends on

1. Number of array elements
2. *Fractional* signal bandwidth
3. Maximum angle of incidence

mm-Wave advantage!

Phased Array Topologies

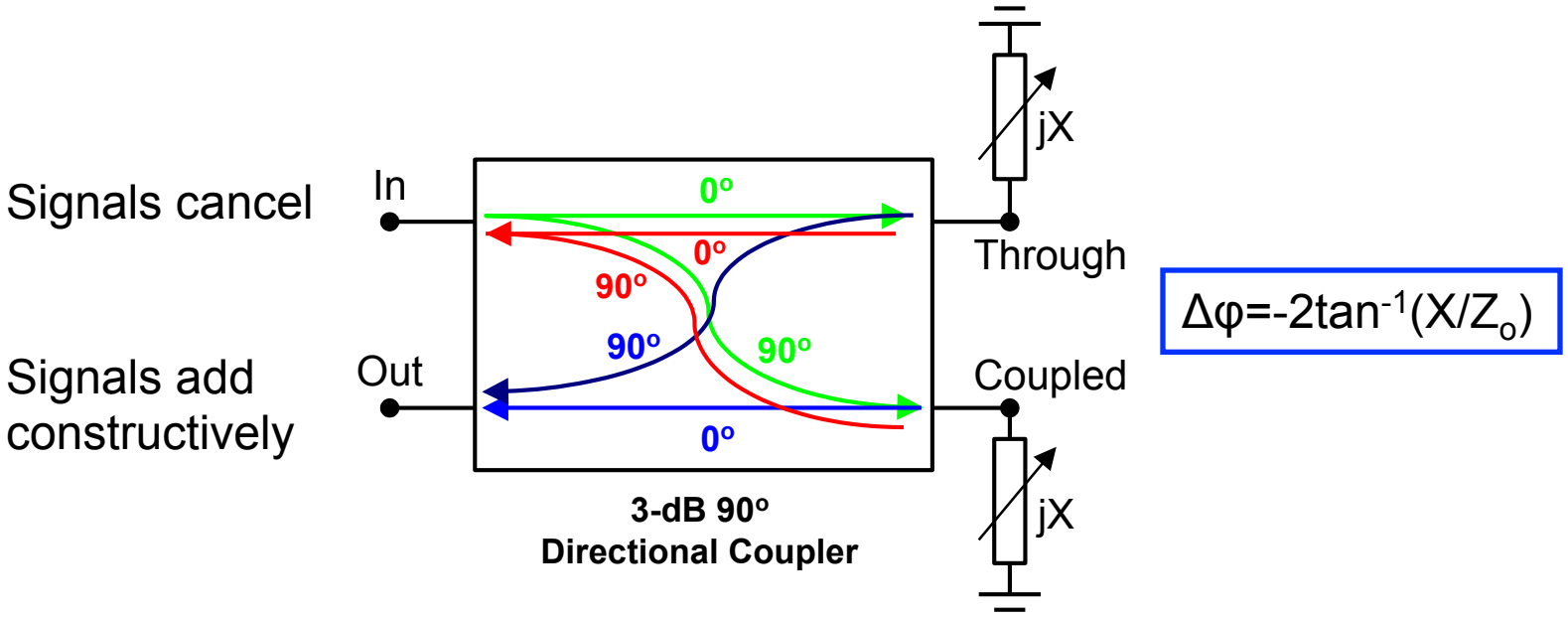


RF Phase-Shifting Architecture

+ Mixer dynamic range requirements eased due to interference cancellation.

- Compact, low-loss phase-shifters are challenging on silicon.

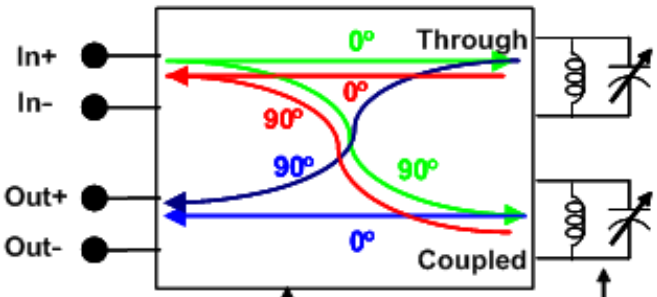
Reflection-Type Phase Shifter

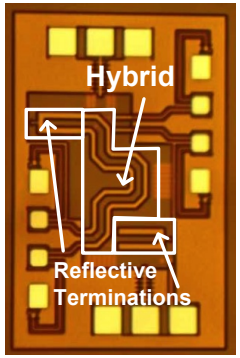


Challenges

- Loss in the quadrature 3dB coupler.
- Loss in the variable reflective termination.

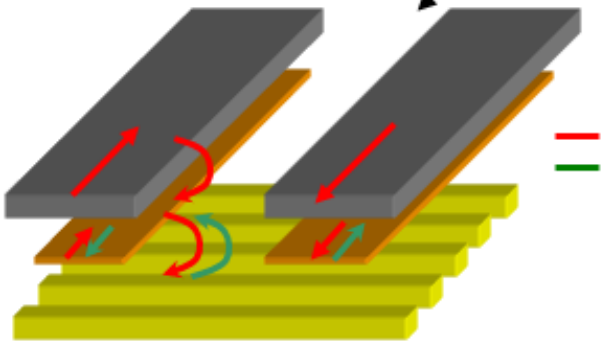
60GHz Differential RTPS in 0.13μm*

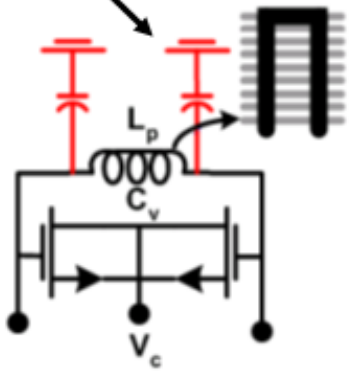


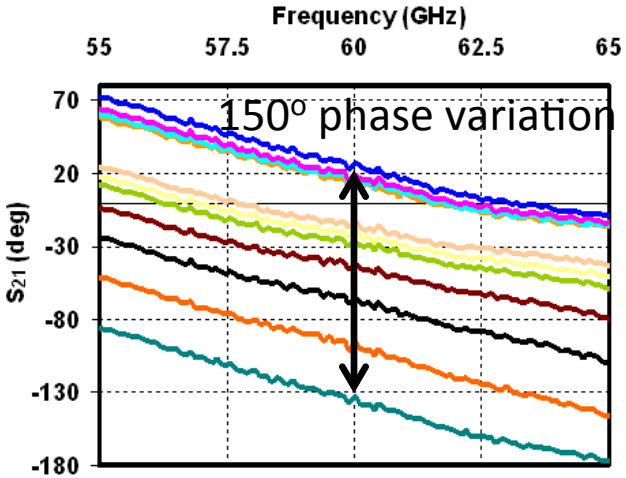


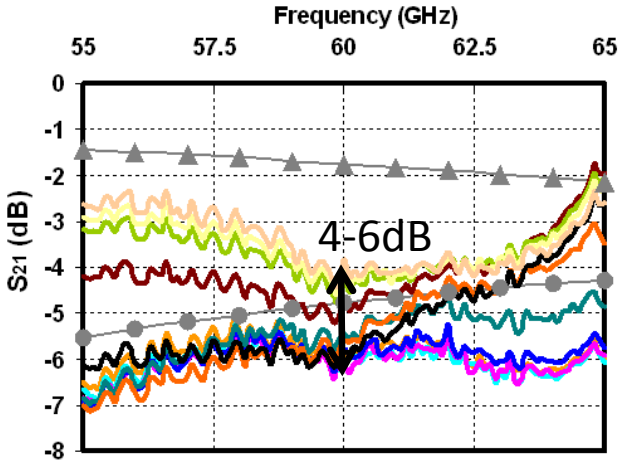
Vertical Coupled-Line Differential Coupler

Variable, resonant, shunt-LC reflective terminations





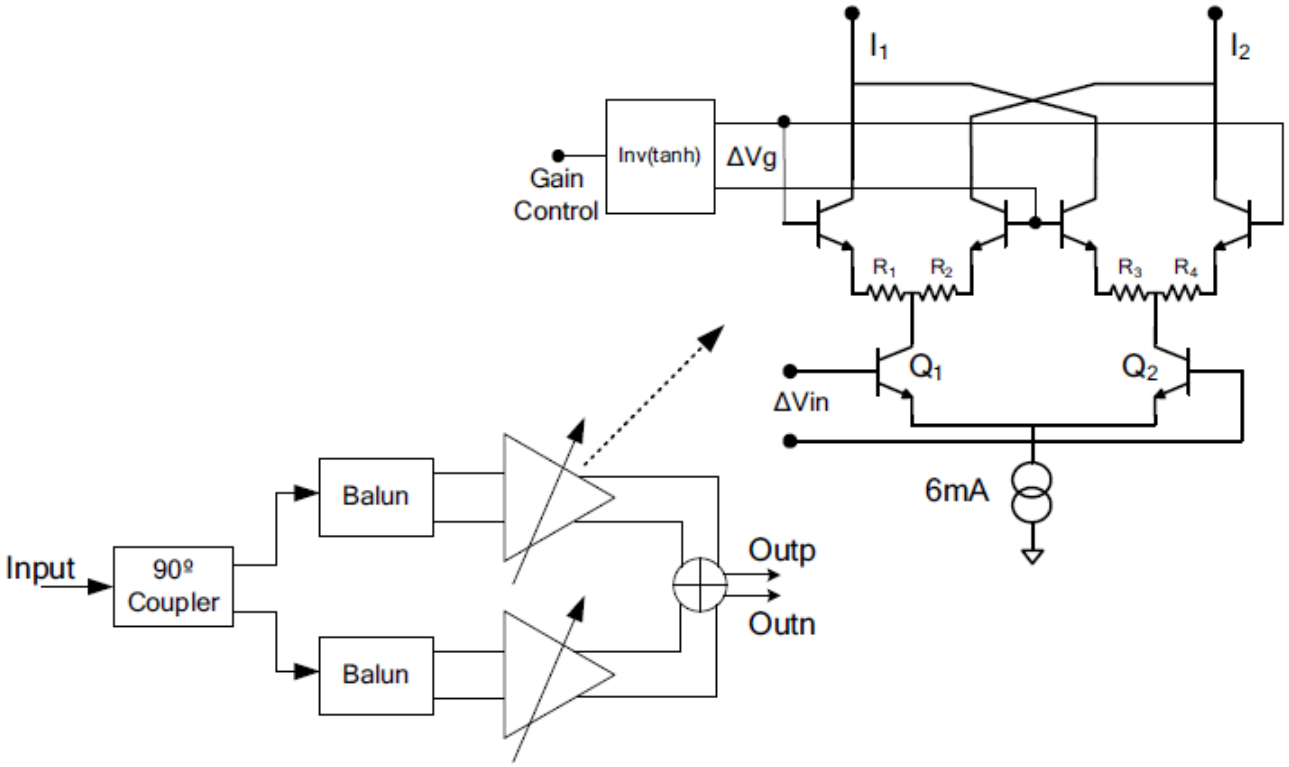


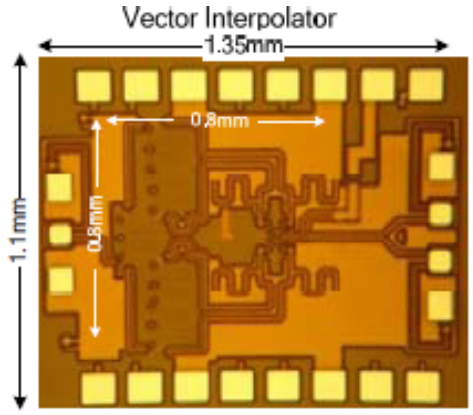


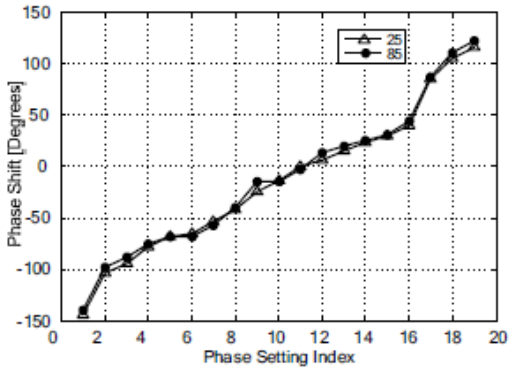
- A variable-gain amplifier is typically needed to compensate for the phase-dependent insertion loss.

* Krishnaswamy et al, "A Silicon-Based, All-Passive, 60GHz … Differential, Reflection-Type Phase Shifter," ARRAY 2010.

Vector Interpolator*



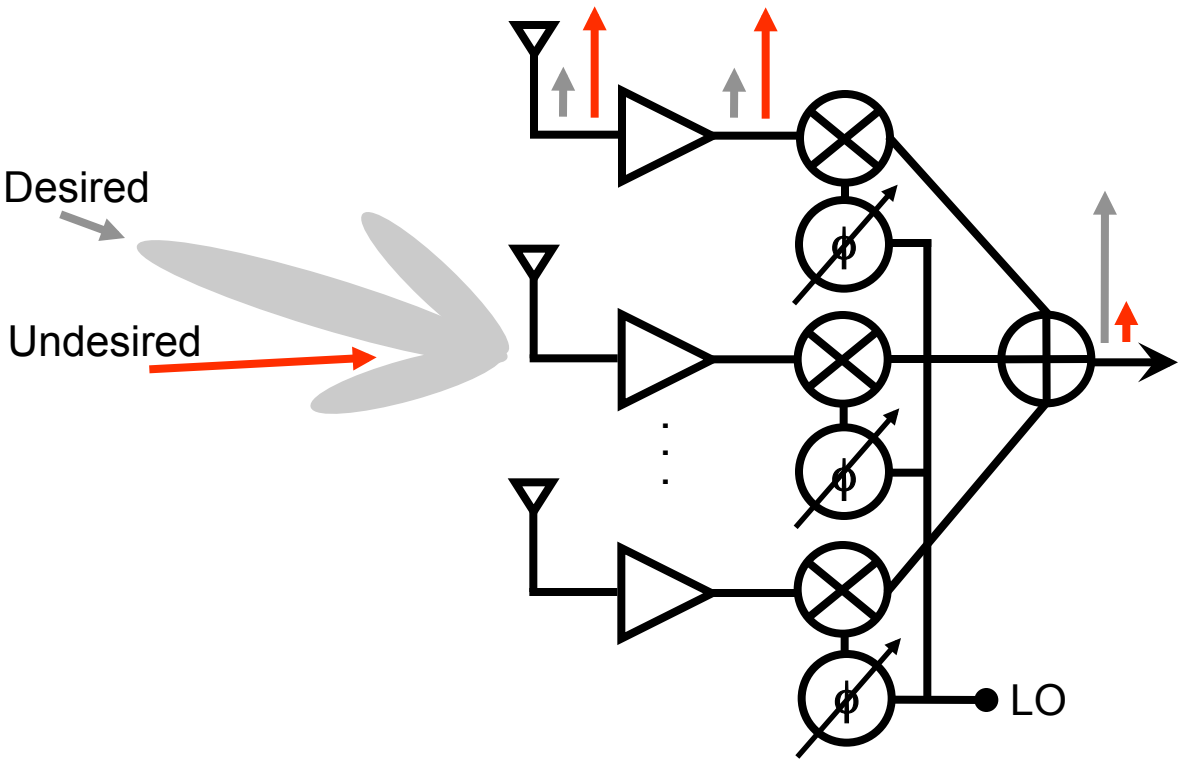




- Ming-Da Tsai et al, "60GHz Passive and Active RF-path Phase Shifters in Silicon," RFIC 2009.

* Figures are the property of the IEEE

Lo Phase-Shifting Architecture

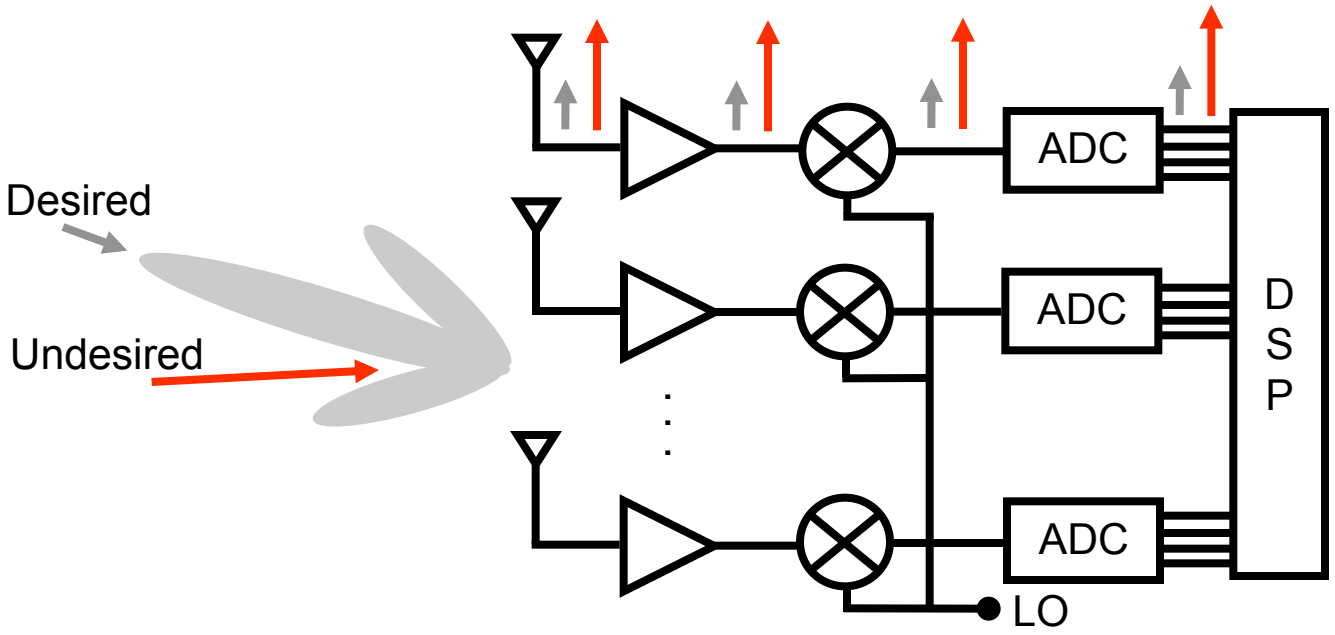


LO Phase-Shifting Architecture

+ Phase shifter is out of the RF signal path.

- Mixers must have enough dynamic range to sustain interferers.

Digital Beamforming Architecture



Digital Beamforming Architecture

+ Flexibility.

- High power consumption of multiple high-dynamic-range ADCs, DSP.

Conclusion

- Millimeter-wave design in CMOS is an exciting emerging area of research with interesting academic research problems *and* commercial applications.
- Millimeter-wave circuit involves an interesting synthesis of RFIC design techniques employed below 10GHz with microwave circuit design concepts traditionally employed in non-integrated settings.
- Current open research problems:
  - Efficient watt-class mmWave PAs *in linearizing architectures*
  - Efficient large-scale mmWave arrays
  - Electromagnetic interfaces for mmWave ICs (antennas on silicon, antennas in package?)
  - Pushing CMOS to high mmWave/THz frequencies (>200GHz)