Assignment-1

Questions 1.1 to 1.4 are straightforward and one can answer them by carefully attending the class-lectures. For 1.5, see [1] and/or [2] from library; for 1.6 see [2] and/or [3]; and think more before answering 1.7.

1.1 Discuss why the doping concentration of the emitter region is the highest, and then that of the base region, and the collector region is least doped? What are the effects of increasing or reducing the doping concentrations and or thickness of the emitter, base, and/or collector regions? Give proper reasoning on the effects of the transistor performances. In this regard, point out the requirements of an ideal transistor and the constraints against achieving the requirements.

1.2 How will a deep emitter and a scaled down emitter affect the base current?

1.3 Why is the doping concentration of the external base more than that of the internal base?

1.4 What is the requirement of the SIC implant? How can it reduce the internal base and how will it affect the internal BC depletion capacitance?

1.5 In a poly-Si emitter BJT, how does a poly-Si layer affect the base current? Why does a deep poly-Si layer in the emitter not contribute much adversely in raising the emitter resistance?

1.6 How can the double-poly self-aligned process reduce the total footprint of the transistor? How does it affect the speed performance of the device?

1.7 Why will the quasi-Fermi potential in the neutral base have to be equated with the base contact potential in a 1D transistor operation?

[1] A. K. Kapoor, D. J. Roulston, Eds., Polysilicon Emitter Bipolar Transistors, New York, IEEE Press, 1989.

[2] D. J. Roulston, Bipolar Semiconductor Devices, McGraw Hill, 1990.

[3] T.H. Ning et al, IEEE Trans. Electron Devices, vol. ED-28, pp. 1010-1013, 1981.

Assignment-2

Questions 2.1, 2.2, 2.5 are straightforward and one can answer them by carefully attending the class-lectures. For 2.3, keep in mind that there are various kinds of amplifiers, such as voltage-amplifier, current amplifier, and power amplifier. For 2.4, search in any basic text book for the recombination process within the space-charge-layer. For 2.6, see section 2.1.4.1 in page-34 of [4]; and think more before answering 2.7.

2.1. What are the various components of base current in a BJT? Under what conditions, which component will dominate over the other components?

2.2. What are the various components of the collector current in a BJT? Under what conditions, which component will dominate over the other components?

2.3. In which situation, does the value of the current transfer ratio become near to unity? Can a BJT in common-base mode be used as an amplifier? Give reason.

2.4. What are the typical values for m_{BEj} and m_{BEr}? Why are they unequal?

2.5. Plot the $V_{B'E'}$ dependent base current and the BE junction capacitance. Write down the steps how you can extract the various related model parameters.

2.6. What happens to the Q_{jEi} and C_{jEi} if (a) $V_{B'E'}=V_{DEi}$ (b) $V_{B'E'}>V_{DEi}$? Can you think of a better solution for C_{jEi} and Q_{jEi} to overcome any problem encountered here?

2.7. If $\tau_f=\tau_{f0}+k_1(i_{Tf0})^{k2}$, and $i_{Tf0}=I_{TS0}\exp(V_{B'E'}/V_T)$, where τ_{f0} is $V_{B'E'}$-independent, k_1,k_2,I_{TS0} are model parameters, and τ_f (i_{Tf0}) refers to the bias-dependent forward transit-time (transfer-current), find out the expression for the forward diffusion capacitance.

[4]Available Online at: http://www.iee.et.tu-dresden.de/iee/eb/forsch/Hicum_PD/Hicum22/hicumL2v2p23/chapter2.pdf

Assignment-3

Questions 3.1, 3.2, 3.4 are straightforward and one can answer them by carefully attending the class-lectures. For 3.3, keep in mind that the hole charge within the base takes major share specially in low current region. Please try to search the answer from the references given at the beginning of the session and/or think more. For 3.5 and 3.6, see section 2.1.3.1 in [4] and also think on it.

3.1. Derive the ICCR for the transfer current in a p-n-p BJT.

3.2. Which assumptions in ICCR can lead to erroneous computation of the transfer current and why?

3.3. In the ICCR, can one integrate the hole charge only within the neutral base region, instead of taking the integration throughout the 1D structure from emitter lead to the collector lead? Give elaborate reasoning.

3.4. If $\tau_f=\tau_{f0}+k_1(i_{Tf0})^2$, where τ_{f0} is $V_{B'E'}$-independent, k_1 is a model parameter, and τ_f (i_{Tf0}) refers to the bias-dependent forward transit-time (transfer current), can you find out explicit expressions for total normalized hole charge and transfer current considering a bias-independent reverse transit time, τ_r?

3.5. Since in the transit time formulation the critical collector current I_{CK} comes in the denominator and sometimes within a square root, neither a zero nor a negative value of I_{CK} is permitted in a compact model implementation. Can you figure out a better expression for I_{CK} with these constraints in mind?

3.6. If i_{Tf0} is less than the critical collector current, I_{CK}, the current dependent part of the transit time $\Delta\tau_f$ can become negative, which is an unphysical value. Can you figure out a better expression for the current dependent forward diffusion charge, ΔQ_{f0} to get rid of this problem?

[4]Available Online at: http://www.iee.et.tu-dresden.de/iee/eb/forsch/Hicum_PD/Hicum22/hicumL2v2p23/chapter2.pdf

Assignment-4

Questions 4.1, 4.2, 4.3, 4.4 are straightforward and one can answer them by carefully attending the class-lectures. For 4.5 and 4.6, please thoroughly think and answer.

4.1. Derive the TICC relation for 1D transient collector and emitter current densities for a p-n-p BJT including the effect of recombination terms.

4.2. How can you describe the charge partitioning effect without using any equation, but only the temporal and positional description of electron concentration, n(x,t)?

4.3. Draw the large signal equivalent circuit model of a 1D BJT that includes the charge partitioning phenomenon. Can you figure out a relation between the charge partitioning factors, β_c and k_c?

4.4. How can one model the charge partitioning factor, k_c using the TICC weight function? How can the charge partitioning factors, β_c and k_c be modeled using various transit time components?

4.5. How will the transient collector current be affected by the charge partitioning effect? Describe using proper plots.

4.6. Can you prove that the TICC weight function $F_C(x)$ satisfies the generalized charge partitioning rule?

Assignment-5

All questions are straightforward and one can answer them by carefully attending the class-lectures.

5.1. Write down various components of the small signal base and collector currents following the small-signal equivalent circuit model. Which current components can be neglected in a forward active mode of operation?

5.2. Derive a relation between C_{diff1} and g_{m0}?

5.3. How can you estimate the depletion capacitances, C_{jEi} and C_{jCi} from the y-parameters data of a 1D BJT?

5.4. How can you extract the charge partitioning factor, k_c from the y-parameter and depletion capacitance data of a 1D BJT?

5.5. Plot the frequency-dependent magnitude and phase of y-parameters for a 1D BJT.

Assignment-6

All questions are straightforward and one can answer them by carefully attending the class-lectures.

6.1. How does the full regional approach helps in determining total 1D transistor delay, τ_d or the transistor cut-off frequency, f_T? Note that f_T is determined keeping $V_{C'E'}$ constant.

6.2. Which junction charge component is considered within the forward transit time, τ_f? How can the forward transit time be extracted from measured characteristics?

6.3. How is it possible to make even a better estimation of f_T using charge partitioning principle? How does it reduce to the f_T formulation given by Gummel at zero charge partitioning (one that uses the ratio between the operating frequency and the imaginary part of the inverse a.c. gain)? When does it reduce to the conventional f_T estimation rule?

6.4. Discuss the reason of the rise and fall of f_T with bias current. How can one estimate the charge partition factor k_c in terms of base minority charge partitioning factor, β_c at low and high current regimes.

Assignment-7

All questions are straightforward and one can answer them by carefully attending the class-lectures.

7.1. How do the frequency-dependent phases of y_{11} and y_{21} behave at QS and NQS regimes? What is the cause of these phase variations at NQS regime?

7.2. Derive $\Delta i_T(\omega)$ and $\Delta Q_{nB}(\omega)$ using the given $\Delta n(x,\omega)$ from Te Winkel's theory.

7.3. For the following small-signal models of y_{11} and y_{21}, suggest a suitable model implementation technique in large-signal domain and write the corresponding verilog-A codes.

$$y_{11}(\omega) = g_{b0} + \frac{j\omega\tau_f g_{m0}}{1 + jA_{Q1}\omega\tau_f + A_{Q2}(\omega\tau_f)^2} \quad \text{(A7.1)}$$

$$y_{21}(\omega) = \frac{g_{m0}\exp(-j\alpha\omega\tau_f)}{1 + jA_{Q1}\omega\tau_f}. \quad \text{(A7.2)}$$

7.4 How can you extract the model parameters, A_{Q1}, A_{Q2}, and α?

7.5. If A_{Q2} is zero in (A7.1) repeat question 7.3.

7.6. If $A_{Q1}=A_{Q2}=0$ in (A7.1) and (A7.2), repeat question 7.3. What are the implications of zero values of these model parameters in frequency-dependent y-parameters plots in comparison with the corresponding QS plots?

Assignment-8

All questions are straightforward and one can answer them by carefully attending the class-lectures.

8.1. Draw the energy band diagram for the following hetero-junctions under forward biased conditions: (i) p-Si and n-SiGe, (ii) n-Si and p-SiGe.

8.2. Draw the energy band diagram for an n-p-n SiGe-base HBT in forward active mode.

8.3. Derive the expression for the maximum oscillation frequency (f_{max}) of a bipolar transistor considering the charge partitioning effect.

8.4. At the same high current regime a Si-BJT and a SiGe-HBT have the following parameters: (i) bias-point τ_f of the SiGe-HBT is one-fourth of that of the Si-BJT, (ii) effective base resistance of SiGe-HBT at the given bias point is found to be 20% of that of the Si-BJT, (iii) base-collector junction capacitance for SiGe-HBT at the same collector-base voltage appears to be double of that of the Si-BJT. If the f_{max} of the Si-BJT is found to be 70GHz, calculate the f_{max} of SiGe-HBT.

8.5. For the equivalent circuit (EC) of Fig. 1, following expressions are given:

$$i_{jBEi} = I_{BEiS}\left(\exp\left(\frac{V_{B'E'}}{m_{BEi}V_T}\right)-1\right), \qquad i_{jBCi} = I_{BCiS}\left(\exp\left(\frac{V_{B'C'}}{m_{BCi}V_T}\right)-1\right), \qquad i_{Tf} = \frac{c_{10}}{Q_{pT}}\exp\left(\frac{V_{B'E'}}{m_{cf}V_T}\right),$$

$$i_{Tr} = \frac{c_{10}}{Q_{pT}}\exp\left(\frac{V_{B'C'}}{m_{cr}V_T}\right), \qquad Q_{pT} = Q_{p0} + h_{jEi}Q_{jEi} + h_{jCi}Q_{jCi} + h_f Q_f + h_r Q_r, \qquad Q_f = \tau_f i_{Tf}, \qquad Q_r = \tau_r i_{Tr},$$

$$Q_{jEi} = \frac{C_{jEi0}V_{DEi}}{1-z_{Ei}}\left(1-\left(1-\frac{V_{B'E'}}{V_{DEi}}\right)^{1-z_{Ei}}\right), \qquad Q_{jCi} = \frac{C_{jCi0}V_{DCi}}{1-z_{Ci}}\left(1-\left(1-\frac{V_{B'C'}}{V_{DCi}}\right)^{1-z_{Ci}}\right)$$

with bias-independent forward (τ_f), reverse transit times (τ_r), zero-bias hole charge (Q_{p0}), and partitioning factor (α).

(i) Find the expression of transconductance. (ii) Draw the corresponding small-signal EC model with proper expressions for all circuit elements. (iii) Write down the Verilog-A code (load statements) for the large-signal ECs shown in Figs. 1 and 2 considering that the sub-circuits in Fig. 2 are used to model delayed (NQS) forward transfer current.

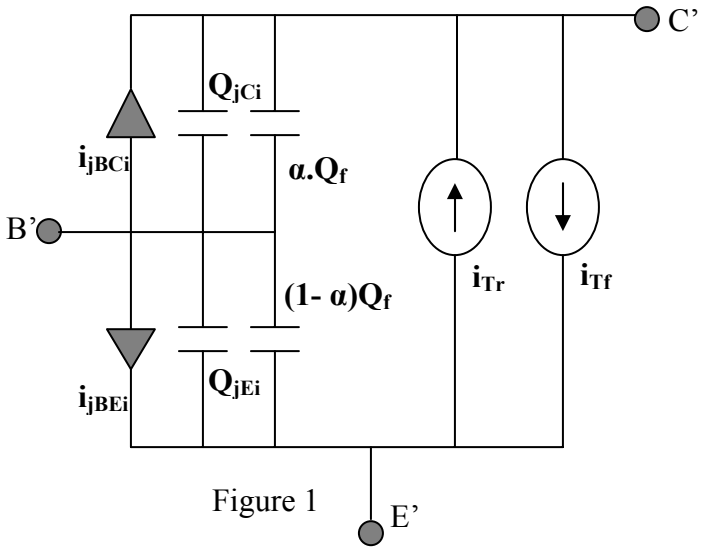

Figure 1

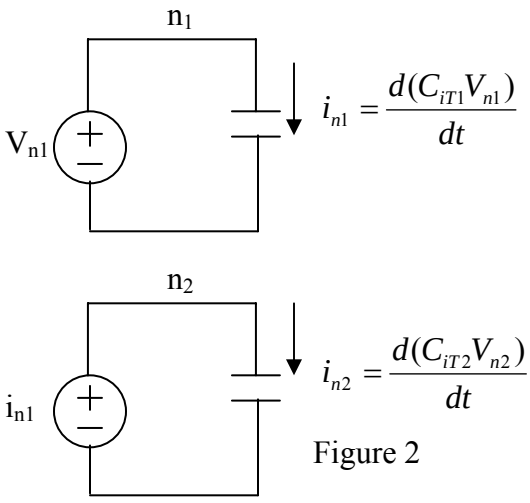

Figure 2

8.6. In a transistor, if measured small-signal parameters at a fixed operating point and f=5GHz are found to be C_{11}= 0.5nF, C_{21}= 0.2nF, r_{11}= 10Ω, and r_{21}= 5Ω, find out its operating point cut-off frequency, f_T.

8.7. If the simulation time is proportional to (n^3+e), where n and e are the number of nodes and number of circuit elements, respectively, for the following cases find out the percentage increase of simulation time with respect to the time required to simulate the QS EC model of Fig. 3 excluding the trans-charge element (-$\alpha.Q_f$): (i) include trans-capacitance effect, (ii) include NQS effect for transfer current using an LCR sub-circuit and minority charge using CR sub-circuit.

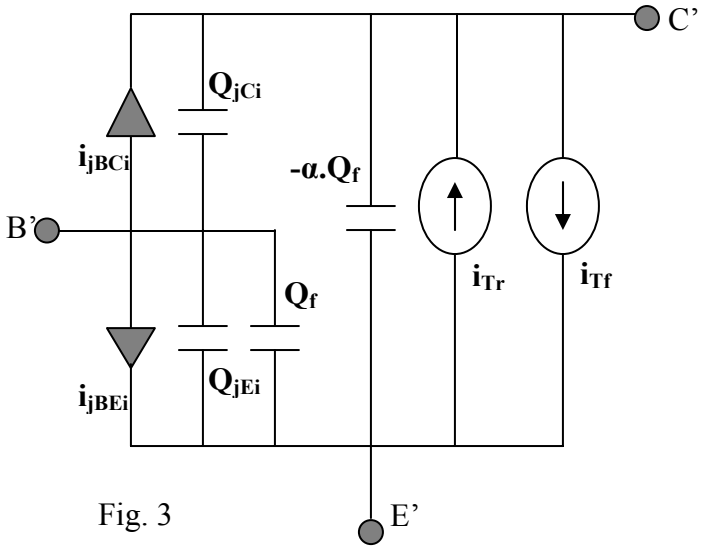

Fig. 3

Assignment-9

All questions are straightforward and one can answer them by carefully attending the class-lectures.

9.1. Draw the small-signal EC of 1D BJT including the noise sources. How will it appear with the input referred noise sources?

9.2. In terms of noise currents and noise voltages, what is the relation of the two circuit configurations (mentioned in Q9.1) that differ only from the perspective of noise sources? What is the relation from the perspective of the noise power spectral densities?

9.3. Express the transfer matrix (obtained in Q9.2) in terms of the small-signal EC elements of the transistor. Compute the input referred noise currents and noise voltages in terms of the small-signal EC elements of the transistor.

9.4. Considering the small-signal quasi-static operation, explain an implementation of noise sources in Verilog-A assuming (a) no correlation between the input and output noise sources and (b) correlation between the input and output noise sources due to charge partitioning effect.

9.5. Considering the small-signal non-quasi-static operation, explain an implementation of noise sources in Verilog-A assuming (a) no correlation between the input and output noise sources and (b) correlation between the input and output noise sources due to charge partitioning effect.

Assignment-10

All questions are straightforward and one can answer them by carefully attending the class-lectures.

10.1. Express the PSDs of the input referred noise sources, v_n and i_n in terms of the small-signal y-parameters and the PSDs of the base and collector current shot noise sources, i_{nb} and i_{nc}, of 1D BJT. Find the expressions of the C_A matrix elements in terms of the small-signal y-parameters and the base and collector current shot noise sources.

10.2. Derive the noise parameters, such as equivalent noise resistance (R_n), minimum noise factor (F_{min}), and the optimum source admittance ($Y_{S,opt}$) in terms of the C_A matrix elements.

10.3. Express the noise parameters in terms of the small-signal y-parameters and the PSDs of the base and collector current shot noise sources for a small-signal quasi-static operation assuming (a) there is no correlation between the base and collector current shot noise sources, (b) correlation between the base and collector current shot noise sources due to the charge partitioning effect.

10.4. Redo the Q10.3 in case of small-signal non-quasi-static operation.

10.5. If the input referred noise current source, i_n is decoupled further into i_{nu} and i_{nc}, so that there is no correlation between the input referred voltage noise source, v_n and i_{nu}, whereas the v_n and i_{nc} are fully correlated via correlation admittance Y_c, and the relation reads $i_n = i_{nu} + Y_c v_n$. Find the expressions of $Y_{S,opt}$ and F_{min} in terms of G_u, R_n, G_c and B_c where G_u refers to the conductance corresponding to the thermal noise PSD equated with the PSD of i_{nu} (i.e., $4kTG_u=S_{inu}$), R_n is the equivalent noise resistance, and G_c (B_c) is the real (imaginary) part of Y_c.

Sample Quiz problems:

Q1. (a) Draw a flow diagram for electrons and holes within an n-p-n transistor that considers ONLY the following two components of the base current: recombination within the neutral base region and the avalanche generation within the base-collector space-charge-region.
(b) Since the avalanche generation increases with collector-base voltage (V_{CB}), the base current is affected with increasing V_{CB}. Plot the V_{CB}-dependent base current.

Q2. (a) For an n-p-n transistor, in case of a fully depleted collector, derive the expression for critical current, I_{CK} as a function of internal collector voltage, V_{ci}.
(b) Calculate the value of I_{CK} at $V_{B'E'}$=0.85V and $V_{B'C'}$=-2.5V using the following parameter values: r_{Ci0}=100Ω, E_{lim}=25kV/cm, w_{Ci}=0.5μm, $N_{Ci}=10^{16}/cm^3$, V_{CEs}=0.05V, and $\varepsilon_{Si}=100x10^{-14}$F/cm.

Q3. Draw the small-signal equivalent circuit of 1D n-p-n BJT. At f=1GHz, $V_{B'E'}$=0.8V and $V_{B'C'}$=-2V, if the small-signal y-parameters are found to be, y_{11}=0.0039+j0.18, y_{21}=0.3861-j0.05, calculate the value of the minority charge partitioning factor, k_c. Given the model parameter values: C_{jEi0}=10pF, V_{DEi}=0.85V, z_{Ei}=0.25, C_{jCi0}=10pF, V_{DCi}=0.7V, z_{Ci}=0.33.

Q4. (a) A 1D n-p-n BJT is biased in a forward active mode at room temperature when I_C=2mA, τ_{mS}=100ps (total delay associated with minority carrier), τ_{BC}=50ps (electron transport delay through the base-collector space charge region which extends mainly in the collector side), C_{jEi}=10pF, and C_{jCi}=5pF. Assuming that the collector is fully depleted, calculate the unity gain cut-off frequency at the given bias condition.

(b) Draw the energy band diagram for an n-p junction made between n-SiGe and p-Si systems. Note that the Ge mole fraction is linearly graded from 25% (deep in the n-side) to 0% (at the metallurgical n-p junction).

Q5. (a) Draw the main large-signal equivalent circuit (EC) model of a 1D n-p-n BJT including the as minimum as possible sub-circuits to consider the NQS effects for which the corresponding small-signal y_{21} and y_{11} are given as

$$y_{11}(\omega)=g_{BEi}+g_{BCi}+j\omega\left(C_{jEi}+C_{jCi}\right)+\frac{j\omega\tau_f g_{m0}}{1+jA_{Q1}\omega\tau_f+A_{Q2}\left(\omega\tau_f\right)^2},$$

$$y_{21}(\omega)=\frac{g_{m0}\left(1-j\alpha A_{Q1}\omega\tau_f-A_{Q2}\alpha\left(\omega\tau_f\right)^2\right)}{1+jA_{Q1}\omega\tau_f+A_{Q2}\left(\omega\tau_f\right)^2}-g_{BCi}-j\omega C_{jCi}.$$

(b) Write the Verilog-A code (load statements) for the above-mentioned complete large-signal EC model.

(c) How will you extract the model parameters, A_{Q1} and A_{Q2}?

Q6. A simplified small-signal equivalent circuit of internal BJT is given in Fig. Q6.
(a) If C_{BE} =2C_{BC} and part of the collector current also flows through C_{BC}, find out the expression for the load resistance, R_l required for maximum power transfer to the output load. If C_{BE}=2C_{BC}=10nF, calculate the room-temperature value of R_l at a collector current, i_C=10mA at f=10MHz.
(b) If C_{BC} is negligible compared to C_{BE} and negligible collector current flows through C_{BC}, find out the expression for f_{max} and calculate f_T and f_{max} values for r_B=100Ω, C_{BE}=10nF and C_{BC}=100pF at i_C=10mA.

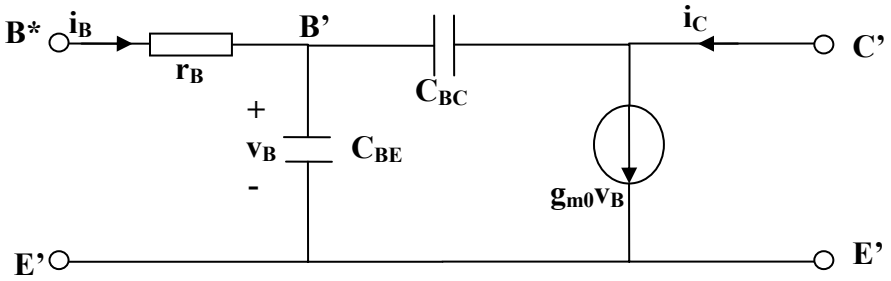

Fig. Q6: Equivalent circuit for Q6.

Q7. Time domain large-signal model equations for the input and output non-quasi-static effects in a 1D BJT are given as (with usual meaning of the variables)

$$\frac{d\left(A_Q\tau_f Q_f\right)}{dt}+Q_f=Q_{f0},\quad Q_{fC}=Q_f-\frac{d\left(\alpha A_Q\tau_f Q_f\right)}{dt},\quad i_T=i_{T0}-\frac{d\left(k_c Q_{fC}\right)}{dt}.$$

(a) Using as minimum as possible extra sub-circuit(s), discuss an implementation of the model clearly showing the equivalent circuit of the main 1D transistor model and the extra sub-circuit(s).
(b) Also write down the Verilog-A code (load statements) of the corresponding implementation.
(c) If $Q_{fC}(t) = Q_f(t - \alpha\tau_f)$, discuss the implementation using proper sub-circuits.

Q8. (a) Draw the small-signal equivalent circuit model of a 1D n-p-n BJT including as minimum as possible sub-circuits for which the corresponding common-emitter small-signal two-port y-parameters are given as (with the usual meaning of the variables):

$$y_{11}(\omega)=g_{BEi}+j\omega\left(C_{jEi}+C_{jCi}\right)+j\omega\tau_f g_{m0}+A_Q\omega^2\tau_f^2 g_{m0},$$

$$y_{21}(\omega)=g_{m0}-j\omega C_{jCi}-k_c j\omega\tau_f g_{m0},$$

$$y_{12}(\omega)=-j\omega C_{jCi},\ y_{22}(\omega)=g_0+j\omega C_{jCi}.$$

(b) If the noise PSD matrix for this 1D n-p-n BJT is given as

$$\begin{bmatrix} S_{i_{nb}i_{nb}^*} & S_{i_{nb}i_{nc}^*} \\ S_{i_{nc}i_{nb}^*} & S_{i_{nc}i_{nc}^*} \end{bmatrix} = \begin{bmatrix} 4k_BT\Re\{y_{11}\} - 2qI_B & 2k_BT\left(y_{21}^* + y_{12} - g_{m0}\right) \\ 2k_BT\left(y_{21} + y_{12}^* - g_{m0}\right) & 2qI_C \end{bmatrix},$$

find a suitable solution for the implementation of the shot noise sources in circuit simulator using proper equivalent circuits.
(c) Write down the Verilog-A code (load statements) for the derived noise model.

Q9. Under equilibrium condition, draw the energy band diagrams of the SiGe HBTs for which the doping profiles are identical and given in Fig. Q9 (a) and three different Ge mole fractions given in Figs. Q9(b), (c) and (d). Comment on the usefulness of each Ge profile.

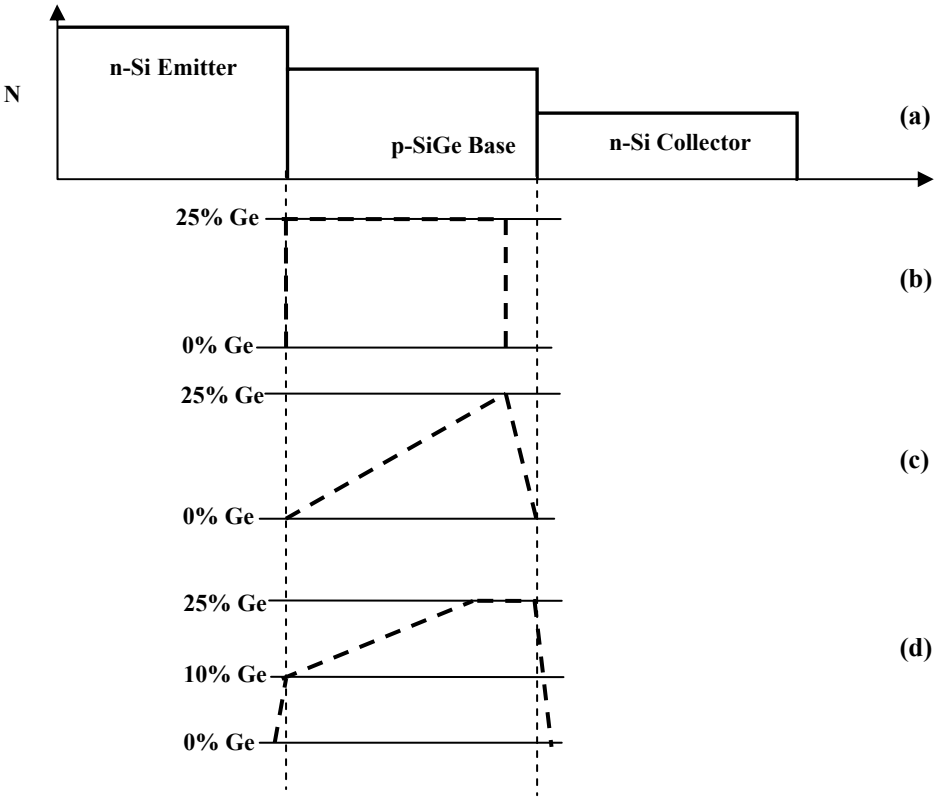

Fig. Q9: Doping and Ge mole fraction for Q9.

Q10. (a) At room temperature and at a sufficiently high current operating condition of a 1D n-p-n BJT, the common-emitter small-signal y_{11} and y_{21} at f=1GHz (quasi-static regime) are given as y_{11}=0.0039+j0.18, y_{21}=0.39. Assume that the associated base and collector current shot noise sources are uncorrelated. At the same operating condition, calculate
(a) the equivalent noise resistance (R_n), and
(b) correlation coefficient between the input referred current and voltage noise sources, i_n and v_n.

(c) If the input referred noise current source, i_n is decomposed into i_{nu} (uncorrelated with v_n) and $i_{nc}=Y_c v_n$ (fully correlated with v_n), calculate the value of Y_c and the optimum source susceptance ($B_{S,opt}$) in this operating condition.