Design and Performance Evaluation of Sub-Systems of Grid-Connected Inverters

A thesis
submitted for the degree of
Doctor of Philosophy
in the Faculty of Engineering

By
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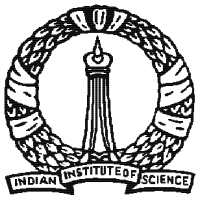

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To my school teachers...

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Abstract

Grid-connected inverters have wide application in the field of distributed generation and power quality. As the power level demanded by these applications increase, the design and performance evaluation of these converters become important. In this thesis, this is considered from the perspective of power quality, efficiency, thermal performance evaluation, reliability and control performance evaluation.

The first part of the work focuses on passive damping network design for LCL filters of grid-connected inverters. Passive damping is considered as it is simple and more reliable. The work explores a split-capacitor resistive-inductive (SC-RL) passive damping scheme for use in high power applications. A method for component selection for the SC-RL scheme that minimises the power loss in the damping resistors while keeping the system well damped is proposed. Analytical results show the losses and quality factor to be in the range of 0.05-0.1% and 2.0-2.5 respectively, which are validated experimentally.

In the second part of the work, a test method to evaluate the thermal performance of the semiconductor devices of a three-phase grid-connected inverter is proposed. Semiconductor device junction temperatures have to be maintained within datasheet specified limits to avoid failure in power converters. Thermal time constants can be large and inverters need to be run for long durations during thermal tests. This consumes a lot of energy and requires sources and loads that can handle high power. The proposed method eliminates the need for high power sources and loads. Only energy corresponding to the losses in the test configuration is consumed. The capability of the method to evaluate the thermal performance of the dc bus capacitors and the output filter components of the inverter has also been studied. The method has been experimentally validated for a 4-wire configuration that uses sine-triangle pulse width modulation and a 3-wire configuration that uses conventional space vector pulse width modulation.

In the third part of the work, a test set-up to evaluate the control performance of grid-connected inverters has been developed. Grid standards require high power grid-connected inverters to remain connected to the grid under short time grid disturbances like voltage sags, voltage swells and the like. To test the grid-connected inverter for proper operation under these disturbances, it is required to re-create them in a controlled manner in the testing laboratory. A back-to-back connected three-phase inverter has been programmed as a hardware grid simulator for this purpose. A novel disturbance generation algorithm has been developed, analysed and implemented in digital controller using finite state machine model for control of the grid simulator. A wide range of disturbance conditions can be created using the developed algorithm. Experimental tests have been done on a linear purely resistive load, a non-linear diode-bridge load and a current-controlled inverter load to validate the programmed features of the grid simulator.

In the present work, a 50 kVA three-phase back-to-back connected inverter with output LCL filter is built to study design and performance aspects of subsystems of grid-connected inverters. The various contributions in the work can be used to improve the reliability and performance of grid-connected inverters.

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Acronyms

ADC	Analog to Digital Converter
APF	Active Power Filter
CM	Common Mode
CSVPWM	Conventional Space Vector Pulse Width Modulation
DM	Differential Mode
DSP	Digital Signal Processor
DSTATCOM	Distribution STATic synchronous COMpensator
DVR	Dynamic Voltage Restorer
EMI	Electro Magnetic Interference
ESR	Equivalent Series Resistance
FEC	Front End Converter
FSM	Finite State Machine
HF	High Frequency
HFCM	High Frequency Common Mode
HFDM	High Frequency Differential Mode
HVRT	High Voltage Ride-Through
IEC	International Electro-technical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bi-polar Transistor
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LF	Low Frequency
LFCM	Low Frequency Common Mode
LFDM	Low Frequency Differential Mode

LUT	Leg Under Test
LVRT	Low Voltage Ride-Through
PCC	Point of Common Coupling
PI	Proportional Integral
PLL	Phase Locked Loop
PR	Proportional Resonant
PWM	Pulse Width Modulation
QF	Quality Factor
SC-R	Split-Capacitor Resistive damping
SC-RL	Split-Capacitor Resistive-Inductive damping
SOGI	Second Order Generalized Integrator
SRF-PLL	Synchronous Reference Frame Phase-Locked Loop
STATCOM	STATic synchronous COMpensator
SUT	System Under Test
SVC	Static Var Compensator
TCR	Thyristor Controlled Rectifier
TDD	Total Demand Distortion
THD	Total Harmonic Distortion
TRD	Total Rated current Distortion
UPF	Unity Power Factor
UPQC	Unified Power Quality Conditioner
UPS	Uninterrupted Power Supply
VSI	Voltage Source Inverter

Nomenclature

$\Delta\omega$	Control frequency output from PLL controller (rad/s)
ω	Grid frequency (rad/s)
ω_{base}	Base value for radian frequency (rad/s)
ω_d	Resonance frequency of the LCL filter with damping components included (rad/s)
ω_{dom}	Frequency of the dominant harmonic in the inverter output voltage spectrum (rad/s)
ω_{ff}	Grid frequency feed-forward (rad/s)
ω_{fu}	Fundamental grid frequency (rad/s)
ω_p	LCL filter parallel resonance frequency (rad/s)
ω_r	Natural frequency of oscillation of the LCL filter (rad/s)
ω_s	LCL filter series resonance frequency (rad/s)
ω_{sw}	Switching frequency (rad/s)
ϕ	Power factor angle at the point of common coupling with the grid (rad)
ψ	Power factor angle at the output terminal of the inverter (rad)
θ	Grid phase angle (rad)
θ^*	Desired phase angle at which the disturbance is to be triggered (rad)
a_C	Ratio C_d/C_1 (no unit)
a_L	Ratio L_1/L_2 (no unit)
C	Capacitor of the inverter output LCL filter (F)
C_1	Switching ripple by-pass capacitor of the LCL filter (F)
C_{base}	Base value for capacitance (F)
C_d	Damping branch capacitor of the LCL filter (F)
C_{DC}	DC bus capacitance (F)

C_{max}	Maximum acceptable value of capacitance C based on constraint on the reactive current drawn by the filter capacitor (F)
$cos\theta$, $sin\theta$	Cos and sin unit vectors (no unit)
C_R, C_Y, C_B	Output filter capacitance for the three phases (F)
d	Duty ratio ($= t_{on}/T_{sw}$) (no unit)
$D(t)$	Instantaneous duty ratio of top IGBT
$D'(t)$	Instantaneous duty ratio of bottom Diode
$D_R(t)_{act}$, $D_Y(t)_{act}$, $D_B(t)_{act}$	Instantaneous duty ratios of the top IGBTs of three phases at steady state in the actual system
$D_R(t)_{test}$,$D_Y(t)_{test}$, $D_B(t)_{test}$	Instantaneous duty ratios of the top IGBTs of three phases at steady state in the test configuration
E_{off}	Turn-off energy dissipation in IGBT (J)
E_{on}	Turn-on energy dissipation in IGBT (J)
E_{rr}	Turn-off energy dissipation in diode (J)
f_{fu}	Fundamental frequency (Hz)
f_r	Resonance frequency (Hz)
f_{sw}	Switching frequency (Hz)
h	Harmonic order (no unit)
$\Im$	Operator meaning 'Imaginary part of'
$i(t)$	Instantaneous inverter output current (A)
I_{base}	Base value for current (A)
i_{cap}	DC bus capacitor current (A)
$i_{cm}(t)$	Instantaneous inverter output per-phase common mode current (A)
i_{cm}^{fu}	Fundamental component of per-phase common mode current (A)
i_{cm}^{ri}	Ripple component of per-phase common current (A)
i_d, i_q	d and q components of current (A)
I_D	rms value of highest fundamental demand current (15 or 30 minute demand) (A)
I_{dc}	Average current on the dc side of the inverter (A)
i_g	Grid side inductor current in a LCL filter (A)
I_h	rms value of h^{th} harmonic component of current (A)
i_i	Inverter side inductor current in a LCL filter (A)

i_{L_d}	Current through the damping inductor L_d (A)
i_{link}	DC link current (A)
I_m	Peak value of inverter output current (A)
i_q^*	q-axis current reference (A)
i_r	Instantaneous R-phase grid current (A)
i_R, i_Y ,i_B	Instantaneous current through the grid side inductors of the three phase output LCL filter (A)
I_R	rms value of fundamental rated current of the equipment or unit under study (A)
$\mathbf{I_R}$, $\mathbf{I_Y}$, $\mathbf{I_B}$	Phasors representing the fundamental frequency three-phase grid-side output currents of the inverter (A)
i_{R_d}	Current through the damping resistor R_d (A)
$i_{R,dm}$, $i_{Y,dm}$, $i_{B,dm}$	Differential mode components of the three-phase currents i_R, i_Y and i_B (A)
$\overline{I}_{R,rated}$	Current phasor of the R-phase inverter rated output current (A)
i_{rated}	Rated per-phase inverter current (A)
i_{R_i}, i_{Y_i}, i_{B_i}	Instantaneous three-phase currents at the inverter output terminal (A)
$i_{R_i,dm}(t)$	Instantaneous R-phase inverter output differential mode current (A)
i_{rms}	rms per-phase inverter current (A)
i_{test}	Current at which datasheet parameters has been taken (A)
$i_{Y,dm}^*$, $i_{B,dm}^*$	Y and B phase set reference differential mode inverter output currents (A)
$\jmath$	Imaginary math operator
K_i	Gain of the integral controller
$K_{I,diode}$	Exponent for current dependency of diode reverse recovery loss (no unit)
K_{L_d}	Damping impedance factor ($= R_d/\omega_{fu} \cdot L_d$) (no unit)
K_p	Gain of the proportional controller
K_r	Gain of the resonant controller
K_{rn}	Gain for the n^{th} harmonic controller in multi-resonant control
$K_{V,diode}$	Exponent for voltage dependency of diode reverse recovery loss (no unit)

$K_{V,IGBT}$	Exponent for voltage dependency of IGBT switching loss (no unit)
L	Front-end converter input filter inductance in the grid simulator (H)
L	Total inductance of the inverter side and grid side inductors (H), $L = L_1 + L_2$
L_1	Inverter side inductor of the inverter output LCL filter (H)
L_2	Grid side inductor of the inverter output LCL filter (H)
L_{base}	Base value for inductance (H)
L_d	Damping inductor of the LCL filter (H)
L_{max}	Maximum value of L (H)
L_{min1}	Minimum required L value (H)
L_{min2}	Minimum required L value (H)
L_p	Parallel inductance of L_1 and L_2 (H), $L_p = L_1L_2/(L_1 + L_2)$
L_R	R-phase output LC filter inductance (H)
L_R, L_Y, L_B	Three phase combined inductances ($L_1 + L_2$) of the inverter output filter (H)
L_{R1}, L_{Y1}, L_{B1}	Inverter-side output filter inductance for the three phases (H)
L_{R2}, L_{Y2}, L_{B2}	Grid-side output filter inductance for the three phases (H)
m	Modulation index
m_{act}	Modulation index in the actual system (no unit)
m_{test}	Modulation index in the test configuration (no unit)
N_g	Neutral connection of the grid
O	Mid-point of the dc bus
$P(\phi)$	Total power loss in a three-phase inverter at a given power factor angle ϕ (W)
P_{base}	Base value for three-phase power (W)
$p_{cm}(t)$	Instantaneous ac side power due to common mode voltages and currents in the three-phase output (W)
$p_D(t)$	Instantaneous conduction loss in diode (W)
P_{D_cond}	Average conduction loss in diode (W)
P_{D_rr}	Average reverse recovery loss in diode (W)
$p_{D,rr}(t)$	Instantaneous reverse recovery loss in diode (W)
$p_{dm}(t)$	Instantaneous ac side power due to differential mode voltages and

	currents in the three-phase output (W)
P_{fu}	Power loss in the damping resistor due to the fundamental frequency component of current (W)
P_m	Peak value of sinusoidal component of total power loss in a three-phase inverter for varying power factor angle ϕ (W)
P_{Mod_term}	Power loss per module due to terminal lead resistance (W)
P_o	Average value of total power loss in a three-phase inverter for varying power factor angle ϕ (W)
P_{rated}	Rated three-phase power (W)
P_{ri}	Power loss in the damping resistor due to the switching ripple component of current (W)
$p_S(t)$	Instantaneous conduction loss in IGBT (W)
P_{S_cond}	Average conduction loss in IGBT (W)
P_{S_sw}	Average switching loss in IGBT (W)
$p_{S,sw}(t)$	Instantaneous switching loss in IGBT (W)
P_T	Total power loss in the damping resistor ($= P_{fu} + P_{ri}$) (W)
$\Re$	Operator meaning 'Real part of'
R, Y, B	Load terminals of the grid simulator output inverter
$R_{CC'+EE'}$	Parasitic terminal-to-terminal ohmic resistance (Ω)
r_{CE}	On-state resistance of IGBT (Ω)
R_d	Damping resistance (Ω)
r_F	On-state resistance of diode (Ω)
R_f, Y_f, B_f	Three-phase ac input terminals of grid simulator front-end converter
R_g, Y_g, B_g	Three-phase terminals of the grid
$R_{g,on}$	Gate turn-on resistance (Ω)
$R_{g,off}$	Gate turn-off resistance (Ω)
R_i, Y_i, B_i	Three-phase ac terminals of the output inverter
R_R	Resistance associated with the R-phase output LC filter inductor (Ω)
R_R, R_Y, R_B	Resistances associated with the three-phase inverter output filter inductors L_1 and L_2 (Ω)
$R_{th,c-h}$	Case to Heatsink thermal resistance including heatsink paste ($^oC/W$)
$R_{th,h-a}$	Heatsink to ambient thermal resistance ($^oC/W$)

$R_{th,j-c,Diode}$	Junction to case thermal resistance of diode ($^oC/W$)
$R_{th,j-c,IGBT}$	Junction to case thermal resistance of IGBT ($^oC/W$)
$S_R(t)$,$S_Y(t)$,$S_B(t)$	Instantaneous switch status of the top IGBTs of the three-phase legs
TC_{Err}	Temperature co-efficient of diode reverse recovery loss ($1/^oC$)
TC_{Esw}	Temperature co-efficient of IGBT switching loss ($1/^oC$)
t_{dis}	Duration of the disturbance (s)
t_{idle}	Duration of idle state between successive disturbances (s)
T_j	Junction temperature at which datasheet parameters have been specified (^oC)
$T_{j,diode}$	Operating junction temperature of the diode (^oC)
$T_{j,IGBT}$	Operating junction temperature of the IGBT (^oC)
t_{on}	Time period for which the top switch of a inverter leg is 'ON' in a given switching time period (s)
T_{ref}	Reference junction temperature at which the the datasheet parameters have been taken (^oC)
T_{smpl}	Sampling time period used for analytical discrete-time computation
T_{sw}	Switching time period of the pulse-width modulated output voltage in the inverter (s)
V_1	Steady state dc voltage output of diode bridge
$v(t)$	Instantaneous inverter terminal voltage w.r.t dc bus mid-point 'O' (V)
v_α, v_β	Orthogonal components of grid voltage (V)
V_{base}	Base value for voltage (V)
v_C	Voltage across the capacitor branch in a LCL filter (V)
v_{cap}	Instantaneous voltage across the LCL filter capacitor in R passive damping (V)
V_{CE0}	Collector-Emitter threshold voltage of IGBT (V)
$\overline{V}_{cm}$	Phasor representing the common mode voltage (V)
$v_{cm,3}$	Third harmonic component of common mode voltage (V)
$v_{cm}(t)$	Instantaneous inverter output common mode voltage (V)
v_{cm}^{fu}	Fundamental component of common mode voltage (V)
v_{cm}^{ri}	Ripple component of common mode voltage (V)
v_{comp}	Compensating voltage from the dynamic voltage restorer (V)

v_d	Voltage across the damping branch capacitor C_d (V)
v_d, v_q	dq components of grid voltage (V)
V_{dc}	Operating dc bus voltage of the inverter (V)
$V_{dc,reduced}$	Reduced dc bus voltage at which the dc bus capacitor test is performed (V)
$V_{dc,test}$	DC bus voltage at which datasheet parameters has been taken (V)
V_{dc}^*	DC bus voltage reference (V)
V_{dis}	Grid voltage during disturbance (V)
V_{F0}	Threshold voltage of diode (V)
V_{fu}	rms value of fundamental frequency component of voltage (V)
v_g	Grid voltage (V)
v_{grid}	Instantaneous single phase grid voltage (V)
V_h	rms value of h^{th} harmonic component of voltage (V)
v_i	Inverter output voltage (V)
v_{load}	Voltage at the load terminals (V)
v_{L_R}, v_{L_Y}, v_{L_B}	Three-phase voltage drops across the output filter inductors (V)
$\mathbf{V_{L_R}}$, $\mathbf{V_{L_Y}}$, $\mathbf{V_{L_B}}$	Fundamental frequency voltage phasors representing the voltage drop across the output inductors in the three-phases (V)
V_m	Peak grid voltage (V)
V_{nom}	Nominal grid voltage (V)
v_q^*	q-axis grid voltage reference (V)
v_r	Instantaneous R-phase grid voltage (V)
$\overline{V_R}$	Voltage phasor of the R-phase inverter output voltage (V)
$\overline{V}_{R,dm}$	Phasor representing the R-phase differential mode voltage (V)
$\overline{V}_{R,rated}$	Voltage phasor of the R-phase inverter rated output voltage (V)
v_{R_g}, v_{Y_g}, v_{B_g}	Three-phase grid voltages (V)
$\mathbf{V_{R_g}}$, $\mathbf{V_{Y_g}}$, $\mathbf{V_{B_g}}$	Three phase fundamental frequency grid voltage phasors (V)
$\mathbf{V_{R_i}}$, $\mathbf{V_{Y_i}}$, $\mathbf{V_{B_i}}$	Three phase fundamental frequency inverter output voltage phasors (V)
$v_{R_iO}(t)$, $v_{Y_iO}(t)$, $v_{B_iO}(t)$	Instantaneous three-phase inverter output voltages (V)
$v_{R_iO,dm}$, $v_{Y_iO,dm}$, $v_{B_iO,dm}$	Differential mode components of the inverter three-phase output voltages (V)

$v_{R_iO,dm}^{fu}$	Fundamental component of R-phase differential mode voltage (V)
$v_{R_iO,dm}^{ri}$	Ripple component of R-phase differential mode voltage (V)
$V_{ripple,pk-pk}$	Peak-to-peak low frequency voltage ripple in the dc bus (V)
v_{rms}	rms grid voltage (V)
$\mathbf{V_S}$	Fundamental frequency phasor representing the voltage at the shorted terminal of the test configuration w.r.t the dc bus mid-point 'O' (V)
$\overline{V_Y}$	Voltage phasor of the Y-phase inverter output voltage (V)
$\overline{V}_{Y,dm}$	Phasor representing the Y-phase differential mode voltage (V)
Z	Impedance (Ω)
Z_{base}	Base value for impedance (Ω)

List of Publications

1. Arun Karuppaswamy B, Vinod John, "A Hardware Grid Simulator to Test Grid-Connected Systems", in Proceedings of *National Power Electronics Conference 2010 (NPEC-2010), IIT Roorkee*, $10^{th} - 13^{th}$ June, 2010.

2. Balasubramanian, A.K., John, V, "Analysis and design of split-capacitor resistive-inductive passive damping for LCL filters in grid-connected inverters", *IET Power Electronics*, vol. 6, issue 9, pp.1822 - 1832, Nov. 2013.

3. Arun Karuppaswamy B, Srinivas Gulur, Vinod John, "A grid simulator to evaluate control performance of grid-connected inverters", *IEEE International Conference on Power Electronics, Drives and Energy Systems*, $16^{th} - 19^{th}$ Dec, 2014.

4. Arun Karuppaswamy B, Vinod John, "A Thermal Test Method for High Power Three-Phase Grid-Connected Inverters", *IET Power Electronics. (Submitted)*

Chapter 1

Introduction

The last two decades has seen a phenomenal change in the way power is generated and utilised. The use of grid-connected inverters is on the increase both at the point of generation and utilisation. On the generation end, they are used to integrate renewable sources of power with the ac grid. On the utility end, they find use in power factor correction, mitigation of harmonics drawn from the grid and to improve the quality of voltage at the load terminals. In all the above applications, it must be ensured that the switching frequency ripple injected into the grid by the grid-connected inverter is within limits specified by the grid standards. This requires a properly designed filter at the output of the inverter. Further, the grid-connected inverter is expected to witness common grid disturbances like voltage sags, voltage swells and the like. It should have controls that ensure its operation under these disturbances. In this regard, the grid-connected inverters are expected to have good control performance. Also, the required power handling capabilities of the grid-connected inverters has increased and stands at a few MWs in the present day. This has necessitated research on general issues related to grid-connected inverters and on specific issues related to their operation at high power levels. As more of these converters are put to use, the research is towards making these inverters more reliable.

In this thesis, the focus of studies has been on issues related to grid-connected inverters and their operation at high power levels in the order of a few hundreds of kW and up into the MW range in the contexts mentioned above.

Section 1.1 discusses the topology of grid-connected inverter considered in this thesis and elaborates on its various applications. In Section 1.2, a survey of research in the area of grid-connected inverters is provided. The relevant standards are also listed. The scope of research in this thesis is discussed in Section 1.3. Section 1.4 provides the details of the

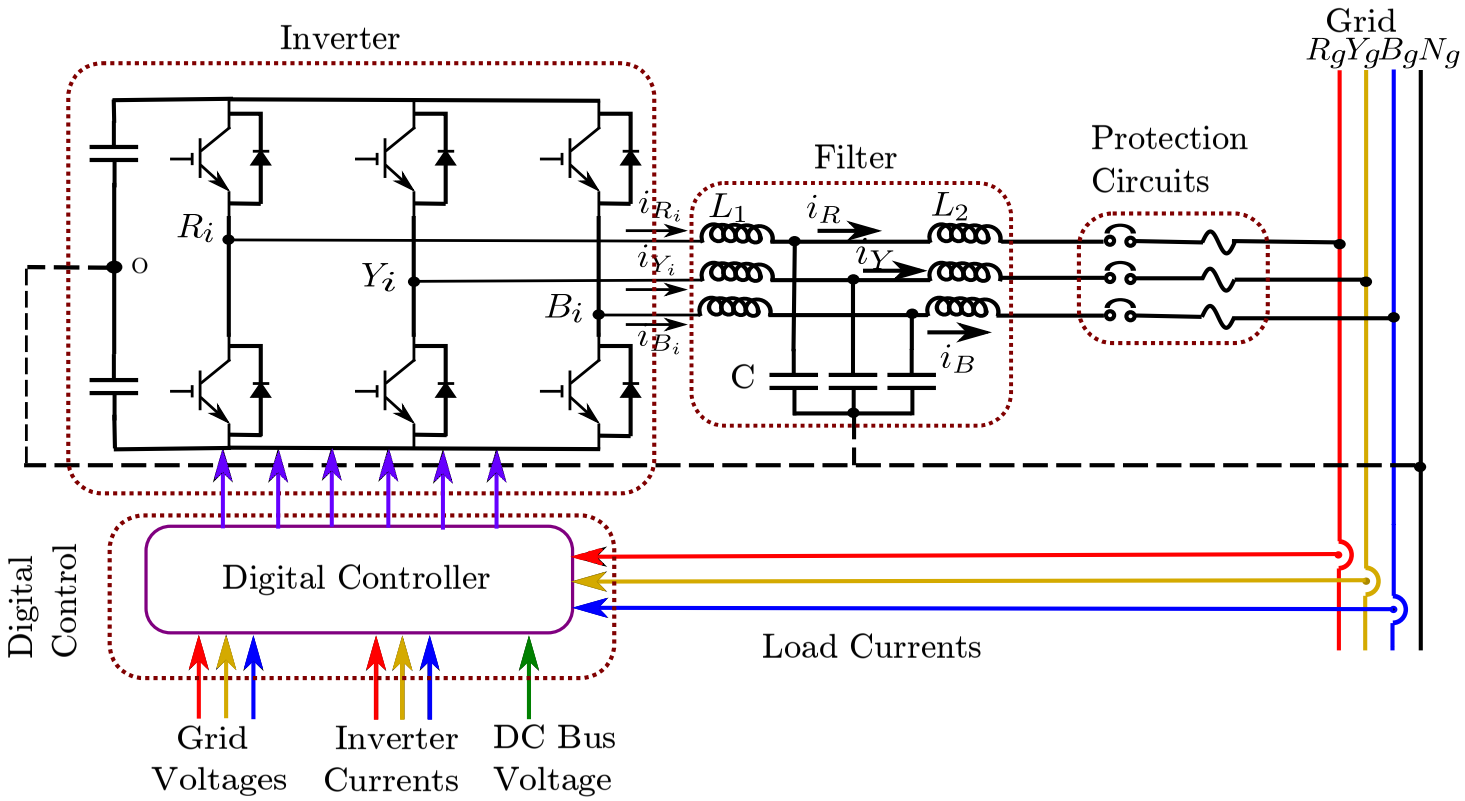


Figure 1.1: Grid-connected inverter. Solid lines indicate a 3-wire configuration and dashed lines indicate a 4-wire configuration. Control inputs depend on the application.

hardware set-up developed for the experimental evaluation. The organisation of the thesis is outlined in Section 1.5. Section 1.6 summarises the Chapter.

1.1 Grid-Connected Inverters

Fig. 1.1 shows a general configuration of a grid-connected inverter considered in this thesis. As shown, a two-level inverter configuration has been considered. Both 3-wire shown in solid lines and 4-wire configuration shown in dashed lines have been considered. The exact inputs for the digital control will depend on the application.

Application	**Examples**
Power Quality	a) STATic synchronous COMpensator (STATCOM) b) Active Power Filter (APF) c) Dynamic Voltage Restorer (DVR) d) Unified Power Quality Conditioner (UPQC)
Distributed Generation	a) Solar b) Wind c) Fuel Cells
Front End Conversion	a) Electric traction b) Electric motor drives

Table 1.1: Applications of Grid-Connected Inverters.

1.1.1 Applications

The simple configuration shown in Fig. 1.1 has a wide variety of applications which makes it an important area of research in Power Electronics. The various applications have been listed in Table 1.1:

1.1.1.1 Power Quality Applications

The grid-connected inverter can be used in shunt or series with the grid to solve several power quality issues like power factor problems, voltage sags, voltage swells and harmonic issues. The various power quality applications are described in detail below.

STATic synchronous COMpensator (STATCOM) Fig. 1.2 shows a grid-connected inverter used as a STATCOM. In an application as a STATCOM [1, 2], the grid-connected inverter is connected in shunt to the grid. The STATCOM dynamically supplies the reactive power demanded by the load while only the real power is drawn from the grid. This reduces the transmission losses incurred in transferring reactive currents from the generation point to the load. Since the consumer is billed only for the real power drawn, the supplier usually restricts the reactive currents that can be drawn by specifying power factor limits. The superior dynamic performance of a STATCOM makes it more preferable than other power factor correction alternatives such as fixed capacitor banks and Static Var Compensators (SVCs).

Active Power Filter (APF) Fig. 1.3 shows an active power filter [3]. As can be observed, the active power filter or a shunt active filter has a similar inverter configuration as a STATCOM. The difference lies mainly in the control. The APF compensates for both the fundamental frequency reactive current and the harmonic frequency currents demanded by the load. While the STATCOM is useful for linear loads, the APF is more generic and can maintain the current drawn from the grid to be near sinusoidal and at near unity power factor for non-linear loads also.

Dynamic Voltage Restorer (DVR) Fig. 1.4 shows a dynamic voltage restorer [4,5]. As shown in the figure, the DVR is a series-connected inverter. The output voltage of the DVR, 'v_{comp}', is added in series with the grid voltage (v_g) through a series-injection transformer.

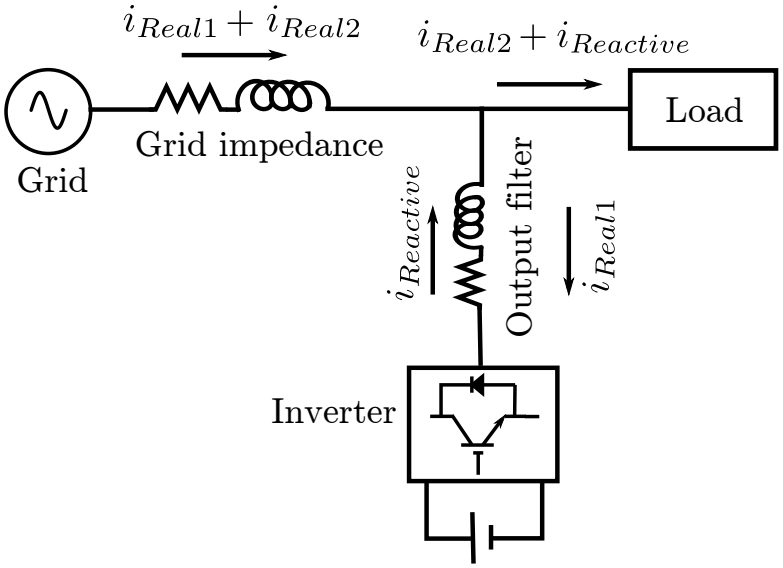


Figure 1.2: A STATCOM providing reactive power support to the load. The losses in transmitting the reactive current from the grid to the load terminal is reduced. The power factor is near unity for the fundamental frequency current drawn from the grid.

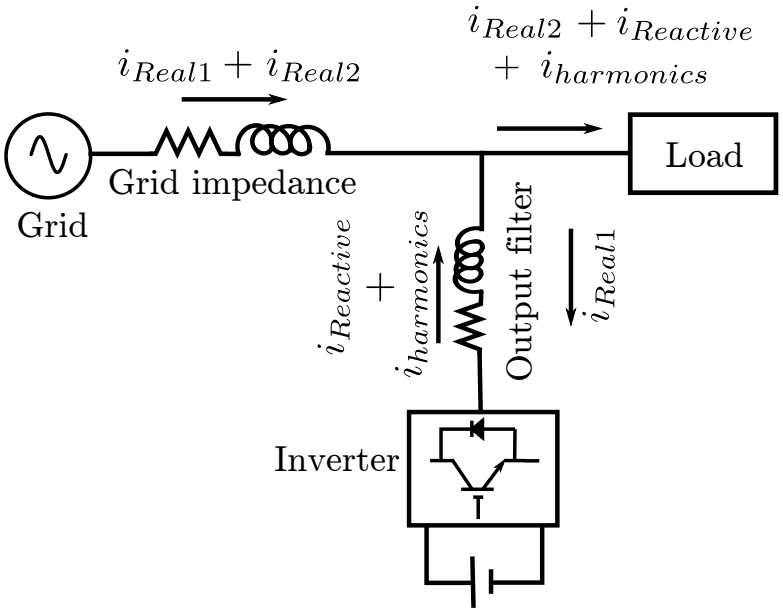


Figure 1.3: An active power filter providing reactive and harmonic current support to the load. The active power filter has the same topology as a STATCOM. The difference lies mainly in the control. The active power filter compensates for the fundamental frequency reactive current and the harmonic frequency current requirements of the load.

The DVR is used to maintain quality voltage (v_{load}) at the load terminals. It compensates for any voltage fluctuations in the grid and ensures a steady ac voltage at the load terminals. The DVR differs from an online uninterrupted power supply (UPS) which also can provide quality voltage. While an online UPS needs to be rated for the full load, a DVR is rated for a fraction of the full load as it compensates only for the deviation of the grid voltage from the nominal.

Unified Power Quality Conditioner (UPQC) Fig. 1.5 shows an unified power quality conditioner [6, 7]. As shown in the figure, the UPQC unifies the capabilities of an APF and a DVR. Besides maintaining the current drawn from the grid to be sinusoidal and at near unity power factor, the UPQC also maintains quality voltage at the load terminals by compensating for any deviations of the grid voltage from the nominal.

1.1.1.2 Distributed Generation Applications

Invariably, all distributed sources require a grid-connected inverter to interface to the grid [8]. The output voltage of the distributed sources are usually converted into a dc voltage that feeds the dc bus of the grid-connected inverter. The inverter transfers the power from the distributed source to the grid. This topology is required as the output voltage from the distributed sources are of varying nature. For example, considering solar, wind and fuel cells, solar panels and fuel cells give a dc output voltage while a wind power generator gives a variable frequency ac as the output. In all the three cases, an inverter is required for grid connection.

1.1.1.3 Front End Conversion (FEC) Applications

A FEC is used to draw power from the grid at near unity power factor [9]. The most common application of a FEC is in traction and in electric motor drives. In either application, the FEC charges and maintains a dc bus at a required dc voltage. In a traction application, the dc may be used directly or converted into an ac or lower dc voltage. In an electric motor drive application, an inverter is used to convert the dc voltage into an ac voltage of required frequency and magnitude to control an electric motor.

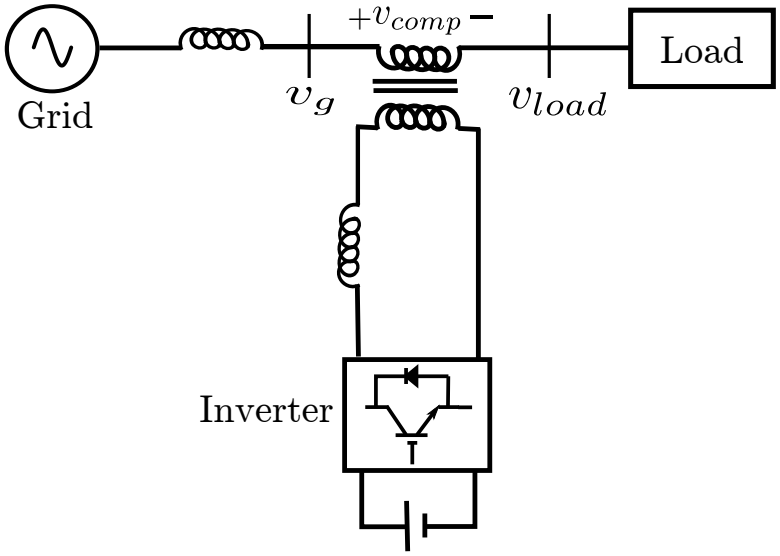


Figure 1.4: A dynamic voltage restorer (DVR) to maintain quality voltage (v_{load}) at the load terminal. The DVR compensates for the deviations in the grid voltage (v_g) by injecting a compensating voltage 'v_{comp}' in series with the grid voltage through a series injection transformer.

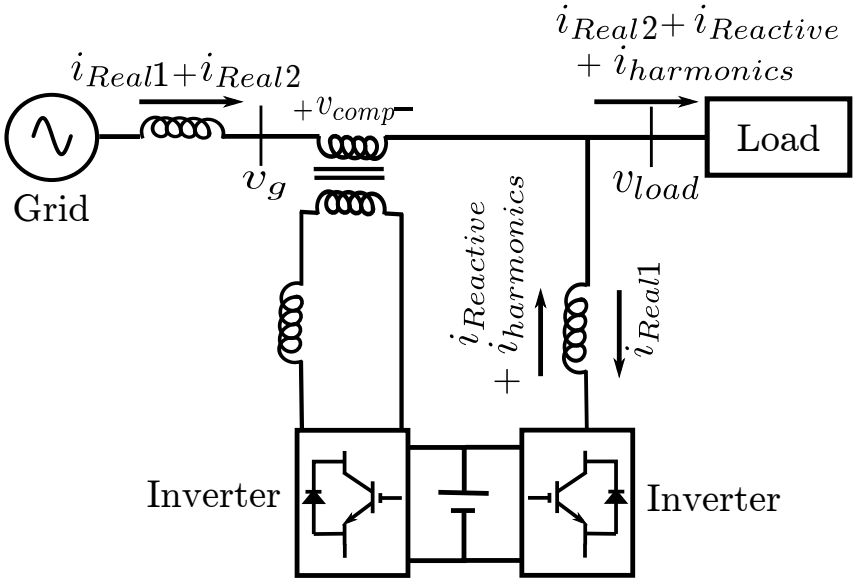


Figure 1.5: An unified power quality conditioner (UPQC). The UPQC unifies the capabilities of a APF and a DVR. Besides ensuring a sinusoidal near unity power factor current to be drawn from the grid, it maintains quality voltage at the load terminals.

1.2 Research in the Area of Grid-Connected Inverters: An Overview

The wide application of grid-connected inverters in recent years as elaborated in Section 1.1 has spurred research interest on inverters in general and grid-connected inverters in particular. The research primarily focuses on improving the reliability and performance of inverters. Also, issues related to integration of inverters to the grid and their operation at high power levels are of interest. Section 1.2.1 and Section 1.2.2 presents a survey of research in the field of grid-connected inverters. The increased inter-connection of inverter with the grid and the increasing power levels of these inverters have led to newer issues in the power grid. This has initiated the development of new standards to ensure the stability and voltage quality in the power grid. Section 1.2.3 discusses some standards relevant to grid-connected inverters. The research work in this thesis focuses on certain aspects listed in this Section, the details of which appears in Section 1.3.

1.2.1 Design Aspects

A survey of research on the design aspects of inverters when used as grid-connected converters is presented below:

1.2.1.1 Topology

A wide variety of inverter topologies have been explored in literature [10–15]. Both single phase [12, 14] and three phase topologies [10, 11, 13] have been presented. Four leg topology has been proposed [10] to eliminate the common mode voltage and for better utilisation of the dc bus. Multi-level inverters have been developed for use at medium voltage levels [13]. The use of multi-level inverters has the advantage of requiring a lower blocking voltage across the device during off-state and lower output voltage ripple [15]. Some of the topologies have been suggested specifically for grid integration of renewable sources [11,12,14]. The two-level inverter is the most commonly used topology of grid-connected inverters and is considered in this thesis.

1.2.1.2 DC Bus Capacitor Selection

The ripple currents at the dc link, the connecting link between the dc bus capacitors and the inverter IGBT modules, are supplied by the dc bus capacitors. The capacitance, ripple current rating and lifetime of the dc bus capacitors are dependent on various parameters such as the converter topology, modulation method, rating, operating dc bus voltage and the load. A proper selection of dc bus capacitors is essential to ensure reliability of the inverter. Reference [16] discusses the analytical computation of dc bus capacitor current to aid the selection of dc bus capacitors for two level inverters. Reference [17] discusses the same for a three level neutral point clamped inverter. Prediction of the lifetime of the dc bus capacitors is of practical importance for inverter manufacturers and has been presented in [18]. Analytical studies of current in dc bus capacitor can be used along with novel test method proposed in this thesis to validate the design of the dc bus capacitors.

1.2.1.3 Busbar and Snubber Design

Busbars are used in power converters to minimize the inductance in the path connecting the dc bus and the device terminals [19]. The inductance leads to voltage spikes across the IGBTs during switching. The voltage spikes can damage the device. Further, the dv/dt is a source of Electro Magnetic Interference (EMI) issues [20, 21]. The busbar design is based on the nature and magnitude of the current flowing in the busbar, the temperature rise of the bus plates and the power connections required at the modules and at the dc bus capacitors. Further, the busbar design should ensure the inductance to be within allowable limits. References [19, 20, 22] discuss some simple modelling techniques based on the busbar geometry to compute the inductance while [21, 23, 24] discuss more accurate methods based on electro-magnetics and finite element analysis. Some methods [21, 22, 24] in literature have been developed for specific topologies like three-level topologies.

Snubbers are required in IGBT based inverters especially at high power levels to reduce the stress on the device due to dv/dt, di/dt, over-voltage and short-circuit [25]. The main purpose of snubber is to absorb the energy in the busbar inductance during switching. The snubber provides an alternative path for the energy during switching thereby avoiding voltage spikes across the device terminals. Snubbers may be associated with power losses as most snubber topologies dissipate energy in resistors. Some designs attempt to lower this loss [26]. Some other designs even attempt to develop inverter topologies that do not require

a snubber [27]. An effective busbar design and appropriate dc bus capacitor selection can be used to eliminate the need for snubbers.

1.2.1.4 Output Filter Design

The IEEE has stringent recommendations [28] on the harmonics that can be injected into the grid. This necessitates the use of a higher order LCL filter for grid-connected inverters. The design of LCL filter depends on several factors such as the damping method used to suppress the resonance introduced by the LCL filter, the switching frequency of the converter, the modulation scheme and the operating dc bus voltage. Several LCL filter design methods have been proposed in literature [29–33].

1.2.1.5 Output Filter Damping

The use of a third-order LCL filter introduces resonance which needs to be damped through active or passive means. Passive damping is simple and robust but requires additional components. Also, it leads to additional power loss in the filter. Active damping does not require additional components and is lossless but adds control complexity. Both passive damping [31, 34] and active damping [35–37] are areas of active research.

1.2.1.6 Electro-Magnetic Interference (EMI) Filter Design

Electromagnetic interference issues arise due to high frequency switching. This can lead to issues such as ground leakage currents, conducted EMI and radiated EMI. Both active [38, 39] and passive methods [40] of EMI filtering are proposed in literature. EMI models of inverter [41] have also been developed to help device techniques that can mitigate EMI.

1.2.1.7 Thermal Design

The semiconductor devices in the inverter are sensitive to temperature. High temperatures can lead to device failure. It must be ensured that the device junction temperatures are maintained within datasheet specified limits. Research is aimed at developing thermal models for inverters [42], developing closed form expressions and analytical methods to compute conduction and switching losses [43] and study of materials used in the IGBT modules that would lead to less junction temperature rise [44].The various models and analytical expressions are generally used to optimize the inverter design from a thermal perspective [45].

1.2.2 Control Aspects

A survey of research on the control aspects of grid-connected inverters is presented below:

1.2.2.1 Modulation Techniques

Modulation techniques are used to convert the reference voltages of an inverter into the actual output voltages. Modulation techniques are aimed at maximum utilization of the available dc bus voltage and at reducing the instantaneous voltage error associated with the output voltage. Sine triangle [46, 47], harmonic injection based pulse width modulation [46] and various space vector based techniques [47, 48] have been discussed in literature. Some Pulse Width Modulation (PWM) methods are developed specifically for multi-level topologies [49, 50]. Carrier interleaved methods [51] help reduce common mode voltages and have also been discussed in literature. Modulation techniques still remain an active area of research.

1.2.2.2 Phase Locked Loops

A Phase Locked Loop (PLL) is a vital control loop in grid-connected systems. The PLL is required to synchronize the inverter to the grid and to keep it locked to the grid. Unit vectors generated by the PLL are usually required for proper operation of the current control loop. So, the PLL control is of importance. Research on PLLs [52–54] aim at improving the operation of the PLL under real-time conditions like grid disturbances and sensor introduced offsets.

1.2.2.3 Current Control

Current control in an inverter with output LCL filter is complex due to the presence of three energy storage elements and the resonance associated with them. Several control methods have been proposed in literature [33, 55–60]. Different controls such as a two current loop control with an outer inductor current loop and an inner output capacitor current regulation loop [55, 59], model predictive method [58] and Proportional-Resonant (PR) controller based control [60] have been investigated. Some controls aim at achieving balanced currents even during unbalanced voltage dips [56].

1.2.2.4 Voltage Control

A fixed dc bus voltage is required in grid-connected inverters. Usually, a dc bus voltage control loop is used to ensure this. For a two-level three-phase inverter topology with 3-wire configuration, the dc bus voltage control is usually simple [2, 61]. However, in multi-level inverter topologies the issue of balancing the individual dc bus capacitor voltages needs attention. Several methods of dc bus voltage balancing have been suggested for multi-level inverters [62–64]. While some methods achieve voltage balance through control [63,64], some others suggest new topologies [62] to eliminate the problem.

1.2.3 Grid Connection Standards

IEEE and IEC have laid down several guidelines related to grid-connection. IEEE Standards 1547-2003 [28] and 519-1992 [65] specify limits on the harmonic currents that can be pumped into the grid. Also, the increasing use of grid-connected inverters has initiated the development of a new IEEE standard [66] for voltage sag and interruption ride-through testing of electrical equipment.

The IEC has several standards for grid-connected systems. To mention a few, it has recommendations for harmonic current limits [67], testing and measurement techniques for voltage dips, short interruptions and voltage variation immunity [68, 69], testing and measurement techniques for harmonics, interharmonics and low frequency immunity [70], specific recommendations for wind turbines [71] and specific recommendations for photo voltaic inverters [72].

1.3 Scope of the Thesis

In this thesis, design and performance evaluation of sub-systems of grid-connected inverters have been researched. The work touches upon areas discussed in Section 1.2.1.5 and Section 1.2.1.7. Also, a test set-up to evaluate the compliance of grid-connected inverters to some standards mentioned in Section 1.2.3 has been developed. An overview of the areas of detailed investigation are:

1. **LCL filter damping design**
   LCL filters are required in grid-connected inverters to comply with the IEEE recommended harmonic limits [28, 65] on the current injected into the grid. LCL filters

introduce resonance. To damp it, either passive or active methods can be used. Passive methods are generally robust. Many passive damping networks are suggested in literature [31, 34]. However, a systematic component selection procedure has not been developed for these networks. A simple and practical component selection procedure would have wide industry application and is a focus of study in this thesis.

2. **Thermal performance evaluation of high power grid-connected inverters**
   For reliability, grid-connected inverters need to be subjected to burn-in tests before commissioning. To save energy during burn-in tests and to avoid the need for high power sources and loads, regenerative methods have been developed [73–82]. However, the available methods either require two converters of similar rating [73–80] or require individual legs of the inverters to have independent cooling arrangement [81, 82]. A method that addresses these issues would be of practical use. Also, methods for thermal testing of the filter components and dc bus capacitors are not available currently. At high power levels, these passive components also require attention. A test method for thermal performance evaluation of grid-connected inverters and the associated passive elements is a focus of study in this thesis.

3. **Verification of control performance of grid-connected inverters**
   Present day grid-connected inverters are expected to have control capabilities to remain in operation under short time grid disturbance conditions like voltage sags, voltage swells and frequency deviations. To test these capabilities, a hardware that can generate the mentioned disturbance conditions in a controlled manner is required. Besides generating sags, swells, unbalance and frequency deviations, the hardware should be programmed to create point of fault conditions like phase jumps. A simple yet powerful algorithm is required for this. Available literatures focus on the topology [83–88] used rather than the algorithm required for disturbance generation. Developing a test set-up to generate grid disturbances in a controlled manner using a powerful algorithm is a focus of study in this thesis.

1.4 Experimental Set-up

A 50kVA back-to-back connected inverter sharing a common dc bus has been custom-built for the experimental studies. The output filters have been designed and fabricated to required

specifications. The inverter set-up uses protection and gate drive circuits developed earlier, in-house. The inverters are controlled using a common digital signal processor (DSP) board. Texas Instrument's TMS320F2812 has been used for digital control. Appendix A tabulates the hardware details and provides some pictures of the experimental set-up.

1.5 Organisation of the Thesis

Chapter 1 discusses the relevance of research on grid-connected inverters. The topology used and its wide application in power quality and distributed generation is detailed. A survey of research in the area of grid-connected inverters is presented and the scope of the present work is explained. The details of the experimental set-up developed for the work is provided and the flow of the thesis is explained.

Chapter 2 discusses the design of output LCL filter and develops a component selection procedure for a chosen passive damping topology. The Chapter begins with introducing the relevant IEEE standard. The need for LCL filters in grid-connected inverters to comply with the IEEE standards is brought out. The selection of ideal LCL filter components is detailed. The issue of resonance is explained. Passive damping is suggested as a robust means to damp the resonance. A comparison of the level of damping and damping resistor power loss for three different passive damping topologies is provided. The SC-RL method is chosen as a suitable topology for high power grid-connected inverters based on the power loss. The state space model is developed for the SC-RL method using which its power loss and damping are analysed. A component selection procedure is developed for the SC-RL damping method with the goal of minimizing the losses in the damping resistor yet achieving an effective damping. Experimental results are shown to have close match with the analytical predictions.

Chapter 3 discusses the thermal performance evaluation of high-power grid-connected inverters. The need for thermal testing of semiconductor devices and the passive components associated with a grid-connected inverter is explained. The different methods available in literature are discussed and the shortcomings of the available methods are pointed out. A new method is proposed. Phasor diagrams are developed to give better insight into the operation of the proposed method. Then, common mode and differential mode equivalent circuits are developed and used for control design. Finally, the method is analysed in detail for the thermal testing of semiconductor switches, dc bus capacitors and output filter components for

both three-phase 3-wire configuration and three-phase 4-wire configuration. Experimental validation has also been provided.

In Chapter 4, a test set-up to study the control performance of grid-connected inverters has been developed. The requirement of a test set-up to create grid disturbances in a controlled manner in the laboratory environment is explained first. Then, the features of simulators available in literature are explained and the focus in the present work is detailed. The topology and controls used in the work are elaborated. A novel voltage disturbance generation algorithm is developed and analysed using finite state machine model. Experimental results of the grid simulator for linear, non-linear and inverter loads are provided to practically validate the developed algorithm.

Chapter 5 summarises the contributions of the work done in this thesis. The implications of the research work in terms of grid-connected inverter design is detailed.

1.6 Summary

In this Chapter, the wide application of grid-connected inverters is highlighted in the context of power quality improvement and distributed generation applications. The topology of the grid-connected inverter researched in this thesis has been briefed. A survey of research in the area of grid-connected inverters is detailed and the specific areas of research touched upon in this thesis is explained. An overview of the set-up built for the experimental validations has been provided and the flow of the thesis has been detailed.

Chapter 2

LCL Filter Design

Electrical equipment have limits on the harmonic currents they can inject into the grid. IEEE Standard 519–1992 [65] and IEEE Standard 1547–2003 [28] are some relevant standards that specify the current harmonic limits. Usually, in case of distributed generation, power quality applications and in front-end converter applications, an inverter connects to the grid. Hence, this grid-connected inverter is expected to meet the mentioned standards in these cases. The stringent requirements of these standards necessitate the use of a third order LCL filter at the output of grid-connected inverters, which otherwise might use a simple L filter. In this chapter, the design of LCL filter is discussed in detail with specific focus and contributions on passive damping design for LCL filters.

Section 2.1 discusses the IEEE standards for connection of power sources to the grid. The discussion brings out the need for LCL filters at the output of grid-connected inverters. Section 2.2 explains the selection of LCL filter components based on the current harmonic limits suggested by the IEEE standards. Section 2.3 details the issue of resonance associated with LCL filters. The need for damping in LCL filters is shown. Section 2.4 analyses a suitable passive damping method for LCL filter in high power grid-connected inverters. A damping component selection procedure that maintains the damping circuit loss at a low level and also provides adequate damping is proposed. Experimental results are provided to support the analytical predictions. Section 2.5 summarises the Chapter.

2.1 Regulations on Power Sources Connected to the Grid

Power sources connected to the grid have limitations on the amount of harmonics they can inject at the point of common coupling (PCC). IEEE Standard 519–1992 [65] and IEEE Standard 1547–2003 [28] are the relevant standards that can be used as reference. IEEE Standard 519–1992 discusses harmonic control in electric power systems in general whereas IEEE Standard 1547–2003 specifically discusses the same for distributed energy sources connected to the grid. The current harmonic specifications in both the mentioned standards arise from the common objective of limiting the individual frequency voltage harmonic to less than 3% of the nominal fundamental voltage and the voltage total harmonic distortion (THD) to less than 5%. Hence, the two standards can be used interchangeably. As per the mentioned standards, the limits on the current harmonics that a distributed source can inject into the grid at the PCC are as given in Table 2.1. Appendix B describes some terminology and definitions related to harmonic limits. Also, it describes the standard test recommended by the IEEE Standard 1547–2003 to check for conformance to the recommended harmonic limits listed in Table 2.1.

Individual harmonic order h (odd harmonics)	**h < 11**	**11 ≤ h < 17**	**17 ≤ h < 23**	**23 ≤ h < 35**	**35 ≤ h**	**TDD**
In % of I	4.0	2.0	1.5	0.6	0.3	5.0
Note 1: I is the local electric power system's maximum demand fundamental load current (15 or 30 minute demand)						
Note 2: Even harmonics are limited to 25% of the odd harmonic limits above						

Table 2.1: IEEE recommended limits on harmonic currents injected into the grid at the PCC by a distributed source feeding a balanced linear load.

2.1.1 Need for LCL Filter in Grid-Connected Inverters

For pulse-width modulated (PWM) inverters with high carrier frequency, the ripple predominantly has frequency components at and around the switching frequency (ω_{sw}) and its multiples. Fig. 2.1 shows a typical voltage spectrum observed at the output terminals of a 3-phase 2-level grid-connected inverter. Considering switching frequencies of 2 kHz and above, the voltage harmonics appear at the harmonic order of $h > 35$. Hence, from Table 2.1, it can be stated that all individual odd and even harmonic components should be limited to 0.3% and 0.075% of the fundamental rated current respectively and the TDD should be limited to 5%.

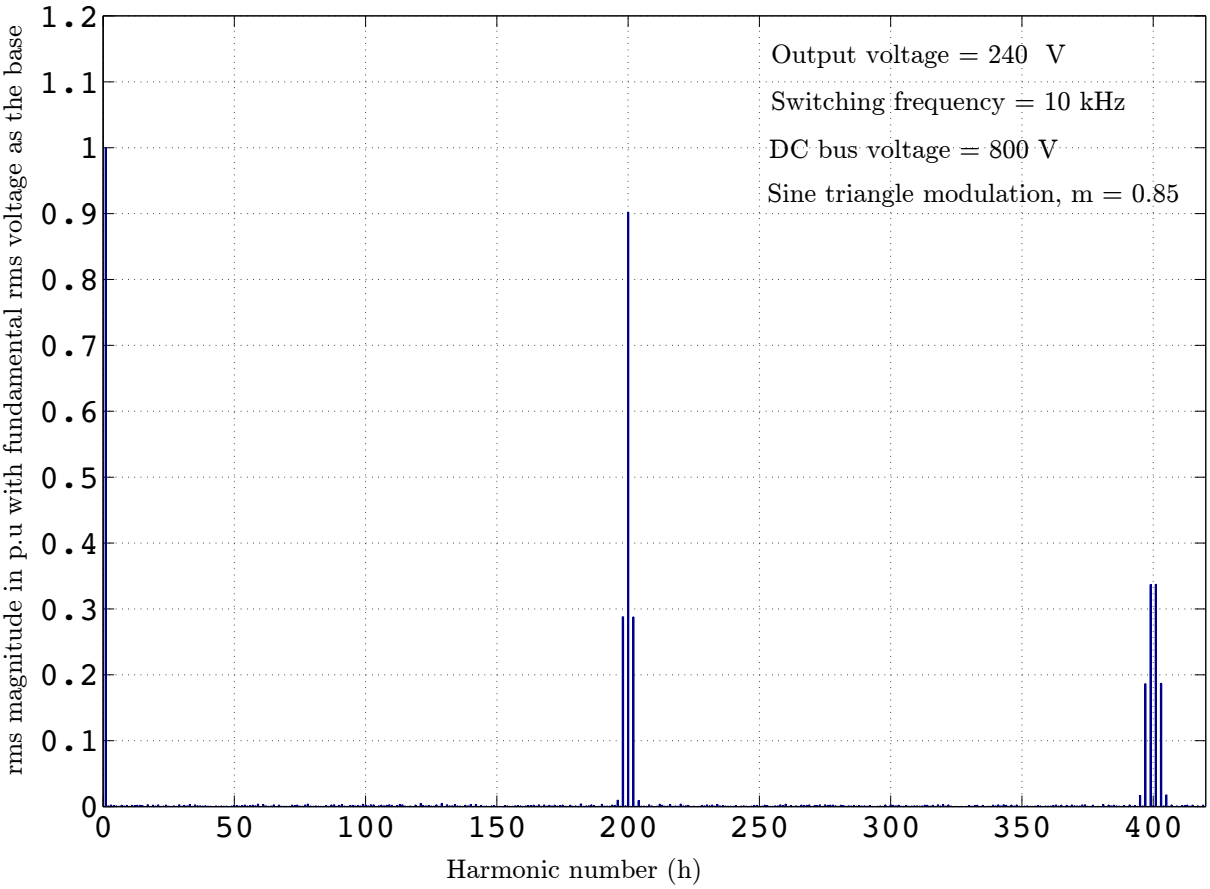


Figure 2.1: Harmonic spectrum of terminal voltage measured with respect to dc bus midpoint in a 3-phase 2-level inverter for a fundamental output voltage of 240 V and dc bus voltage of 800 V. The spectrum is valid for the case when the inverter just balances the grid. Switching frequency f_{sw} considered is 10kHz.

Let us attempt to use a simple first order L filter to achieve the required individual harmonic limit for the spectrum shown in Fig. 2.1. Considering a 4-wire connection with the neutral connected to the dc bus mid-point, the predominant harmonic component is at $h = 200$. If the chosen filter limits the 200^{th} harmonic component of current to within 0.075%, all the other individual harmonic components will surely be within the limits as the impedance offered by the filter to all other harmonic components would almost be the same or higher. For the 200^{th} harmonic, V (p.u) = 0.9 and I (p.u) = 0.00075 (as per limits). So, the required fundamental frequency impedance Z (p.u) is,

$$\text{Z (p.u)} = \omega(p.u) \cdot L(p.u) = \frac{V(p.u)}{I(p.u) \cdot 200} = 6.0 \text{ p.u.}$$

The p.u impedance of 6.0 is too high. Besides being bulky and costly, the high filter impedance will increase the dc bus voltage requirement to impractical levels. The dc bus voltage is chosen such that the maximum ac voltage that can be produced at the output of the inverter will be able to balance the phasor sum of the grid voltage and the output filter drop. An increase in the switching frequency can be thought of as a solution to maintain the inductance value to be less and still maintaining the harmonic current limits. However, the increased switching losses and the limitations on the maximum switching frequency of the available devices will make it impossible. A higher order filter is the only viable solution. A second order LC filter is not usually opted as both the inverter considered and the grid are voltage sources and connecting a capacitor in parallel to a voltage source is redundant. Hence, a third order LCL filter is generally used. The next Section explains the LCL filter design.

2.2 LCL Filter Design

Fig. 2.2 shows the 3-phase 2-level inverter connected to the grid through a LCL filter. The 4-wire configuration gives the worst-case current ripple and is considered for the LCL filter design. The design outcome can be used for a 3-wire configuration also though it would be conservative. Reference [89] discusses a method of choosing the ideal LCL filter components L_1, L_2 and C shown in Fig. 2.2. The design of the ideal LCL filter components used in this work follows a similar methodology as [89]. However, there are significant differences in the method developed in this thesis. This Section explains the selection of ideal LCL

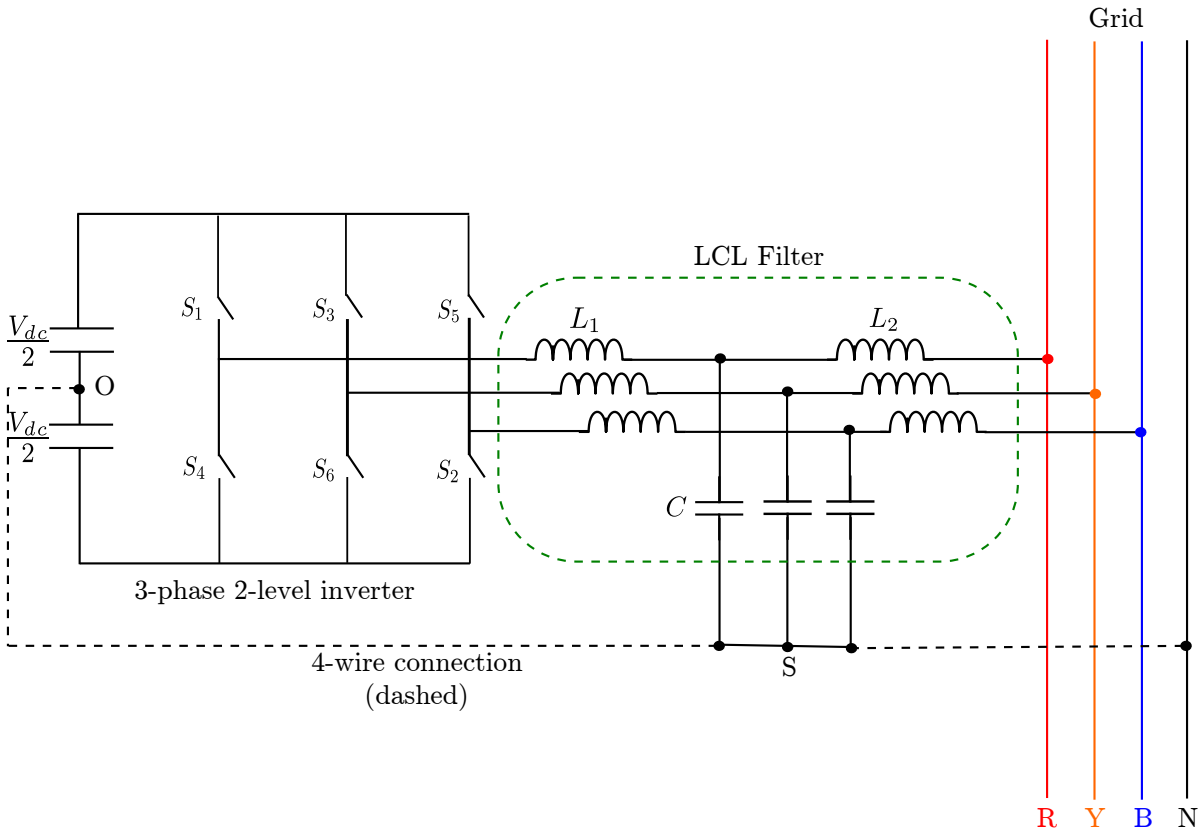


Figure 2.2: 3-phase 2-level inverter connected to the grid through a LCL filter in a 3-wire configuration (solid lines) and 4-wire configuration (dashed lines).

filter components used in the present work. The differences as compared to [89] are pointed out wherever applicable. With the ideal LCL filter components selected as described in this Section, a component selection procedure for a passive damping network is proposed in Section 2.4. The proposed method is useful to damp the LCL filter resonance, specifically at high power levels.

2.2.1 Choice of L

Fig. 2.3 shows the simplified circuit equivalent of the 4-wire configuration shown in Fig. 2.2. The grid is considered shorted for frequencies other than fundamental as the grid voltage is ideally zero at those frequencies. With the grid shorted and ω_r representing the natural frequency of oscillation of an ideal LCL filter with no damping, it can be shown that,

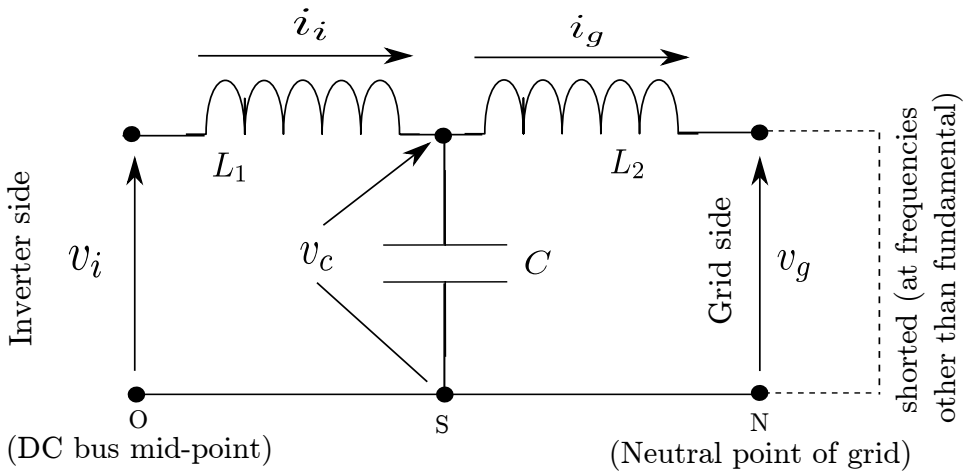


Figure 2.3: Per-phase circuit equivalent of the LCL filter connected between a 3-phase 2-level inverter and the grid in a 4-wire configuration. The grid impedance is lumped along with L_2.

$$\frac{I_g(s)}{V_i(s)} = \frac{1/L}{s[1 + (s/\omega_r)^2]} \tag{1}$$

Where,

$$L = L_1 + L_2 \tag{2}$$

$$\omega_r = \frac{1}{\sqrt{CL_p}} \tag{3}$$

$$L_p = \frac{L_1 L_2}{L_1 + L_2} \tag{4}$$

From (1),

$$L = \frac{|V_i(j\omega)|}{|I_g(j\omega)|\ |j\omega|\ |1 - (\omega/\omega_r)^2|} \tag{5}$$

As explained in Section 2.1.1, generally if the filter limits the dominant harmonic around the switching frequency to be within the individual harmonic limit, all other individual harmonics will also be within the limits. This can also be observed from Fig. 2.4, which shows a typical bode plot of $\frac{I_g(s)}{V_i(s)}$. Considering considerably high switching frequencies of 2

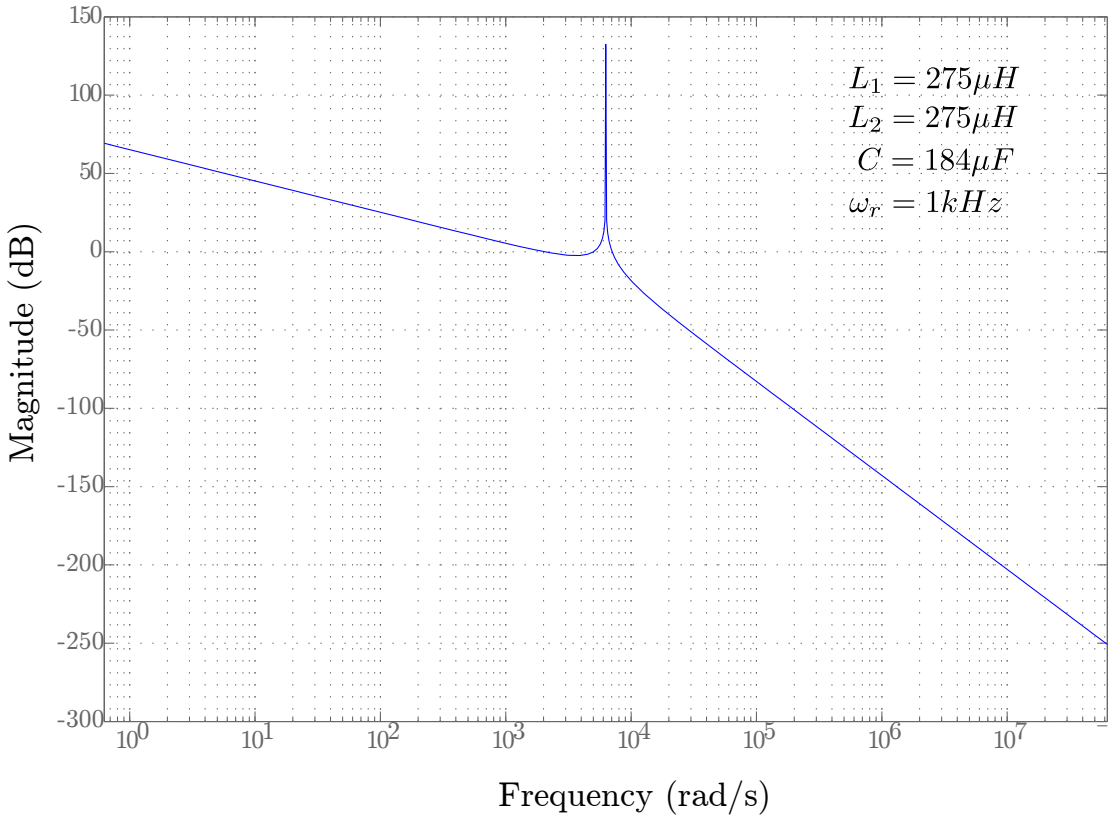


Figure 2.4: A typical bode plot of the transfer function $\frac{I_g(s)}{V_i(s)}$ for an ideal LCL filter. The pass band and stop band frequencies are decided by the chosen resonance frequency. All frequencies above the resonance frequency are attenuated.

kHz and above, the TDD will also be within the limits. If the dominant harmonic component is represented as ω_{dom}, we have from (5),

$$L_{min1} = \frac{|V_i(j\omega_{dom})|}{|I_g(j\omega_{dom})|\ |j\omega_{dom}|\ |1-(\omega_{dom}/\omega_r)^2|} \tag{6}$$

Equation (6) gives a minimum value of L as any value of L lower than this will not meet the IEEE recommended harmonic limits. Equation (6) requires ω_r to be known. The choice of ω_r is discussed in Section 2.4.4.1. Consider a sample design where the choice of ω_r is, $\omega_r = 2 \cdot \pi \cdot 1000$. On a frequency base of $2 \cdot \pi \cdot 50$, $\omega_r(\text{p.u}) = 20$. The resonance frequency ω_r sets the pass band frequency of the filter as can be observed from Fig. 2.4. The frequencies

above the resonance frequency will be strongly attenuated. From, Fig. 2.1, the dominant frequency is 200 p.u and its magnitude is 0.9 p.u. Reference [89] considers an approximate value for the magnitude of the dominant frequency. In this thesis, an accurate actual p.u magnitude from the spectral analysis is used. The dominant frequency being an even harmonic greater than 35, the IEEE recommended harmonic current limit from Table 2.1 is 25% of 0.3%. Substituting the values of the various parameters in (6), we have,

$$L_{min1} = \frac{0.9}{(0.25 * 0.003) \cdot (200) \cdot \left| 1 - \left(\frac{200}{20} \right)^2 \right|} = 0.0606 \tag{7}$$

The maximum value of L is limited to say 0.1 p.u, to avoid too high a value of dc bus voltage requirement. Thus,

$$L_{max} = 0.1 \text{ p.u} \tag{8}$$

L_{min1} and L_{max} sets limits for L of the LCL filter. Observing (7), it can be seen that the value of L_{min1} can be considerably reduced if even harmonics are not present in the voltage spectrum as the current harmonic limits are too stringent for even harmonics. A proper choice of switching frequency can remove the presence of even harmonics. For example, the voltage harmonic spectrum for a switching frequency of 9.75 kHz is shown in Fig. 2.5. Here, unlike in Fig. 2.1, the dominant harmonic is h = 195 which is odd. There are no even harmonics present in the voltage spectrum. The value of L_{min1} in this case is 0.0167 p.u.

2.2.2 Choice of L_1 and L_2

Let,

$$L_1 = a_L \cdot L_2 \tag{9}$$

Then, from (3) and (4),

$$L = \frac{(1 + a_L)^2}{\omega_r^2 \cdot a_L \cdot C} \tag{10}$$

Reference [89] does not consider any limits on the reactive power requirement of the filter capacitor. A lesser reactive power requirement of the filter capacitor at the fundamental frequency or equivalently a lesser value of filter capacitance C is desirable. Hence a reactive power limit for the capacitor is also used as a filter design constraint in this work. Also,

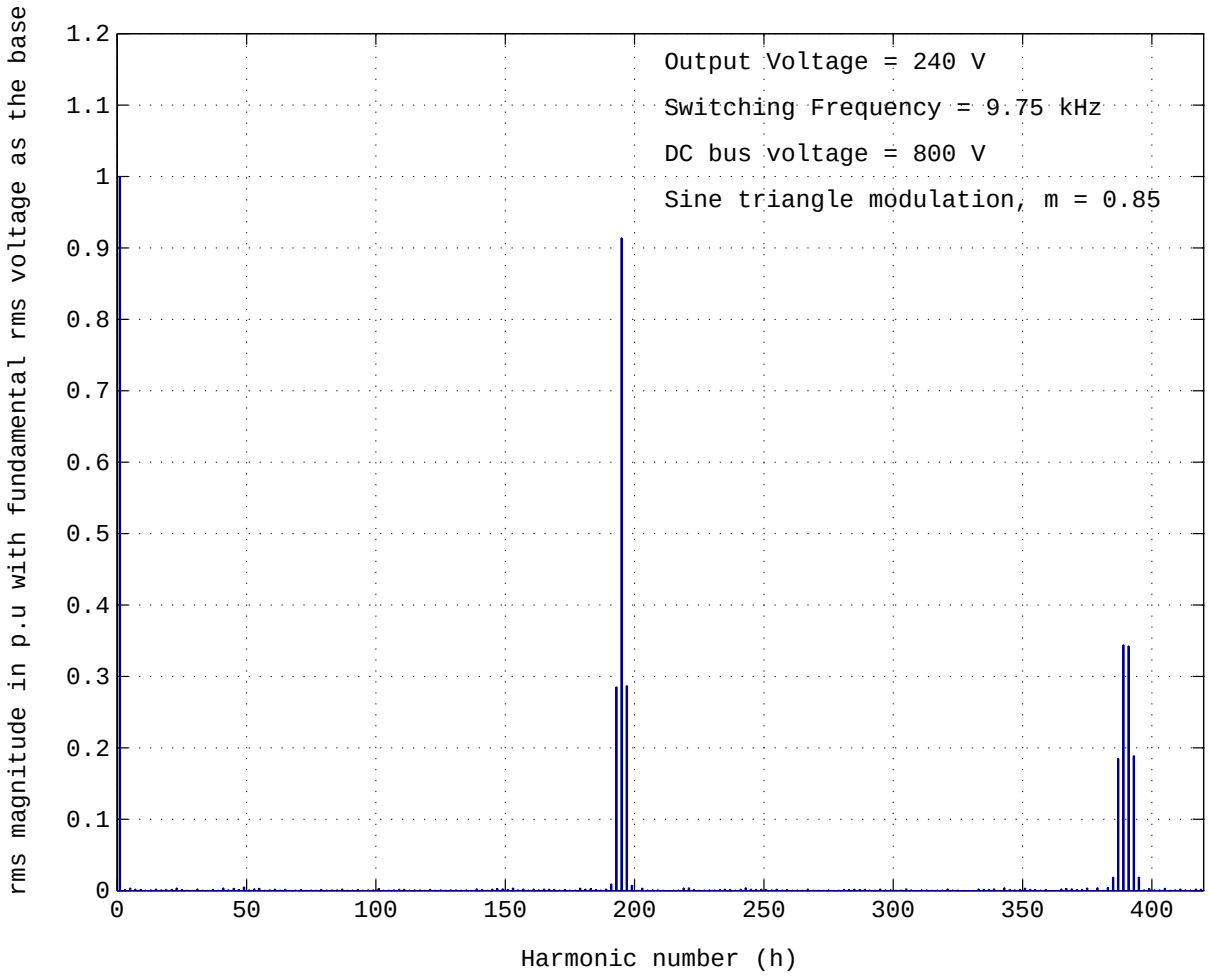


Figure 2.5: Harmonic spectrum of terminal voltage measured with respect to dc bus mid-point in a 3-phase 2-level inverter for a fundamental output voltage of 240 V and dc bus voltage of 800 V. The spectrum is valid for the case when the inverter just balances the grid. Switching frequency f_{sw} considered is 9.75kHz.

a lesser value of inductance L is desirable. While a lesser value capacitance reduces the unnecessary flow of larger reactive currents in the filter capacitor, a lesser value of inductance helps reduce the system cost. When the experimental set-up was designed, the cost per kVA of the capacitor and inductor were Rs.3000 and Rs.18000 respectively. From (10), for a chosen ω_r and $C = C_{max}$ decided by the limit on the reactive power requirement of the filter capacitor, the inductance L is minimum when $dL/da_L = 0$ and $d^2L/da_L^2 > 0$. This gives $a_L = 1$.

So,

$$L_1 = L_2 = \frac{L}{2} \tag{11}$$

L_2 includes the grid inductance. Using (10), based on the constraint on the reactive current drawn by the capacitor, we have for $a_L = 1$,

$$L_{min2} = \frac{4}{\omega_r^2 C_{max}} \tag{12}$$

L is chosen such that,

$$max(L_{min1}, L_{min2}) \leq L \leq L_{max} \tag{13}$$

As outlined in [89], L can be optimized for the power loss at this stage. Once it is optimized at this stage, the selection of damping elements will not alter the power loss in L significantly. This is because, the resonance frequency component of current is negligible compared to the fundamental frequency and switching ripple components of current through them and do not contribute much to their total power loss. Also, the damping elements do not significantly alter the fundamental and switching ripple components of current through L_1 and L_2.

2.2.3 Selection of C

Using (4) and (11), $L_p = L/4$. So, for the L chosen using (13), we have from (3),

$$C = \frac{4}{\omega_r^2 L} \tag{14}$$

2.3 Resonance in LCL Filters

Two resonances exist in an LCL filter that is connected at the output of a grid-connected inverter. This section explains the origin of these resonances and the need for damping. The resonances can be understood from the simplified per-phase equivalent circuit shown in Fig. 2.3.

2.3.1 Parallel Resonance

This occurs when the parallel impedance of L_2 and C becomes infinite at some frequency ω_p. ω_p is the parallel resonance frequency. Ideally, this leads to zero current flow for any voltage of that frequency present at the inverter output terminal since $L_2 \parallel C$ now appears as a virtual open circuit.

We have,

$$\frac{\jmath\omega_p L_2 \cdot \frac{1}{\jmath\omega_p C}}{\jmath\omega_p L_2 + \frac{1}{\jmath\omega_p C}} = \infty \tag{15}$$

From (15), $\omega_p = \frac{1}{\sqrt{L_2 C}}$

2.3.2 Series Resonance

This occurs when the parallel impedance of L_2 and C gets cancelled by the impedance of L_1 at some frequency ω_s. ω_s is the series resonance frequency. Under ideal circuit conditions, this leads to infinite current flow for any voltage of that frequency present at the inverter output terminal since the filter appears as a virtual short.

We have,

$$\jmath\omega_s L_1 + \frac{\jmath\omega_s L_2 \cdot \frac{1}{\jmath\omega_s C}}{\jmath\omega_s L_2 + \frac{1}{\jmath\omega_s C}} = 0 \tag{16}$$

From (16), $\omega_s = \frac{1}{\sqrt{L_p C}}$

It is desirable that the inverter output voltage should not contain components of voltage at the resonance frequencies ω_p and ω_s. But, the switching transients and non-idealities such as the dead-time can cause resonance frequency voltage components to appear at the

inverter output terminals. So, the effect of resonances cannot be ignored. However, only the series resonance is the one of concern as the current flow is zero in the case of parallel resonance. It may be noted that this is because of the fact that a voltage source inverter (VSI) is being considered currently.

The series resonance needs to be damped in order to avoid excessive current flow due to excitation of the series resonance frequency. The damping can be done through active or passive means. Passive damping does not require any complex control and is more reliable. Hence, in the present work, a novel component selection procedure is developed for a passive damping method and is used to contain the series resonance. The next Section discusses the passive damping method in detail.

2.4 Damping Design for LCL Filter

Several passive damping methods have been suggested in literature. References [31] and [34] give an almost exhaustive list of possible passive damping schemes. In this Section, some selected schemes based on the simplicity of the circuitry are briefed. Then, a detailed analysis of the Split-Capacitor Resistive-Inductive (SC-RL) scheme is presented. The better suitability of the SC-RL scheme as compared to the other schemes for use in high power inverters is shown. The hardware being of higher power, the SC-RL scheme is chosen. A novel component selection procedure is developed for the SC-RL passive damping scheme. The proposed method performs the design selection of the damping network components one at a time, optimizing the circuit parameters at each stage of addition of the components. The method thus relies on a practical engineering method to passive network design rather than on a purely multi-parametric mathematical optimization approach. The power loss in the damping network and the level of damping are the cost functions used for optimization at every stage.

2.4.1 Passive Damping Schemes

2.4.1.1 Purely Resistive (R) Damping Scheme

The purely resistive (R) damping scheme is the simplest of the damping schemes where a damping resistor (R_d) is connected in series with the capacitor as shown in Fig. 2.6(a). The drawback of this scheme is that all the components of current - fundamental, resonance and

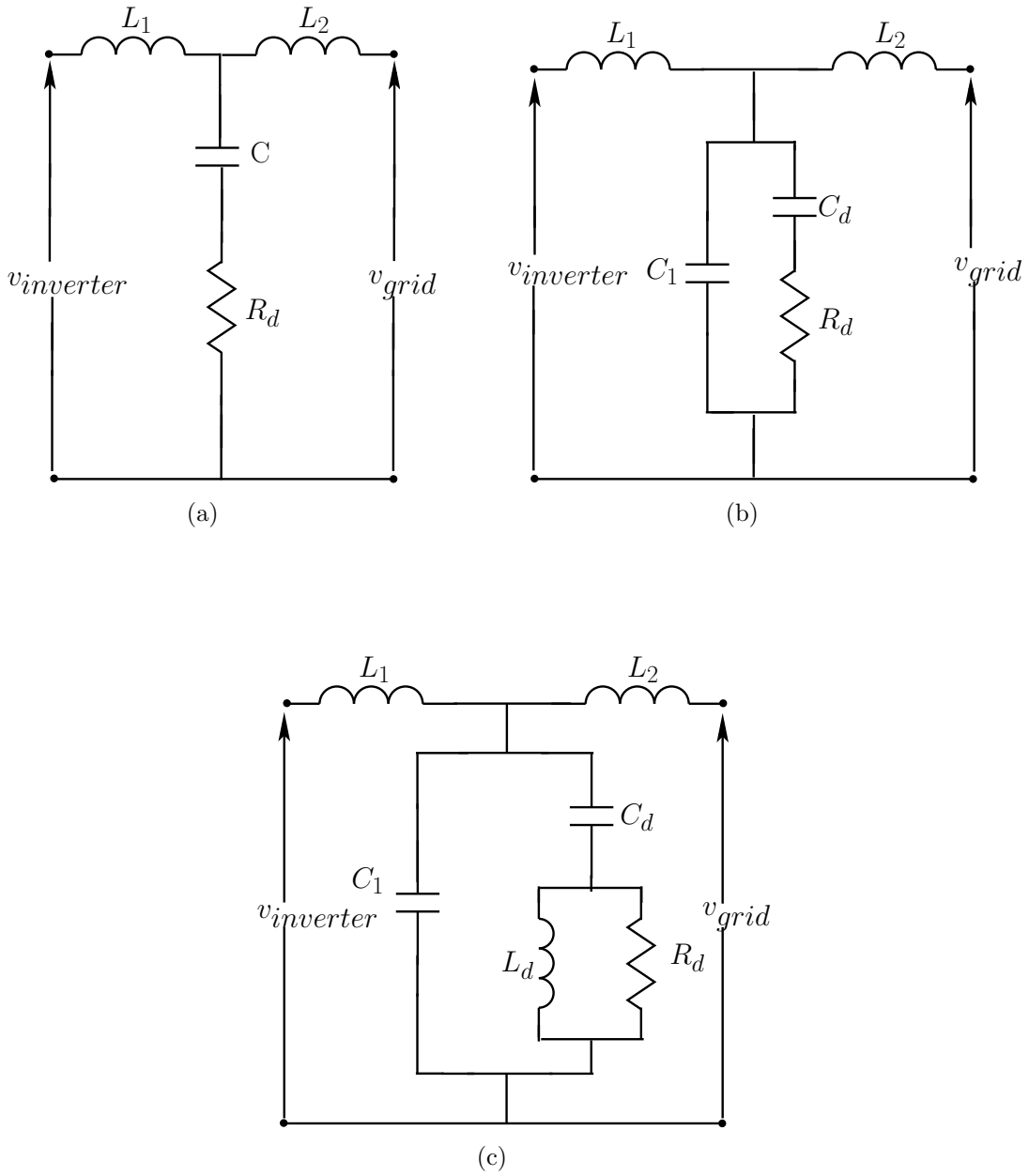


Figure 2.6: Passive damping schemes. (a) Purely Resistive (R) damping scheme. (b) Split-Capacitor Resistive (SC-R) damping scheme. (c) Split-Capacitor Resistive-Inductive (SC-RL) passive damping scheme.

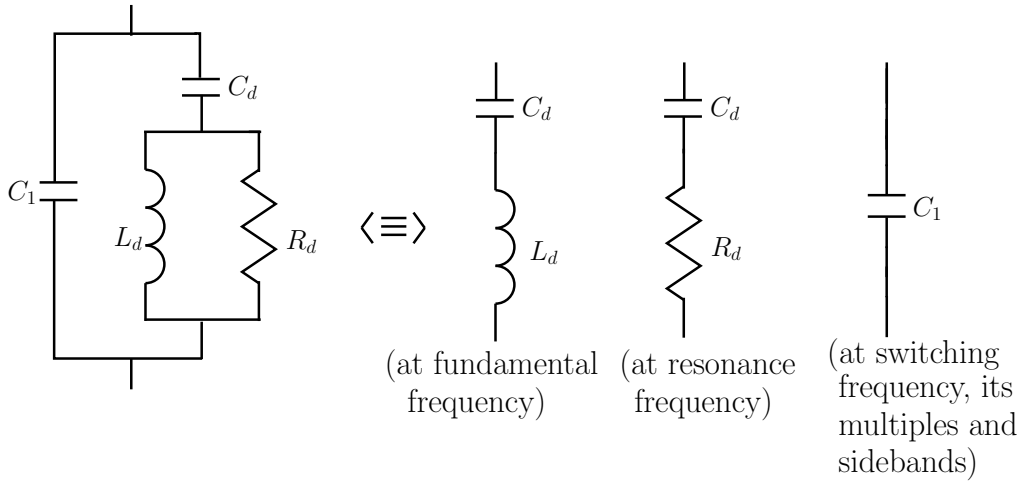


Figure 2.7: Conceptual view of SC-RL damping scheme showing the predominant current flow paths in the filter capacitor branch at different frequencies.

switching flow through the damping resistor R_d. So, the loss in R_d is high. However, this method is suitable for low power inverters up to a few kVA due to the less component count.

2.4.1.2 Split-Capacitor Resistive (SC-R) Damping Scheme

Fig. 2.6(b) shows the Split-Capacitor Resistive (SC-R) damping scheme. Here, the switching ripple gets predominantly by-passed through capacitor C_1 and R_d finds only the fundamental and resonance components flowing through it. So, the loss in R_d is moderate. This method is suitable for inverter power levels in the range of a few kVA to few tens of kVA.

2.4.1.3 Split-Capacitor Resistive-Inductive (SC-RL) Damping Scheme

In the SC-RL damping scheme shown in Fig. 2.6(c), the fundamental frequency component of current is largely by-passed through the damping inductor, L_d, the switching ripple currents are largely by-passed through C_1 and only the resonance current flows predominantly through R_d. So, SC-RL damping scheme has very less loss in R_d and hence is suitable for high power inverters ranging from a few tens of kVA up to around 1 MVA. Fig. 2.7 shows the conceptual view of the SC-RL damping scheme.

It can be observed that the SC-RL damping scheme is an evolution over the R and SC-R damping schemes in an attempt to reduce the loss in the damping resistor.

2.4.1.4 Focus of Work

The present work on passive damping design for LCL filters focuses on the following:

1. To develop state space models for R, SC-R and SC-RL passive damping networks.

2. To analyse the level of damping and the power loss in the damping network using the developed state space models.

3. To make a quantitative comparison of R, SC-R and SC-RL damping schemes based on their attenuation at the switching frequency and the total power loss in the damping resistor for the same level of damping.

4. To develop a component selection procedure for the damping scheme that has low losses. The SC-RL scheme has the low losses and so a component selection procedure that aims at minimising the power loss in the damping resistor while keeping the system well damped has been developed for the same. Though the SC-RL passive damping scheme is available in literature [31, 34], a systematic component selection procedure has not been developed for the topology.

2.4.2 Modelling and Analysis of SC-RL Damped LCL Filter

Any passive damping scheme can be evaluated for its performance based on its level of damping and the total power loss (P_T) in the damping resistor. The power loss is of concern especially when the inverter is rated at or above a few tens of kVA. The level of damping is quantified by Quality Factor (QF). A low value of QF translates into better damping. In this Section, first a state space model is developed for the damped LCL filter. Then, expressions for QF and P_T are derived. The state space model is made use of in the power loss computations. The advantages of the state space approach to compute the power loss over a direct time-domain simulation is explained in Section 2.4.2.3. The modelling and analysis have been discussed in detail for the SC-RL passive damping scheme. The state-space model, QF expressions and the power loss expressions can be derived for the R and SC-R passive damping schemes also using the same principles explained for the SC-RL damping scheme. The various expressions for R and SC-R damping schemes appear in Appendix D.

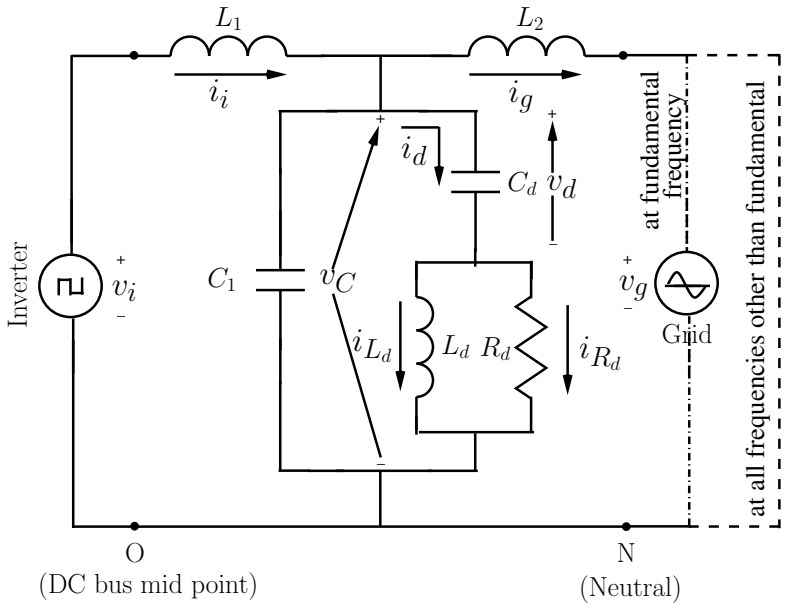


Figure 2.8: An SC-RL damped LCL filter at the output of one phase of a three-phase 4-wire inverter, showing the various state variables used to model the system.

2.4.2.1 Modelling of SC-RL Damped LCL Filter

The SC-RL damped LCL filter is modelled by considering one leg of a three-phase 4-wire inverter as shown in Fig. 2.8. The state variables are chosen to be i_i, i_g, v_C, v_d and i_{L_d}. From Fig. 2.8, the state equations and the output equation considering i_{R_d} as the output are as follows:

$$\frac{di_i}{dt} = \frac{1}{L_1}v_i - \frac{1}{L_1}v_C \tag{17}$$

$$\frac{di_g}{dt} = \frac{1}{L_2}v_C - \frac{1}{L_2}v_g \tag{18}$$

$$\frac{dv_C}{dt} = \frac{1}{C_1}[i_i - i_g - (i_{L_d} + \frac{v_C - v_d}{R_d})] \tag{19}$$

$$\frac{dv_d}{dt} = \frac{1}{C_d}[i_{L_d} + (\frac{v_C - v_d}{R_d})] \tag{20}$$

$$\frac{di_{L_d}}{dt} = \frac{1}{L_d}(v_C - v_d) \tag{21}$$

$$i_{R_d} = \frac{1}{R_d}[v_C - v_d] \tag{22}$$

The state equations (17) to (21) and the output equation (22) can be represented in the

matrix form as,

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \end{aligned} \tag{23}$$

Where,

$$\mathbf{A}= \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 \\ \frac{1}{C_1} & -\frac{1}{C_1} & -\frac{1}{C_1 R_d} & \frac{1}{C_1 R_d} & -\frac{1}{C_1} \\ 0 & 0 & \frac{1}{C_d R_d} & -\frac{1}{C_d R_d} & \frac{1}{C_d} \\ 0 & 0 & \frac{1}{L_d} & -\frac{1}{L_d} & 0 \end{bmatrix}; \mathbf{B}= \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & -\frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}; \mathbf{x}= \begin{bmatrix} i_i \\ i_g \\ v_C \\ v_d \\ i_{L_d} \end{bmatrix};$$

$$\mathbf{u}= \begin{bmatrix} v_i \\ v_g \end{bmatrix}; \quad \mathbf{C}= \begin{bmatrix} 0 & 0 & \frac{1}{R_d} & -\frac{1}{R_d} & 0 \end{bmatrix}; \quad \mathbf{D}= [0 \;\; 0]; \quad \mathbf{y}= i_{R_d};$$

The inputs to the model are the inverter output voltage, v_i, and the grid voltage, v_g. The inverter voltage v_i is either $+V_{dc}/2$ or $-V_{dc}/2$ depending on whether the top switch of the inverter leg is ON or OFF respectively.

$$v_i = \begin{cases} +\frac{V_{dc}}{2}, & 0 < t < t_{on} \\ -\frac{V_{dc}}{2}, & t_{on} < t < T_{sw} \end{cases} \tag{24}$$

where, t_{on} is the time duration in a switching cycle when the top switch of the inverter leg is ON and T_{sw} is the switching time period. The output of the model has been selected to be i_{R_d} so that it can be used for loss evaluation in the damping circuit.

Based on the above filter model, the quality factor and power loss of the SC-RL damped LCL filter for a three-phase 4-wire configuration are derived in Section 2.4.2.2 and Section 2.4.2.3 respectively. It may be noted that the model can be used even for a three-phase 3-wire case if v_i is modified suitably to include the dc bus mid-point to output neutral voltage. Equivalently, only the differential mode component of v_i at every instant is to be considered for a 3-wire case. The differential mode component of voltage is the actual voltage at the inverter output terminal w.r.t the dc bus mid-point less the common mode component. The common mode component of voltage at every instant can be computed as the average of the three phase instantaneous voltages at the output terminals of the inverter.

2.4.2.2 Quality Factor (QF)

In Fig. 2.8, $V_C(s)/V_i(s)$ – the capacitor voltage to inverter leg voltage, is the representative transfer function that is used to study the damping of the series resonance in the present work. Fig. 2.9 shows a typical plot of the transfer function $V_C(s)/V_i(s)$. The difference in magnitude between the resonance peak of the curve and the flat portion of the curve defines the quality factor (QF). The flat portion of the curve extends from dc to near resonance frequency. The nature of the bode plot explains the choice of the transfer function $V_C(s)/V_i(s)$. The QF can be easily defined using this transfer function rather than for example, using the transfer function $I_g(s)/V_i(s)$ shown for an ideal LCL filter in Fig. 2.4.

Mathematically, the QF can be expressed as,

$$QF = \frac{\left|\frac{V_C(j\omega)}{V_i(j\omega)}\right|_{\text{at } \omega = \omega_d}}{\left|\frac{V_C(j\omega)}{V_i(j\omega)}\right|_{\omega \to 0}} \tag{25}$$

where, ω_d is the resonance frequency of the LCL filter with the damping components included. ω_d is that value of ω for which the magnitude of the transfer function (26) peaks. A detailed discussion of QF in the context of LCL filter design appears in Appendix C.

From Fig. 2.8, considering the grid side voltage source as a short, $V_C(s)/V_i(s)$ can be shown to be,

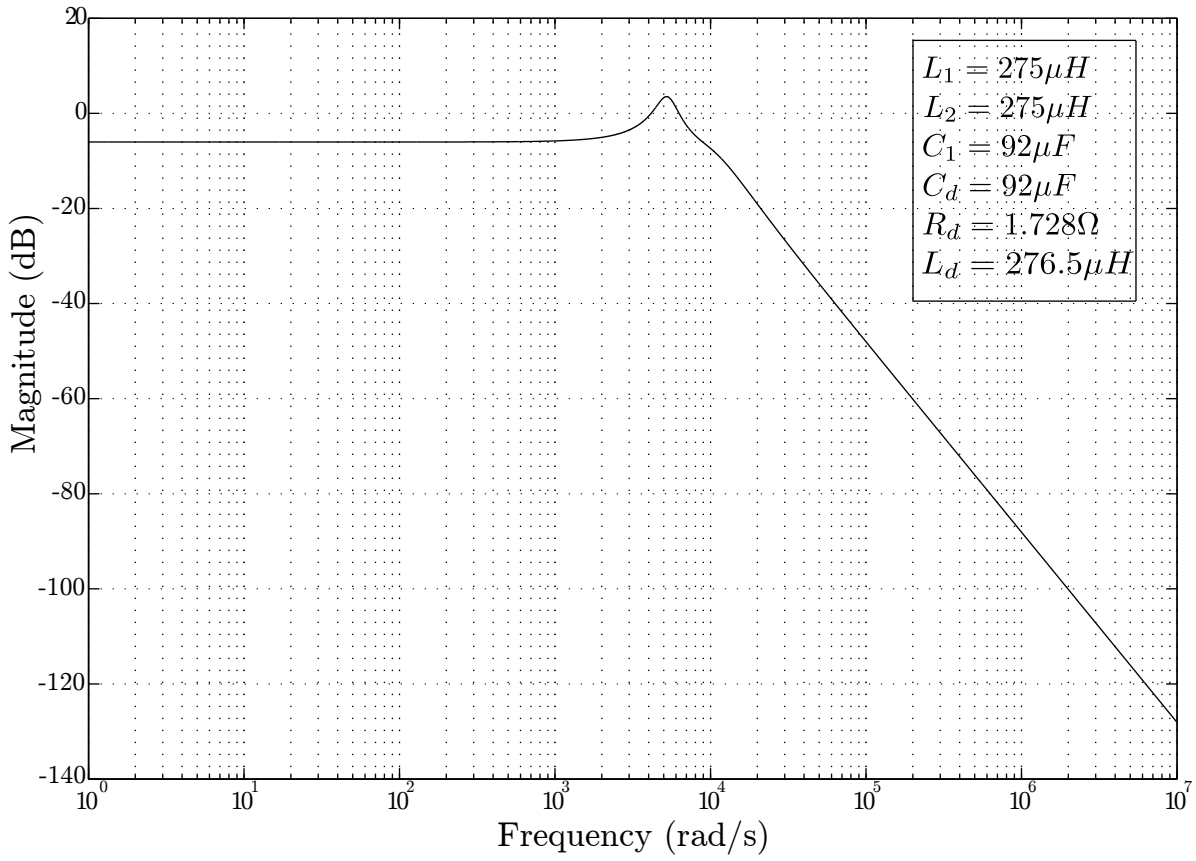


Figure 2.9: A typical bode plot of the transfer function $\frac{V_C(s)}{V_i(s)}$ for a SC-RL damped LCL filter. The quality factor is a measure of the resonance peak of the plot with respect to the flat portion of the curve extending from dc to near resonance frequency.

$$\frac{V_C(s)}{V_i(s)} = \frac{Nr(s)}{Dr(s)} \tag{26}$$

Where,

$$\begin{aligned} Nr(s) &= R_d\ L_2\ s + \ L_2\ L_d\ s^2 + R_d\ C_d\ L_2\ L_d\ s^3; \\ Dr(s) &= R_d(L_1 + L_2)s + (L_1 + L_2)L_d s^2 + R_d[L_1 L_2(C_1 + C_d) + L_d C_d(L_1 + L_2)]s^3 \\ &\quad + L_1 L_2(C_1 + C_d)L_d s^4 + R_d L_1 L_2 C_1 C_d L_d s^5. \end{aligned}$$

The transfer function is applicable for all frequencies other than the fundamental. The grid reactance can be lumped along with the output inductance L_2.

Simplified approximate expression for QF can be arrived at by assuming $\omega_d = \omega_r$. ω_r is the resonance frequency of the ideal LCL filter without the damping components. i.e. the assumption is that the resonance frequency remains the same even after the passive damping components are added to the ideal LCL filter. The following are the steps to find the approximate QF expression.

1. The s-domain transfer function $\frac{V_C(s)}{V_i(s)}$ is derived using simple circuit principles assuming grid to be shorted.
2. The relationship $\frac{V_C(j\omega)}{V_i(j\omega)}$ is obtained by the substitution $s = j\omega$.
3. The numerator in (25) is computed from $\frac{V_C(j\omega)}{V_i(j\omega)}$ by using the substitution $\omega = \omega_r = \frac{1}{\sqrt{(L_1 \parallel L_2)C}}$. $L_1 = L_2 = \frac{L}{2}$ as discussed in Section 2.2.2.
4. The denominator in (25) is computed from the $\frac{V_C(j\omega)}{V_i(j\omega)}$ by using the substitution $\omega = 0$. This gives the magnitude of the transfer function at low frequencies and dc.
5. By substituting the numerator and denominator expressions computed as explained above, the simplified approximate closed form expression for QF can be arrived at from (25).

From (26), with $C_1 = C_d = C/2$ as suggested in Section 2.4.4, the simplified expression for QF is given by,

$$QF = 2 \times \sqrt{1 + \left(1 - \frac{R_d\sqrt{LC}}{2L_d}\right)^2} \tag{27}$$

Equivalently,

$$QF = 2 \times \sqrt{1 + \left(1 - \frac{K_{L_d} \cdot \omega_{fu}}{\omega_r}\right)^2} \tag{28}$$

where, the damping impedance factor (K_{L_d}) is defined as,

$$K_{L_d} = \frac{R_d}{\omega_{fu} \cdot L_d} \tag{29}$$

K_{L_d} is a function of L_d and it can be interpreted as that multiple of fundamental frequency (ω_{fu}) at which the damping resistance equals the impedance of the damping inductor. It can be observed later that K_{L_d} is unitless and serves as a generalized design parameter.

It can be seen from (28) that the minimum QF occurs for $K_{L_d} = \omega_r/\omega_{fu} = \omega_r$(p.u.). However, the addition of the damping circuit will actually alter the resonance frequency of the LCL filter. The refined value of K_{L_d} due to the modified resonance frequency is obtained numerically as described in Section 2.4.4.3. The usefulness of (28) is that it indicates a possible relationship between K_{L_d} and ω_r(p.u.). A detailed discussion on this appears in Section 2.4.4.4.

2.4.2.3 Power Loss

The power loss primarily consists of two components - the fundamental frequency component, P_{fu}, and the switching ripple component, P_{ri}. The switching frequency is well separated from the resonance frequency and does not excite any resonance component in steady state. However, in the hardware small resonance components that are excited by the transients and other sources such as switch non-idealities are usually observed. The QF being low, the current and hence the power loss due to this is negligible and is not considered for the total power loss (P_T) computations.

Loss due to fundamental frequency current: From Fig. 2.8, the fundamental power loss component, P_{fu}, in the damping resistor of the filter can be obtained as follows:

$$P_{fu} = \Re\{V_C \; I_d^*\}|_{\omega=\omega_{fu}} \tag{30}$$

From the circuit analysis of Fig. 2.8, we can express P_{fu} as,

$$P_{fu} = \Re\left\{\frac{V_C \; V_C^*}{\left[\frac{j\omega_{fu} \; L_d \; R_d}{R_d + j\omega_{fu} \; L_d} + \frac{1}{j\omega_{fu} \; C_d}\right]^*}\right\} \tag{31}$$

At fundamental frequency, the voltage magnitude at the inverter and the grid are close to 1 p.u. So, V_C can be approximated to be 1 p.u as the voltage drop in the filter inductors L_1

and L_2 is less. Substituting all quantities in per unit, we have,

$$P_{fu}(p.u.) = \frac{C_d^2 R_d}{K_{L_d}^2 - 2C_d R_d K_{L_d} + (1 + C_d^2 R_d^2)} \tag{32}$$

The denominator function in (32) represents a parabola with a symmetry parallel to the y-axis when K_{L_d} is plotted in the x-axis and the value of the function is plotted along the y-axis. Since the magnitude of a parabola increases rapidly with x-axis value, P_{fu} which is an inverse function falls to a low value quickly and changes very less there after. This can be observed in the fundamental frequency power loss curve of Fig. 2.14 shown in Section 2.4.4. The fundamental frequency power loss curve has a knee point as expected. After the knee point, the power loss almost remains a constant. So, any value of K_{L_d} after the knee point is a good choice from the perspective of P_{fu}.

Loss due to switching ripple current: Using the state space model given by (23), the loss due to the switching ripple component of current that comprises of the switching frequency, its multiples and sidebands can be computed. The computation of i_{R_d} and $i_{R_d,rms}$ is given in detail in Section 2.4.2.4. The ripple current is dependent on the duty ratio d, which varies every switching cycle. The worst-case condition of switching that leads to high rms ripple current is that of a square wave, which occurs for the case of zero fundamental voltage. This corresponds to a duty ratio, $d = 0.5$ and has been used in the computation of P_{ri} from a worst case power loss consideration.

By substituting quantities in p.u, the power loss due to the ripple component of current can be computed as,

$$P_{ri}(p.u.) = (i_{R_d,rms})^2 \cdot R_d \tag{33}$$

Total power loss in the damping resistor: Using (32) and (33), the total power loss in the damping resistor can be computed as,

$$P_T(p.u.) = P_{fu}(p.u.) + P_{ri}(p.u.) \tag{34}$$

2.4.2.4 Computation of $i_{R_d,rms}$

From (23), it can be observed that i_{R_d} is a linear combination of the state variables. So, the computation of i_{R_d} and hence $i_{R_d,rms}$ for a given duty ratio d requires solving the state equation (23). Since the ripple current is the parameter of interest, the computation need

to be done over a switching time interval, T_{sw} only. Following is the step-by-step procedure to compute i_{R_d} for a given duty ratio d:

1. The solution for (23) is given by [90],

$$\mathbf{x}(t) = e^{\mathbf{A}t}\mathbf{x}(0) + \int_0^t e^{\mathbf{A}(t-\tau)}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{35}$$

From (23), '**A**' is a 5x5 matrix for the LCL filter with SC-RL damping. So, to simplify the computations and to avoid matrix inversion error in the computation of the initial condition for the solution in later steps, the actual model in terms of $\mathbf{x}$(t) is transformed into its diagonal form in terms of $\bar{\mathbf{x}}$(t) using similarity transformation. The similarity transformation helps break down the vector $\mathbf{x}$(t) of larger dimension into multiple vectors $\bar{\mathbf{x}}$(t) of smaller dimensions which can be solved easily. Numerical values of the filter parameters are used for the transformation.

Let us consider a numerical example with $L_1 = 275\mu H$, $L_2 = 275\mu H$, $C_1 = 92\mu F$, $C_d = 92\mu F$, $R_d = 1.728\Omega$ and $L_d = 500\mu H$. For the chosen set of filter values, we have from (23),

$$\mathbf{A}= \begin{bmatrix} 0 & 0 & -3636.4 & 0 & 0 \\ 0 & 0 & 3636.4 & 0 & 0 \\ 10869.6 & -10869.6 & -6290.3 & 6290.3 & -10869.6 \\ 0 & 0 & 6290.3 & -6290.3 & 10869.6 \\ 0 & 0 & 2000 & -2000 & 0 \end{bmatrix};$$

$$\mathbf{B}= \begin{bmatrix} 3636.4 & 0 \\ 0 & -3636.4 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}; \mathbf{x}= \begin{bmatrix} i_i \\ i_g \\ v_C \\ v_d \\ i_{L_d} \end{bmatrix}; \mathbf{u}= \begin{bmatrix} v_i \\ v_g \end{bmatrix};$$

$\mathbf{C}$= [0 0 0.579 $-$ 0.579 0]; $\mathbf{D}$= [0 0]; $\mathbf{y}$= i_{R_d};

Similarity Transformation:

The eigen values of the above system are $\lambda_{1,2} = -4094.6 \pm 6242.5\jmath$, $\lambda_3 = 0$, $\lambda_{4,5} = -2195.8 \pm 5100.4\jmath$ and the eigen vector matrix is,

$$\mathbf{Q}= \begin{bmatrix} -0.25+0.07\jmath & -0.25-0.07\jmath & -0.707 & -0.18+0.19\jmath & -0.18-0.19\jmath \\ 0.25-0.07\jmath & 0.25+0.07\jmath & -0.707 & 0.18-0.19\jmath & 0.18+0.19\jmath \\ -0.17+0.50\jmath & -0.17-0.50\jmath & 0 & 0.15+0.37\jmath & 0.15-0.37\jmath \\ 0.72 & 0.72 & 0 & 0.80 & 0.80 \\ 0.24+0.13\jmath & 0.24-0.13\jmath & 0 & 0.21+0.16\jmath & 0.21-0.16\jmath \end{bmatrix};$$

Comparing $\mathbf{Q}$ with, $\mathbf{Q}$= [q_1 q_2 q_3 q_4 q_5], let, $\mathbf{P}^{-1}$ = [$\Re(q_1)$ $\Im(q_1)$ q_3 $\Re(q_4)$ $\Im(q_4)$]. Then,

$$\mathbf{P}= \begin{bmatrix} -1.72 & 1.72 & -1.26 & -2.37 & 6.80 \\ -3.33 & 3.33 & 2.24 & -2.62 & 2.53 \\ -0.71 & -0.71 & 0 & 0 & 0 \\ 1.55 & -1.55 & 1.14 & 3.39 & -6.14 \\ 3.097 & -3.10 & -1.36 & 1.09 & 2.16 \end{bmatrix};$$

The similarity transformation equations, $\bar{A} = PAP^{-1}$, $\bar{B} = PB$, $\bar{C} = CP^{-1}$, $\bar{D} = D$ and $\bar{X} = PX$ give,

$$\bar{\mathbf{A}}=\begin{bmatrix} -4094.6 & 6242.5 & 0 & 0 & 0 \\ -6242.5 & -4094.6 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -2195.8 & 5100.4 \\ 0 & 0 & 0 & -5100.4 & -2195.8 \end{bmatrix} = \begin{bmatrix} \bar{\mathbf{A}}_1 & 0 & 0 \\ 0 & \bar{\mathbf{A}}_2 & 0 \\ 0 & 0 & \bar{\mathbf{A}}_3 \end{bmatrix};$$

$$\bar{\mathbf{B}}=\begin{bmatrix} -6257.19 & -6257.19 \\ -12090.12 & -12090.12 \\ \text{- - - - - - - - - - - - - - - - - -} & \\ -2571.32 & 2571.32 \\ \text{- - - - - - - - - - - - - - - - - -} & \\ 5651.56 & 5651.56 \\ 11261.17 & 11261.17 \end{bmatrix} = \begin{bmatrix} \bar{\mathbf{B}}_1 \\ \bar{\mathbf{B}}_2 \\ \bar{\mathbf{B}}_3 \end{bmatrix};$$

$$\bar{\mathbf{C}}=[-0.51 \;\; 0.29 \;\; : \;\; 0 \;\; : \;\; -0.38 \;\; 0.21] = \left[\bar{\mathbf{C}}_1\bar{\mathbf{C}}_2\bar{\mathbf{C}}_3\right]; \quad \bar{\mathbf{D}}=[0 \;\; 0];$$

$$\bar{\mathbf{x}}=\begin{bmatrix} -1.72 & 1.72 & -1.26 & -2.37 & 6.80 \\ -3.33 & 3.33 & 2.24 & -2.62 & 2.53 \\ -0.71 & -0.71 & 0 & 0 & 0 \\ 1.55 & -1.55 & 1.14 & 3.39 & -6.14 \\ 3.097 & -3.10 & -1.36 & 1.09 & 2.16 \end{bmatrix} \begin{bmatrix} i_i \\ i_g \\ v_C \\ v_d \\ i_{L_d} \end{bmatrix} = \begin{bmatrix} \bar{\mathbf{x}}_1 \\ \bar{\mathbf{x}}_2 \\ \bar{\mathbf{x}}_3 \end{bmatrix}; \; \mathbf{u}= \begin{bmatrix} v_i \\ v_g \end{bmatrix};$$

Matrix $\bar{\mathbf{A}}$ shows that the fifth order system has been transformed into three systems – two of second order and one of first order. The state space representation of the reduced order systems is given by,

$$\dot{\bar{\mathbf{x}}}_l(t) = \bar{\mathbf{A}}_l\bar{\mathbf{x}}_l(t) + \bar{\mathbf{B}}_l\mathbf{u}(t) \tag{36}$$

where, l = 1,2,3 and the output equation is given by,

$$\mathbf{y}(t) = \bar{\mathbf{C}}\bar{\mathbf{x}}(t) + \bar{\mathbf{D}}\mathbf{u}(t) \tag{37}$$

2. The number of independent reduced order systems resulting from the similarity transformation depend on the nature of the poles. Each real pole and each set of complex conjugate poles lead to an independent system. For a SC-RL damped LCL filter, there can be one real pole and two sets of complex conjugate poles or three real poles and a set of complex conjugate poles depending on the choice of parameters. This can be observed from the pole-zero plot, Fig. 2.18. So, there are either 3 or 4 sets of independent equations for the SCRL damped LCL filter. The solution for each of the simpler vectors $\bar{\mathbf{x}}_\mathbf{l}$(t) is given by,

$$\bar{\mathbf{x}}_\mathbf{l}(\mathbf{t}) = \mathbf{e}^{\bar{\mathbf{A}}_\mathbf{l}\mathbf{t}}\bar{\mathbf{x}}_\mathbf{l}(\mathbf{0}) + \int_\mathbf{0}^\mathbf{t} \mathbf{e}^{\bar{\mathbf{A}}_\mathbf{l}(\mathbf{t}-\tau)}\bar{\mathbf{B}}_\mathbf{l}\mathbf{u}(\tau)\mathbf{d}\tau \tag{38}$$

where, l = 1,2,3 or l = 1,2,3,4 depending on the nature of the poles.

3. Considering the switching time period, T_{sw}, to be divided into n small sampling time intervals of duration T_{smpl}, the discrete-time equivalent of (38) is [90],

$$\bar{\mathbf{x}}_\mathbf{l}[\mathbf{m}+\mathbf{1}] = \mathbf{e}^{\bar{\mathbf{A}}_\mathbf{l}\mathbf{T}_\mathbf{smpl}}\bar{\mathbf{x}}_\mathbf{l}[\mathbf{m}] - \left(\int_\mathbf{0}^{\mathbf{T}_\mathbf{smpl}} \mathbf{e}^{\bar{\mathbf{A}}_\mathbf{l}\alpha}\mathbf{d}\alpha\right)\bar{\mathbf{B}}_\mathbf{l}\mathbf{u}[\mathbf{m}] \tag{39}$$

with, n = sample points in one switching cycle = $\dfrac{T_{sw}}{T_{smpl}}$.

n has been taken to be 200 for the numerical computations in the present work.

4. Using (39), $\bar{\mathbf{x}}_\mathbf{l}[\mathbf{m}]$ is computed at intervals of T_{smpl} for the required duty ratio, d. The computation of $\bar{\mathbf{x}}_\mathbf{l}[\mathbf{m}]$ requires the initial condition $\bar{\mathbf{x}}_\mathbf{l}[\mathbf{0}]$ and the inputs v_i and v_g. $\bar{\mathbf{x}}_\mathbf{l}[\mathbf{0}]$ is taken to be the equilibrium point at the desired duty ratio d. The computation and use of equilibrium point as the initial condition for solving the state equations is

explained after Step 5. Input v_i is given by (24) with $t_{on} = dT_{sw}$. Input v_g is the grid voltage corresponding to the chosen duty ratio and is given by, $V_{dc} \cdot (d - 0.5)$. This choice of v_g assumes that there is no current flowing between the inverter and the grid. i.e. the inverter just balances the grid. Since the switching ripple current is the parameter of interest and as the voltage drop in the filter is negligible, this assumption is considered valid.

5. From $\bar{\mathbf{x}}_\mathbf{l}$[m], $\mathbf{x}$[m] is found using inverse transformation. Then, using (23), i_{R_d}[m] can be computed as,

$$i_{R_d}[m] = \frac{(x_3[m] - x_4[m])}{R_d} = \frac{v_C[m] - v_d[m]}{R_d} \tag{40}$$

Equilibrium Points: For a given time period of computation, the equilibrium point gives the initial value for which the state would return to the same value at the end of the computation. The switching ripple component of currents and voltages are the parameters being computed. In steady state, assuming the fundamental component of currents and voltages to be constant over a switching time period, the switching ripple component will be at equilibrium. i.e. the switching ripple components of currents and voltages return to their initial value at the end of the switching time period. This is equivalent to invoking the inductor volt-sec balance and the capacitor charge-balance [91] over a switching cycle. The equilibrium points can be used as initial condition to compute successive discrete time values using (39) for a given duty ratio d. It may be noted that an approximation is made in the above discussion as the fundamental component of currents and voltages do change slightly though insignificantly over a switching time period. So, actually a quasi-steady state approximation is used.

Using (38) and considering T_{sw} to be the switching time period, we have

$$\begin{aligned} \bar{\mathbf{x}}_\mathbf{l}(\mathbf{T_{sw}}) &= e^{\bar{\mathbf{A}}_\mathbf{l}\mathbf{T_{sw}}}\bar{\mathbf{x}}_\mathbf{l}(\mathbf{0}) + \int_{\mathbf{0}}^{\mathbf{dT_{sw}}} \mathbf{e}^{\bar{\mathbf{A}}_\mathbf{l}(\mathbf{T_{sw}}-\tau)}\bar{\mathbf{B}}_\mathbf{l}\mathbf{u}(\tau)\mathbf{d}\tau \\ &\quad + \int_{dT_{sw}}^{T_{sw}} e^{\bar{\mathbf{A}}_\mathbf{l}(\mathbf{T_{sw}}-\tau)}\bar{\mathbf{B}}_\mathbf{l}\mathbf{u}(\tau)\mathbf{d}\tau \end{aligned} \tag{41}$$

In steady state – for a given duty ratio d – by invoking equilibrium, we have, $\bar{\mathbf{x}}_\mathbf{l}(\mathbf{T_{sw}}) = \bar{\mathbf{x}}_\mathbf{l}(\mathbf{0})$.

Using this in (41) and solving for $\bar{\mathbf{x}}_\mathbf{l}(\mathbf{0})$, the equilibrium points can be obtained as,

$$\begin{aligned}\bar{\mathbf{x}}_\mathbf{l}(\mathbf{0}) &= [\mathbf{I} - \mathbf{e}^{\bar{\mathbf{A}}_\mathbf{l}\mathbf{T_{sw}}}]^{-\mathbf{1}} \left\{ \int_{\mathbf{0}}^{\mathbf{dT_{sw}}} \mathbf{e}^{\bar{\mathbf{A}}_\mathbf{l}(\mathbf{T_{sw}}-\tau)} \bar{\mathbf{B}}_\mathbf{l}\mathbf{u}(\tau)\mathbf{d}\tau \right. \\ &\quad \left. + \int_{dT_{sw}}^{T_{sw}} e^{\bar{\mathbf{A}}_\mathbf{l}(\mathbf{T_{sw}}-\tau)} \bar{\mathbf{B}}_\mathbf{l}\mathbf{u}(\tau)\mathbf{d}\tau \right\} \end{aligned} \tag{42}$$

From (42), it can be observed that there is a possibility of matrix inversion error due to poles present at origin. The damped LCL filter has one pole at the origin. So, in the transformed state equations, one of the equations would lead to matrix inversion error. For the LCL filter with the proposed damping method, the inversion problem occurs always for the state variable which is a scaled sum of the currents through L_1 and L_2. This can be observed from the matrix $\bar{\mathbf{A}}$ and the vector $\bar{\mathbf{x}}$.

Let us assume an intial condition that,

$$i_{L_1} + i_{L_2} = 0 \tag{43}$$

Then, the state variable with the inversion problem has an initial condition of zero and,

$$i_{L_1} = -i_{L_2} \tag{44}$$

From Step 4 in the computation of $i_{R_d,rms}$, $v_i = v_g$. So, by symmetry, since $L_1 = L_2$, i_{L_1} should be equal to $-i_{L_2}$. So, our assumption of initial condition is valid. So, we can solve the system. It may be noted that we are avoiding the matrix inversion error through our knowledge of the physical circuit.

Computation of $i_{R_d,rms}$: The rms value of i_{R_d} for a given duty ratio d is,

$$i_{R_d,rms} = \sqrt{\frac{1}{n}\sum_{m=0}^{n}(i_{R_d}[m])^2} \tag{45}$$

Knowing $i_{R_d,rms}$ for $d = 0$ to 1 for a quasi-steady state condition, the rms switching ripple current in the damping resistor over one fundamental cycle of time period T, for a sinusoidally varying inverter output voltage is given by,

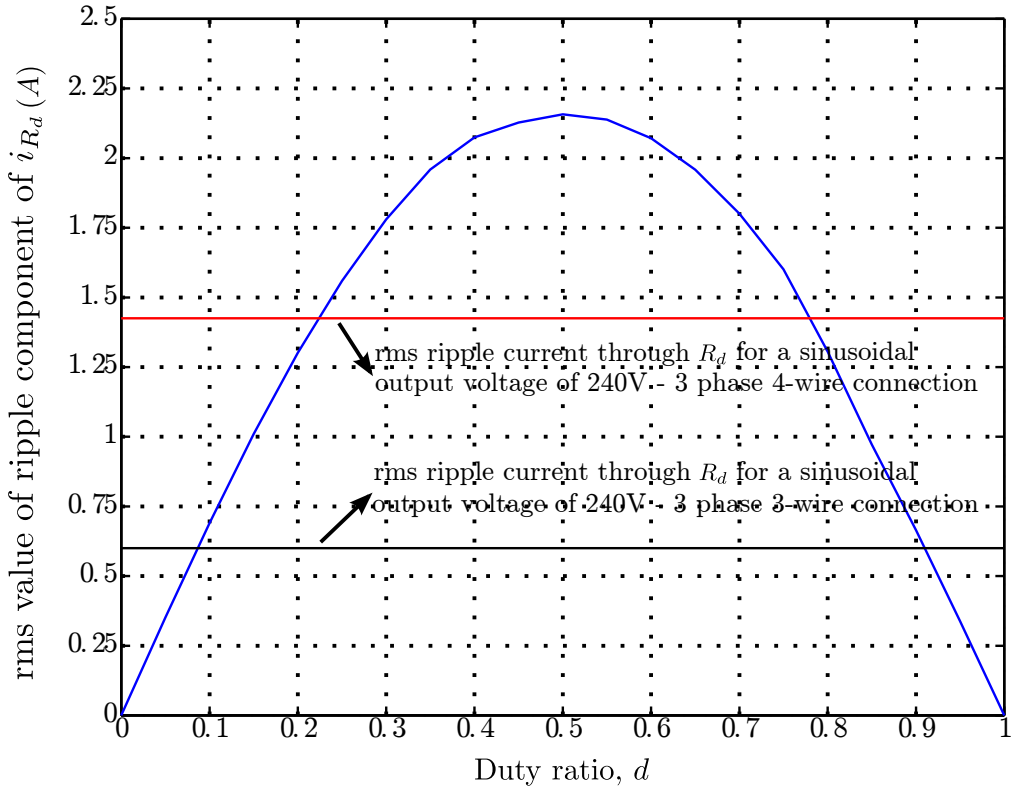


Figure 2.10: Variation of rms value of ripple component of i_{R_d} with duty ratio for $L_d = 500\mu H$. The rms ripple current for a sine output voltage is also shown for the 3-phase 3-wire and 3-phase 4-wire cases.

$$\text{rms switching ripple current over a fundamental cycle} = \sqrt{\frac{1}{T}\sum_{j=0}^{p}(i_{R_d,rms}(j))^2\ T_{sw}} \quad (46)$$

Where, p is the number of switching periods within T given by, T/T_{sw} and, $i_{R_d,rms}(j)$ is the rms value of the switching ripple current during the j^{th} switching cycle.

Fig. 2.10 shows the variation of rms value of ripple component of i_{R_d} for different values of d. It can be seen that the worst case ripple current appears at $d = 0.5$. Hence, the ripple current loss at $d = 0.5$ has been considered in this work as the value of P_{ri}. The rms ripple current for a sinusoidal variation of output voltage of 240 V is also shown, which is lower than the worst case rms ripple current. Fig. 2.10 also shows the comparison of rms ripple current through R_d for the 3-phase 3-wire case and 3-phase 4-wire case for sine-triangle modulation. The 3-phase 4-wire case can be observed to have more ripple and hence is considered in the

present work. The component selection thus can be used for a 3-phase 3-wire case also. The power loss would be lower in the 3-phase 3-wire case.

P_T and QF expressions for the R-damping and SC-R damping schemes can be derived in a similar manner as explained above and has been used for comparison of damping schemes in the following Section. The various expressions for R and SC-R damping schemes appear in Appendix D. For these schemes the state space model has a lower order as the energy storage elements are fewer.

The above described state space based computation of power loss due to the switching ripple current is simple compared to the usual simulation methods. In usual simulation, the system needs to be simulated through the transient and steady state durations for arriving at the results which involves several hundred switching cycles. The quasi-steady state approximation and the concept of equilibrium points help compute the result directly through computations done for a single switching cycle.

2.4.3 Comparison of Damping Schemes

Table 2.2 compares the power loss in the three mentioned damping schemes for the same damping level given by $QF = 3$. Expressions (25),(32)-(34) shown in the last Section are used for the SC-RL scheme. Similar expressions were derived for the other schemes also for the purpose of comparison. The equations used for R-damping and SC-R damping appear in Appendix D. The base values are given in Table 2.3. It can be observed that the power loss is very low in the case of SC-RL damping scheme. For example, in a 40 kVA three phase inverter, the power loss in each of the damping resistors of a three-phase inverter would be 205 W, 107 W and 9 W respectively for the R, SC-R and SC-RL damping schemes. In view of this, the SC-RL damping scheme has been chosen for the high power experimental set-up.

A few salient points related to the comparison table are listed here:

- P_{ri} is less in the case of SC-R damping as compared to R-damping as expected.
- P_{fu} is less in the case of SC-RL damping as compared to SC-R damping as expected.
- The value of $|i_g/v_i|@f = f_{sw}$ changes from that of the ideal LCL filter on addition of the damping components. The ideal value is -71 dB for the chosen LCL filter. The deviation from ideal value is more in the case of R damping as an additional zero gets

Parameter	**R Damping**	**SC-R Damping**	**SC-RL Damping**
f_{sw}	9.75kHz	9.75kHz	9.75kHz
f_r	1kHz	1kHz	1kHz
$L_1(p.u.)$	0.02	0.02	0.02
$L_2(p.u.)$	0.02	0.02	0.02
$C(p.u.)$	0.25	-	-
$C_1(p.u.)$	-	0.125	0.125
$C_d(p.u.)$	-	0.125	0.125
$R_d(p.u.)$	0.0718	0.484	0.4
$L_d(p.u.)$	-	-	0.0201
$\lvert i_g/v_i \rvert @ f = f_{sw}$	-59 dB	-65 dB	-65 dB
QF	3.0	3.0	3.0
$P_{fu}(\%)$	0.45	0.75	0.0016
$P_{ri}(\%)$	1.09	0.05	0.065
$P_T(\%)$	1.54	0.80	0.0666

Table 2.2: Comparison of R, SC-R and SC-RL damping schemes.

added into the system in R damping which changes the nature of the high frequency attenuation characteristics.

- The minimum required attenuation is -63.33 dB for the chosen LCL filter to follow the IEEE standards. It can be seen that SC-R and SC-RL damping satisfies this.

2.4.4 SC-RL Damping Circuit Design

The system under consideration being of higher order, adding one component at a time to the design would lead to a simplified procedure of component selection. Also, a multi-parameter numerical optimization approach to the damping circuit may not provide adequate design insight. So, the approach of adding damping components in steps to the ideal LCL filter has been used. At each step, the selection of the component being added is based on the objective of maintaining both QF and P_T to be low. First, L_1, L_2 and C are chosen for an ideal LCL filter as explained in Section 2.2. Then, the filter capacitor C is split into C_1, C_d and the damping resistance R_d is added in series with C_d to get a SC-R damped LCL filter as described in Section 2.4.4.2. Finally, the damping inductor L_d is added to the SC-R scheme to convert it into SC-RL damping scheme using the method given in Section 2.4.4.3. The procedure takes into account the influence of switching frequency, resonance frequency and the choice of inductance and capacitance values of the LCL filter on the damping component selection. The proposed method damps the additional resonance due to the damping components also.

The inverter power level and the ac per phase grid voltage are chosen as the base values. The frequency base is chosen to be the fundamental grid frequency. These are used to normalize the filter parameters. Table 2.3 lists the base values used. The inverter is considered to have a dc bus voltage of 800 V and switching at 9.75 kHz.

2.4.4.1 Selection of Ideal LCL Filter Components: Choice of Resonance Frequency, ω_r

The selection of L_1, L_2 and C has been discussed in Section 2.2. The selection procedure requires a choice of ω_r. The choice of ω_r depends on the fundamental frequency, ω_{fu}, and switching frequency, ω_{sw}. A good choice of resonance frequency would be to set it in between the fundamental frequency and switching frequency. This frequency separation ensures that

the various components of current - the fundamental, resonance and ripple at switching frequency, multiples and sidebands - do flow primarily as shown in Fig. 2.7. For example, in an inverter switching at 9.75 kHz and interfaced to a 50 Hz grid, a resonance frequency of 1 kHz would be a reasonable choice as the resonance frequency is about a decade below the switching frequency and well above the fundamental frequency.

Ideally, the resonance frequency can be selected to be, $\omega_r = \sqrt{\omega_{fu} \cdot \omega_{sw}}$. However, it should be noted that a lower value of resonance frequency would require a higher value of L or C or both as can be observed from (3). This increases the filter size and cost. So, practically, one might want to set ω_r to be higher than $\sqrt{\omega_{fu} \cdot \omega_{sw}}$. Further, the control bandwidth is set to less than the resonance frequency in case of passive damping. This requires the resonance frequency to be as high as possible. From this perspective too, the designer might want to set ω_r to be higher than $\sqrt{\omega_{fu} \cdot \omega_{sw}}$.

2.4.4.2 Selection of Components for SC-R Damping Scheme

With the selected ideal LCL filter parameters, we proceed to find C_1, C_d and R_d. As explained earlier, the QF and P_T should both be kept low. Let, $C_d = a_C \cdot C_1$. Fig. 2.11 shows the QF curve for varying values of a_C. For every value of a_C, R_d has been varied to get the minimum possible QF. Using the R_d that gives the minimum QF for a given a_C, P_T is computed. Fig. 2.12 shows the P_T curves for varying switching frequencies. ω_r has been taken to be the geometric mean of the fundamental and switching frequency in all cases. The QF curve is the same for varying switching and resonance frequencies.

From Fig. 2.11 and Fig. 2.12, it can be seen that both QF and P_T are low around $a_C = 1$. The ratio in which C is split into C_1 and C_d is a trade-off between damping and power loss in the damping resistor. An a_C value in the range 0.75 to 1.5 would be a good choice. For the present work, a_C is taken to be 1. The corresponding value of R_d is very close to $\sqrt{L/C}$ and can be approximated to it. The chosen filter parameters are listed in Table 2.4.

The SC-R damped LCL filter has four poles. Two of the four poles are real and the other two are complex conjugates. The complex conjugate pair is the one that decides QF. For the suggested choice of $C_1 = C_d$ and $R_d = \sqrt{L/C}$, the complex conjugate pair can be shown to be $s = \omega_r(-0.225 \pm 1.113\jmath)$. This implies that, for the suggested design methodology, the complex conjugate poles always lie along a line of constant damping. Hence, the choice of switching and resonance frequency does not affect the quality factor for the SC-R passive

Quantity	**Notation**	**Base Value**
Power	P_{base}	40 kVA
Voltage	V_{base}	240 V
Current	I_{base}	55.6 A
Impedance	Z_{base}	4.32 Ω
Inductance	$L_{base} = Z_{base}/(2 \cdot \pi \cdot 50)$	14 mH
Capacitance	$C_{base} = 1/(Z_{base} \cdot 2 \cdot \pi \cdot 50)$	737 μF
Frequency	ω_{base}	$2 \cdot \pi \cdot 50\ rad/s$

Table 2.3: Base values used for the filter analysis.

Parameter	$\mathbf{L_1 = L_2}$	$\mathbf{C_1 = C_d}$	$\mathbf{R_d}$	$\omega_\mathbf{r}$	$\omega_\mathbf{sw}$
Per Unit Value	0.02	0.125	0.4	20	195
Physical Value	275μH	92μF	1.728Ω	6283 rad/s	61261 rad/s

Table 2.4: Filter Parameter Values for SC-R Passive Damping.

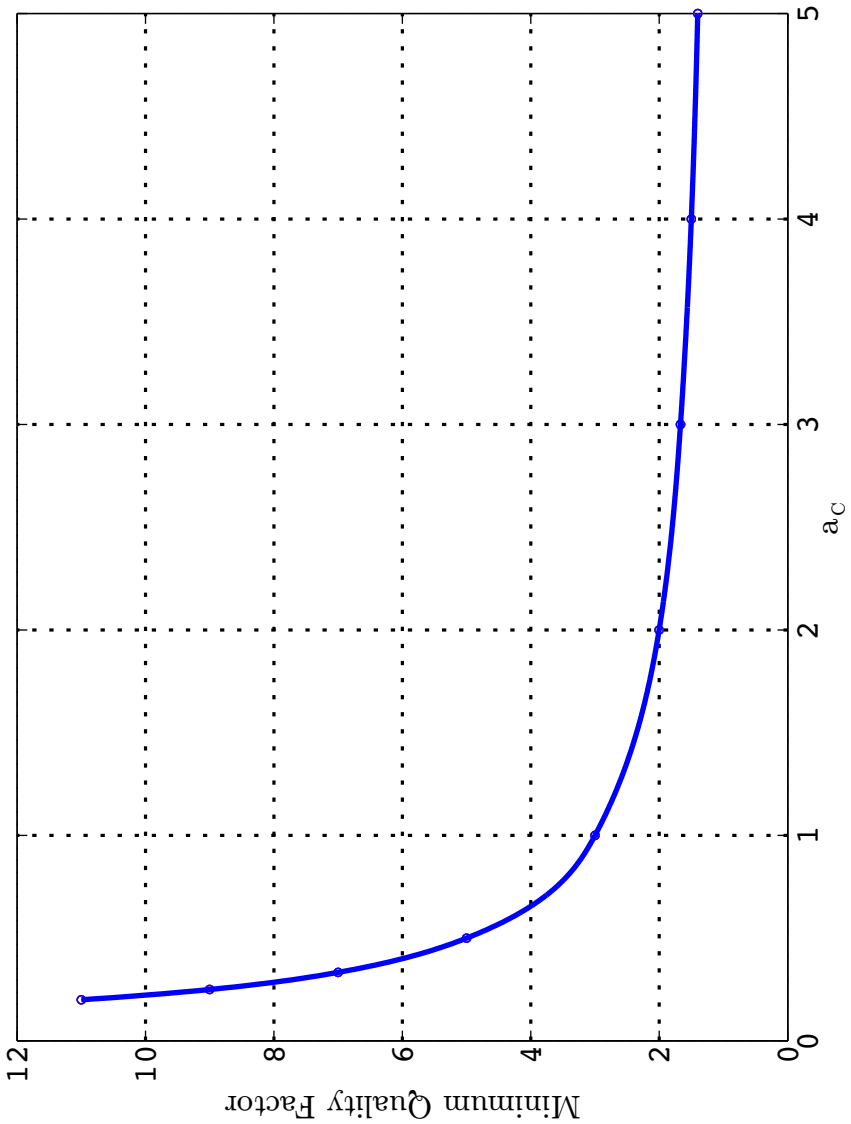


Figure 2.11: Variation of minimum QF with $a_C = C_d/C_1$ including the effect of resonance frequency shift. The plot uses $\omega_r = \sqrt{\omega_{fu} \cdot \omega_{sw}}$, rated 3-phase power (power base) of 250 kVA for the inverter and nominal grid voltage (voltage base, frequency base) = 240 V, 50 Hz. The minimum quality factor curve does not change with switching frequency.

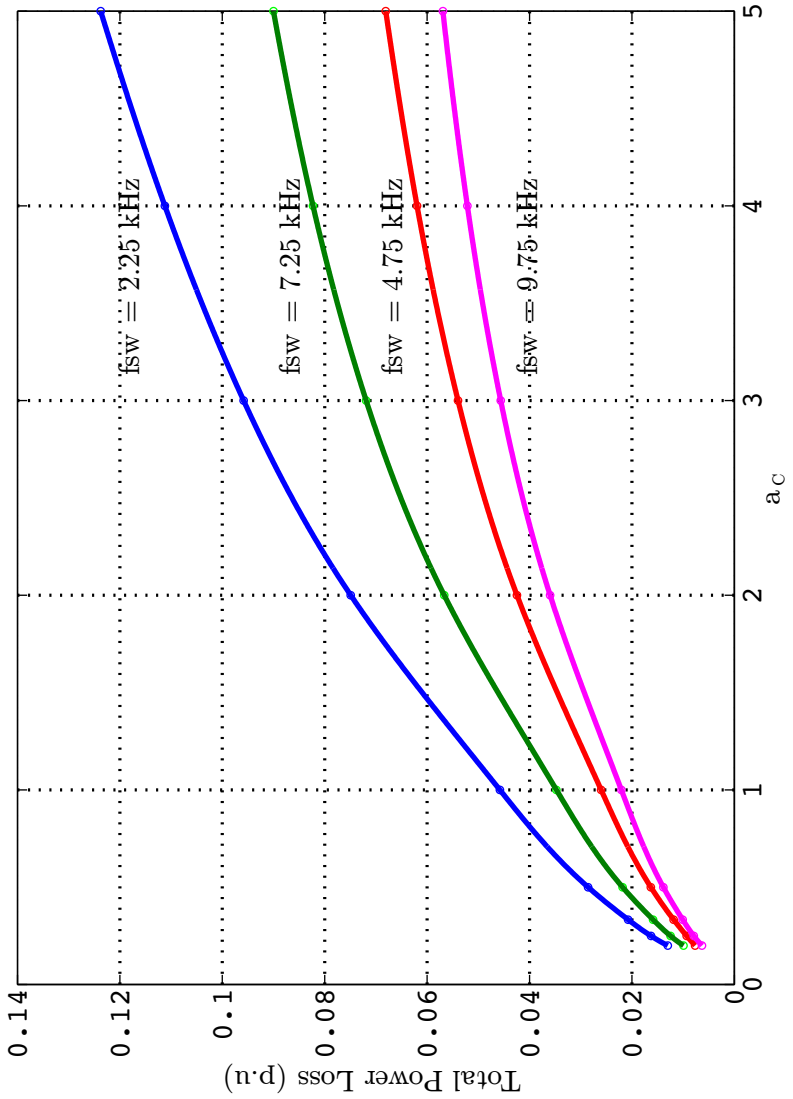


Figure 2.12: Variation of P_T with $a_C = C_d/C_1$ for varying values of switching frequency. The plot uses $\omega_r = \sqrt{\omega_{fu} \cdot \omega_{sw}}$, inverter rated 3-phase power (power base) = 250 kVA and nominal grid voltage (voltage base, frequency base) = 240 V, 50 Hz.

damping component selection method provided above. This also explains the QF curve in Fig. 2.11 remaining the same for varying switching and resonance frequencies.

Fig. 2.13 shows the pole-zero plot for a SC-R damped LCL filter with $C_1 = C_d$ and R_d varying from $0.5\sqrt{L/C}$ to $10\sqrt{L/C}$. It can be observed that the system has maximum damping when R_d is around $\sqrt{L/C}$. The solid arrows in the figure indicate the poles and zeros corresponding to the component selection $C_1 = C_d$ and $R_d = \sqrt{L/C}$.

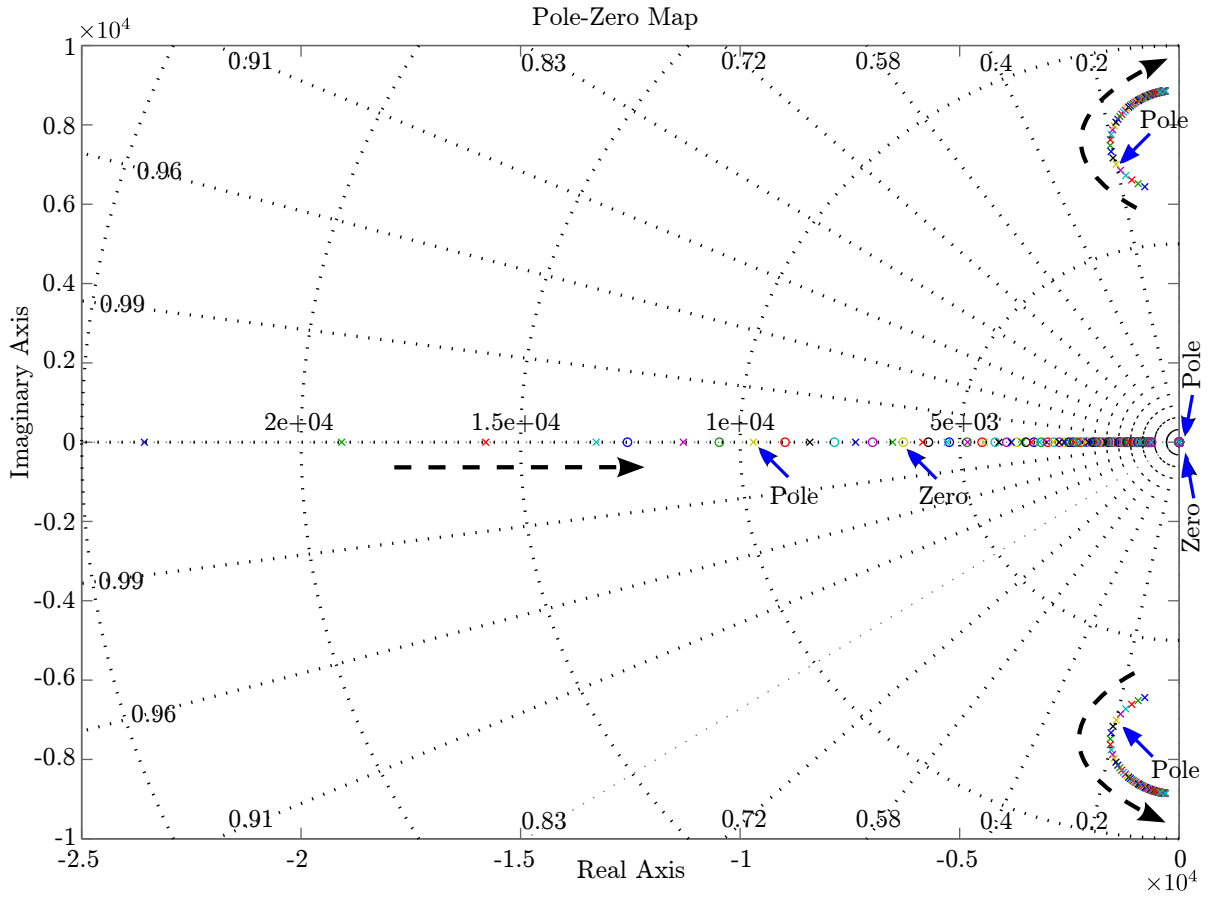


Figure 2.13: Pole-Zero plot of SC-R damped LCL filter for varying R_d. R_d is varied from $0.5\sqrt{L/C}$ to $10\sqrt{L/C}$. The system has maximum damping when R_d is around $\sqrt{L/C}$. The dashed arrows indicate pole movement for increasing R_d. The solid arrows indicate poles and zeros for the component selection $C_1 = C_d$ and $R_d = \sqrt{L/C}$.

2.4.4.3 Selection of L_d for SC-RL Damping Scheme

The QF and P_T are the determining factors for selection of L_d also. As indicated in Section 2.4.2.2, $K_{L_d} = \omega_r/\omega_{fu} = \omega_r(p.u) = 20$ gives the minimum QF. Using the expressions (32) - (34), power loss can be plotted as a function of damping impedance factor K_{L_d} as shown in Fig. 2.14. The power loss curve shows that $K_{L_d} = 20$ is a good choice in terms of P_T also. This suggests a relationship between K_{L_d} and ω_r.

The choice of $K_{L_d} = 20$ assumes that the resonance frequency does not vary after the ideal LCL filter is modified to include the passive damping components. So, the value of K_{L_d} is tuned numerically to capture the effect of the shift in the resonance frequency. To tune the value of K_{L_d} numerically, a bode plot of the transfer function V_C/V_i given by (26) was plotted for $K_{L_d} = 1$ to 30. From the peaks of the bode plots computed numerically for $K_{L_d} = 1$ to 30, an exact plot of quality factor as a function of damping impedance factor K_{L_d} is obtained and is shown in Fig. 2.15. A numerical approach by plotting the exact bode gain plots is used because an analytical solution would need solving a fifth order characteristic equation.

The plot shows the tuned value of K_{L_d} that gives the lowest QF to be 10.5 including the effect of shift in the resonance frequency due to the addition of the damping components. Fig. 2.14, $K_{L_d} = 10.5$ is suitable in terms of P_T also. The choice of $K_{L_d} = 10.5$ yields the value of the damping inductor, $L_d = 0.04$ p.u. All the computations being in per-unit, the value arrived at is valid for converters for a wide range of power rating and switching at 9.75 kHz with resonance frequency being set at 1 kHz. The proposed component selection method for SC-RL damping scheme is useful for the power range of a few tens of kVA to around 1 MVA. At higher power levels, it might not be possible to switch the inverter at 9.75 kHz. The effect of use of lower switching frequencies is considered in the next Section.

2.4.4.4 Damping Impedance Factor (K_{L_d}) - Physical Implication and Some Observations

The damping impedance factor is,

$$K_{L_d} = \frac{R_d}{\omega_{fu} \cdot L_d} \tag{47}$$

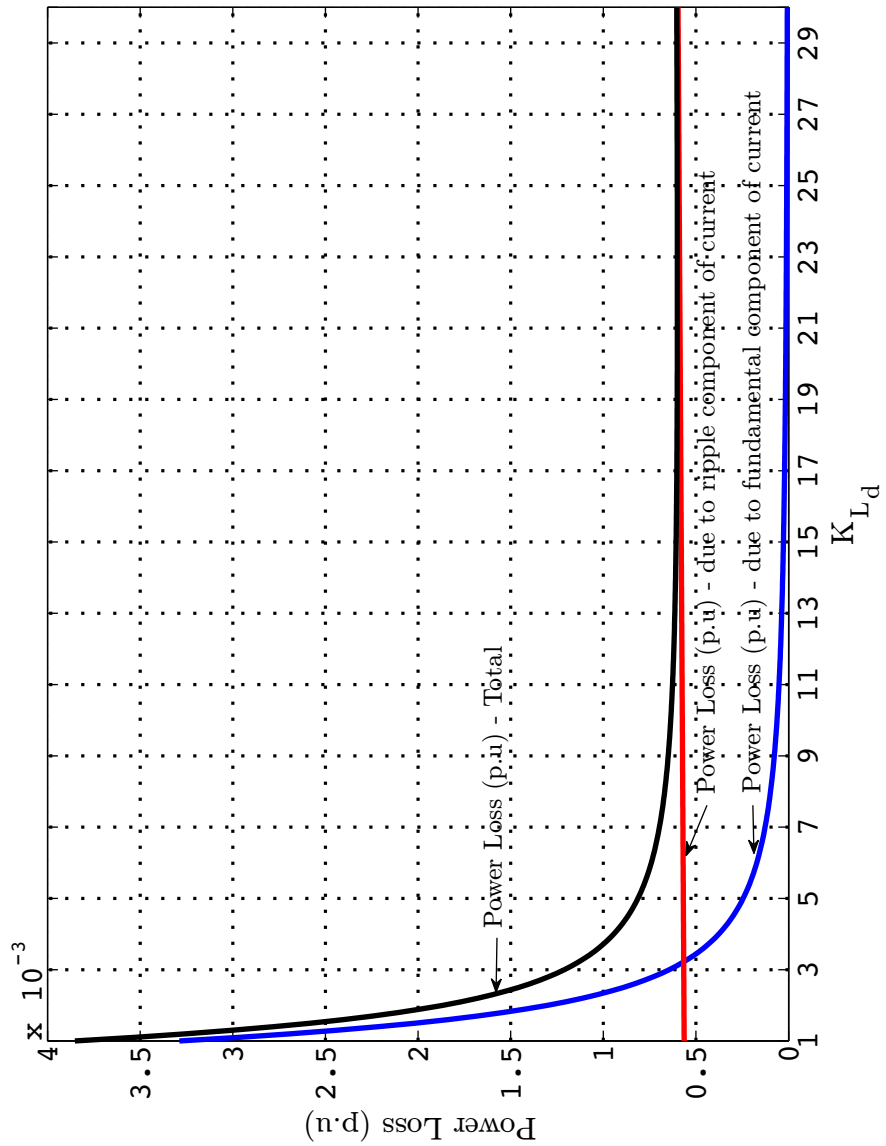


Figure 2.14: Variation of different components of power loss in the damping resistors versus damping impedance factor K_{L_d}.

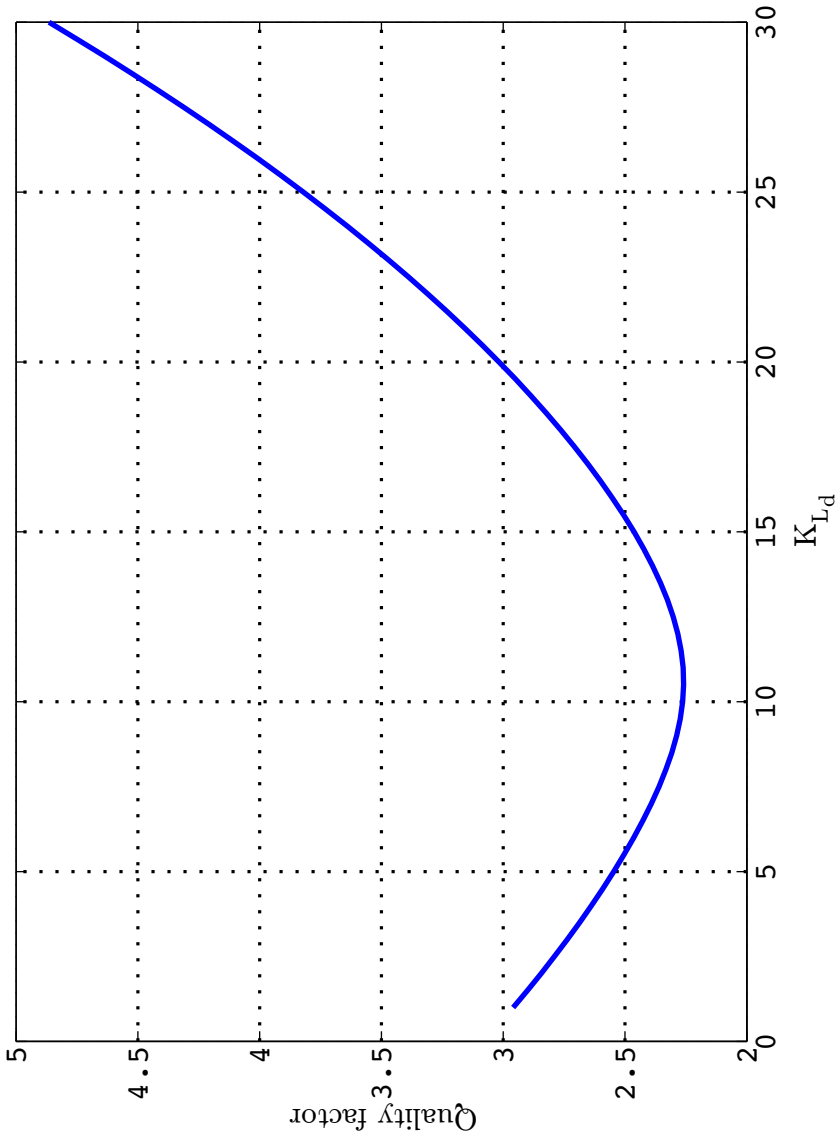


Figure 2.15: QF determined numerically from the magnitude bode plot versus damping impedance factor K_{L_d} including the effect of resonance frequency shift.

The physical implication of varying K_{L_d} is that it changes the impedance offered at resonance frequency by the parallel combination of R_d and L_d. For example, a choice of K_{L_d} $= \omega_r/\omega_{fu}$ means that the impedance of L_d equals the value of R_d at ω_r. Thus the effective impedance at ω_r is $R_d/2$. As K_{L_d} decreases, the effective impedance at ω_r moves close to R_d which is desirable. But, the value of K_{L_d} cannot be reduced arbitrarily as it would soon lead to an increase in the fundamental frequency losses as can be observed from Fig. 2.14. Also, QF does not vary linearly with K_{L_d} which can be observed from Fig 2.15.

It is numerically observed that K_{L_d} can practically be chosen to be,

$$K_{L_d} = \frac{1}{2} \cdot \frac{\omega_r}{\omega_{fu}} \tag{48}$$

The value of K_{L_d} that gives the minimum QF and low P_T is observed to be close to (48) and can be approximated to it. This has been seen to hold good for a wide range of switching frequencies and wide choice of inductance and capacitance values. Fig. 2.16 and Fig. 2.17 plot QF vs K_{L_d} and P_T vs K_{L_d} respectively for switching frequencies in the range 2 kHz to 10 kHz. It can be seen that with K_{L_d} chosen using (48), the QF is very close to minimum and power loss does not exceed the knee point of the curve. This can readily be applied to inverters of power level up to around 1 MW and operating at switching frequencies in the range 2 kHz to 10 kHz with voltage drop across the inductors (L_1 + L_2) ranging from 4% to 17.5%.

The minimum QF obtained using the choice of K_{L_d} given by (48) can be reasoned out using the pole zero plot. The SC-RL damped LCL filter has five poles. Apart from the one pole at origin, the other four poles can be two sets of complex conjugates or a set of complex conjugates and a set of real poles. For the suggested choice of K_{L_d} given by (48) and other parameters as in Section 2.4.4.2, the four poles turn out to be two sets of complex conjugates that are equal given by $s = \omega_r[-(1/2) \pm (\sqrt{3/2})j]$ – twin poles at each location. These poles always lie along a constant damping line irrespective of the choice of resonance and switching frequency. Also, the zeros of (26) can also be shown to always lie along constant damping lines. This leads to a fixed and minimum quality factor as can be observed from Fig. 2.16. So, the validity of the design is based only on P_T curve. As far as the suggested value of K_{L_d} is at or below the knee of the P_T curve, the power loss does not become excessive and the design holds good. For switching frequencies from 2 kHz and above, the suggested K_{L_d} value is at or below the knee point of the P_T curve as shown in Fig. 2.17 and hence results in a valid design. Further, the twin complex conjugate poles indicate that the additional resonance

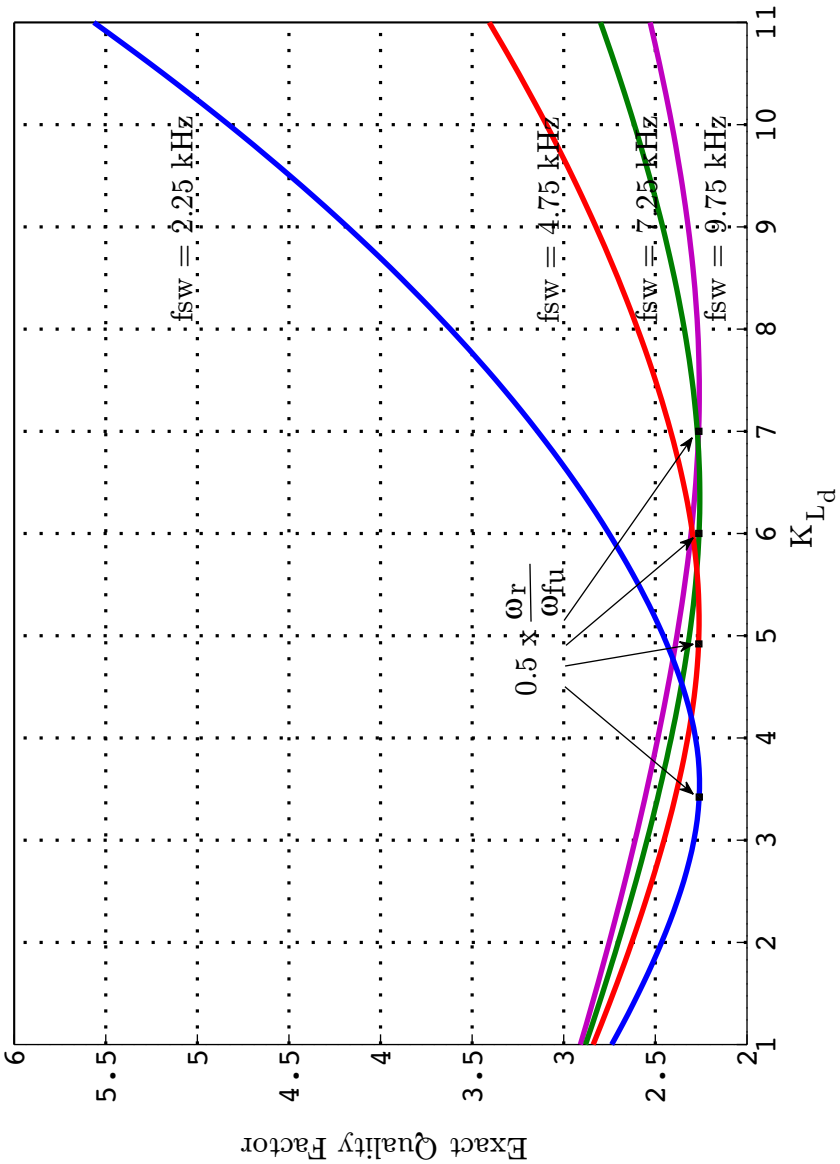


Figure 2.16: Variation of QF with K_{L_d} including the effect of resonance frequency shift for varying values of switching frequency. The plot uses $\omega_r = \sqrt{\omega_{fu} \cdot \omega_{sw}}$, inverter rated 3-phase power (power base) = 250 kVA and nominal grid voltage (voltage base, frequency base) = 240 V, 50 Hz.

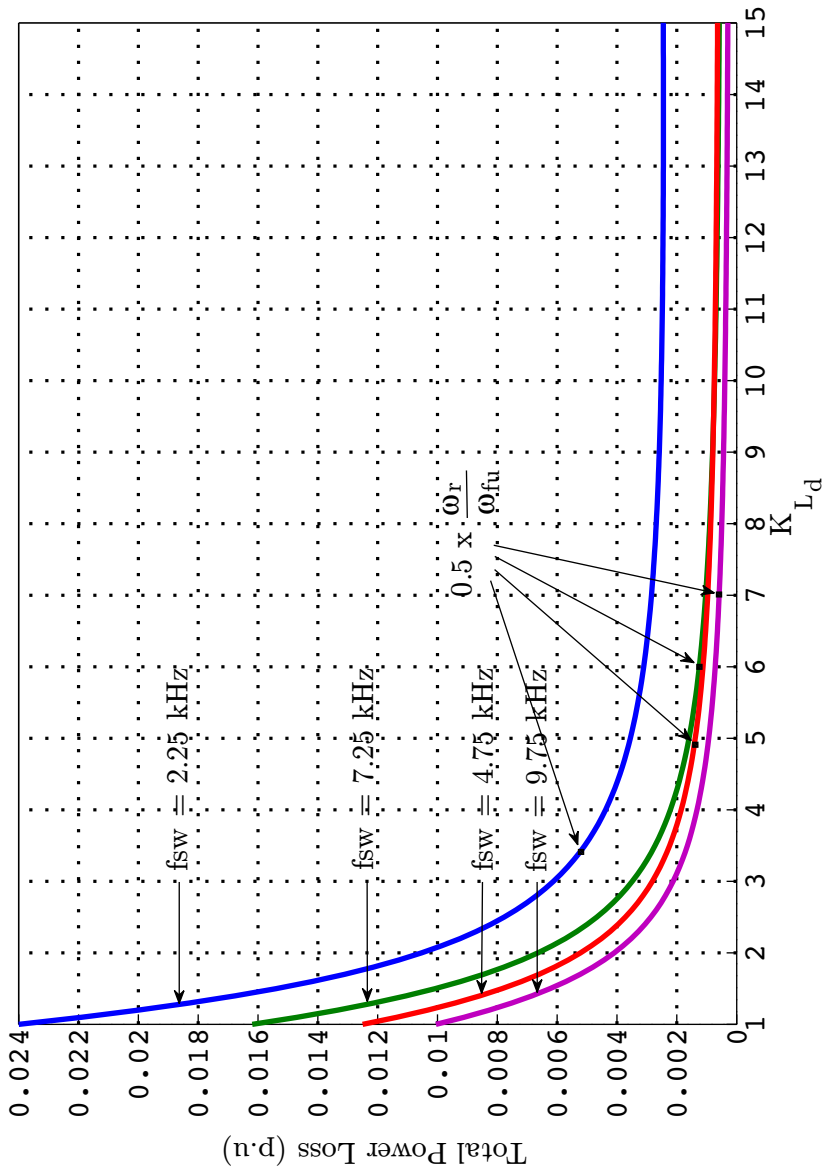


Figure 2.17: Variation of P_T with K_{L_d} for varying values of switching frequency. The plot uses $\omega_r = \sqrt{\omega_{fu} \cdot \omega_{sw}}$, inverter rated 3-phase power (power base) = 250 kVA and nominal grid voltage (voltage base, frequency base) = 240 V, 50 Hz.

introduced into the circuit due to the damping components too has the same frequency as the series resonance and hence is damped.

Fig. 2.18 shows the pole-zero plot for a SC-RL damped LCL filter with $C_1 = C_d$, $R_d = \sqrt{L/C}$ and K_{L_d} varying from $0.5 \times \left[\frac{1}{2} \cdot \frac{\omega_r}{\omega_{fu}}\right]$ to $10 \times \left[\frac{1}{2} \cdot \frac{\omega_r}{\omega_{fu}}\right]$. It can be observed that the system has maximum damping when K_{L_d} is $\frac{1}{2} \cdot \frac{\omega_r}{\omega_{fu}}$. The solid arrows in the figure indicate the poles and zeros corresponding to $K_{L_d} = \frac{1}{2} \cdot \frac{\omega_r}{\omega_{fu}}$.

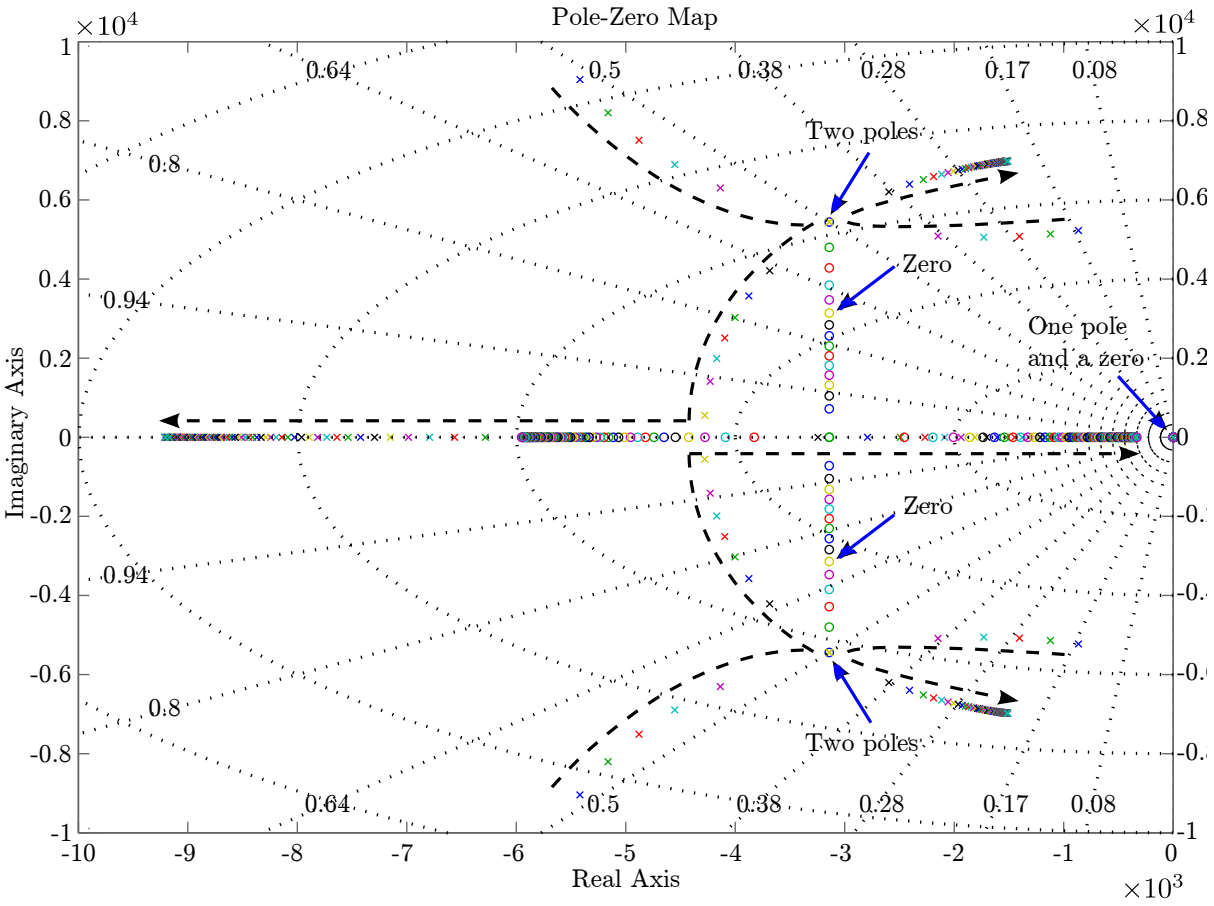


Figure 2.18: Pole-Zero plot of SC-RL damped LCL filter for varying K_{L_d}. K_{L_d} is varied from $0.5 \times \left[\frac{1}{2} \cdot \frac{\omega_r}{\omega_{fu}}\right]$ to $10 \times \left[\frac{1}{2} \cdot \frac{\omega_r}{\omega_{fu}}\right]$.The system has maximum damping when K_{L_d} is $\frac{1}{2} \cdot \frac{\omega_r}{\omega_{fu}}$. The dashed arrows indicate pole movement for increasing K_{L_d}. The solid arrows indicate poles and zeros for $K_{L_d} = \frac{1}{2} \cdot \frac{\omega_r}{\omega_{fu}}$.

2.4.5 Summary of Component Selection Procedure for an SC-RL Damped LCL Filter

The following steps summarize the selection procedure for the various components of an output SC-RL damped LCL filter in a grid-connected inverter. The system is assumed to be connected in a 3-phase 4-wire configuration.

1. Select a desired ω_{sw} based on the device restrictions and thermal considerations. A ω_{sw} that does not result in even harmonics in the output voltage spectrum can reduce the minimum value of inductance required.

2. Choose a resonance frequency, ω_r which is well separated from both ω_{fu} and ω_{sw}. Ideally, ω_r can be chosen to be, $\omega_r = \sqrt{\omega_{fu} \cdot \omega_{sw}}$. However, a slightly higher value of ω_r might be used to reduce the system size and cost.

3. Compute L_{min1}(p.u.) using the relation, $L_{min1} = \dfrac{|V_i(\jmath\omega_{dom})|}{|I_g(\jmath\omega_{dom})|\ |\jmath\omega_{dom}|\ |1-(\omega_{dom}/\omega_r)^2|}$. This is required for the ideal LCL filter without the damping components to comply with the IEEE standards.

4. $L_{max} = 0.1$ p.u. This is required for a practical choice of dc bus voltage.

5. $L_1 = L_2 = L/2$ from the inductor cost perspective. L_2 includes the grid inductance.

6. Choose a value of C_{max} based on the desired limit on the reactive power requirement of the filter capacitor.

7. $L_{min2} = \dfrac{4}{\omega_r^2 C_{max}}$.

8. Choose any value of L that satisfies, $max(L_{min1}, L_{min2}) \leq L \leq L_{max}$.

9. $C = \dfrac{4}{\omega_r^2 L}$.

10. $C_1 = C_d = C/2$ and $R_d = \sqrt{L/C}$. This selection of C_1, C_d and R_d gives a low value of QF and P_T in an SC-R damped LCL filter.

11. $K_{L_d} = \dfrac{1}{2} \cdot \dfrac{\omega_r}{\omega_{fu}}$ for QF and P_T to be very low in a SC-RL damped LCL filter. Correspondingly, $L_d = \dfrac{R_d}{K_{L_d} \cdot \omega_{fu}}$ or $L_d = L_1 + L_2 = L$.

12. Check if with the damping components included, the filter gives the required attenuation for the dominant harmonic component. If the attenuation is less, increase L slightly and repeat steps 9 to 12 again.

2.4.6 Experimental Results

The experimental evaluation was carried out at an ac output voltage of 100 Vrms with a dc bus voltage of 400 V using the experimental set-up mentioned in Section 1.4. The switching frequency used is 10kHz. Fig. A.2(a) shows the inverter setup along with the output LCL filter and its associated SC-RL passive damping circuitry. The various filter components used in the experimental validation are listed in Table 2.5. The table assumes the base values of power, voltage, current and frequency to be 50 kVA, 240 V, 70 A and $(2 \cdot \pi \cdot 50) rad/s$ respectively. K_{L_d} was varied in the range 1 to 35 using series-parallel combinations of damping inductors. The various damping inductor values used and the equivalent K_{L_d} are listed in Table 2.6.

Parameter	$\mathbf{L_1 = L_2}$	$\mathbf{C_1 = C_d}$	$\mathbf{R_d}$	$\omega_\mathbf{r}$
Per Unit Value	0.05	0.032	1.24	25
Physical Value	550μH	30μF	4.3Ω	$2 \cdot \pi \cdot 1250 rad/s$

Table 2.5: Filter component values used in the experimental set-up.

$\mathbf{L_d}$ $(\mu\mathbf{H})$	400	520	600	650	780	975	1170	1560	2000	4000	6000	9000
$\mathbf{K_{L_d}}$	34.2	26.3	22.8	21.0	17.5	14.0	11.7	8.8	6.8	3.4	2.3	1.5

Table 2.6: List of damping inductor values and equivalent damping impedance factor K_{L_d} used for measurements.

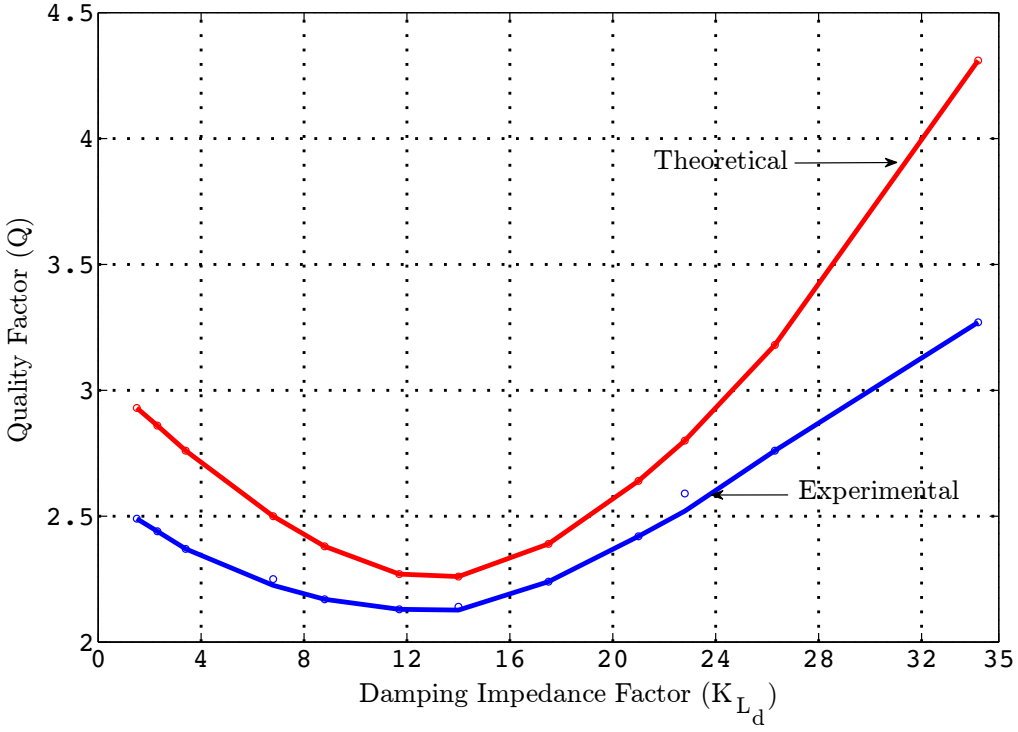


Figure 2.19: Theoretical and experimental quality factor curves as a function of the damping impedance factor K_{L_d}.

2.4.6.1 Measurement of QF

A network analyser (AP Instruments - Model 200) is used to experimentally determine the quality factors for various values of K_{L_d}. Fig. 2.19 shows the theoretical and experimental quality factor curves. The deviations in the quality factor from the theoretical values can be attributed to the component tolerances and the non-idealities associated with the circuit elements. In particular, it can be observed that the experimental curve shows the damping to have improved over the theoretical prediction which is expected as the ESR of the inductor and capacitor and the wire resistances give additional damping.

2.4.6.2 Measurement of Power Loss (P_{fu} and P_{ri})

To experimentally validate the fundamental frequency power loss P_{fu} in the filter damping resistor, the inverter should be connected to the grid through the SC-RL damped LCL filter.

Equivalently, the current circulation procedure developed in Chapter 3 can also be used as only the fundamental frequency component of current in the damping resistor is of interest. Hence, the current circulation procedure is used in the present work. A digital power meter (Yokogawa - WT1600) is used to experimentally measure the power loss due to fundamental frequency component of current through the damping resistor (R_d).

The worst case ripple current power loss is to be calculated at a duty ratio of $d = 0.5$. To experimentally validate the power loss in the damping resistor due to the worst case ripple current P_{ri}, the grid is shorted i.e. the grid is disconnected and the grid-side inductors are connected to mid-point of the dc bus capacitor. Then, a 50% duty cycle pulse is applied at the output of the inverter and the loss due to the worst case ripple current in the damping resistor is measured using the data of current from high bandwidth LEM current sensors captured through LeCroy WaveRunner 6050 oscilloscope.

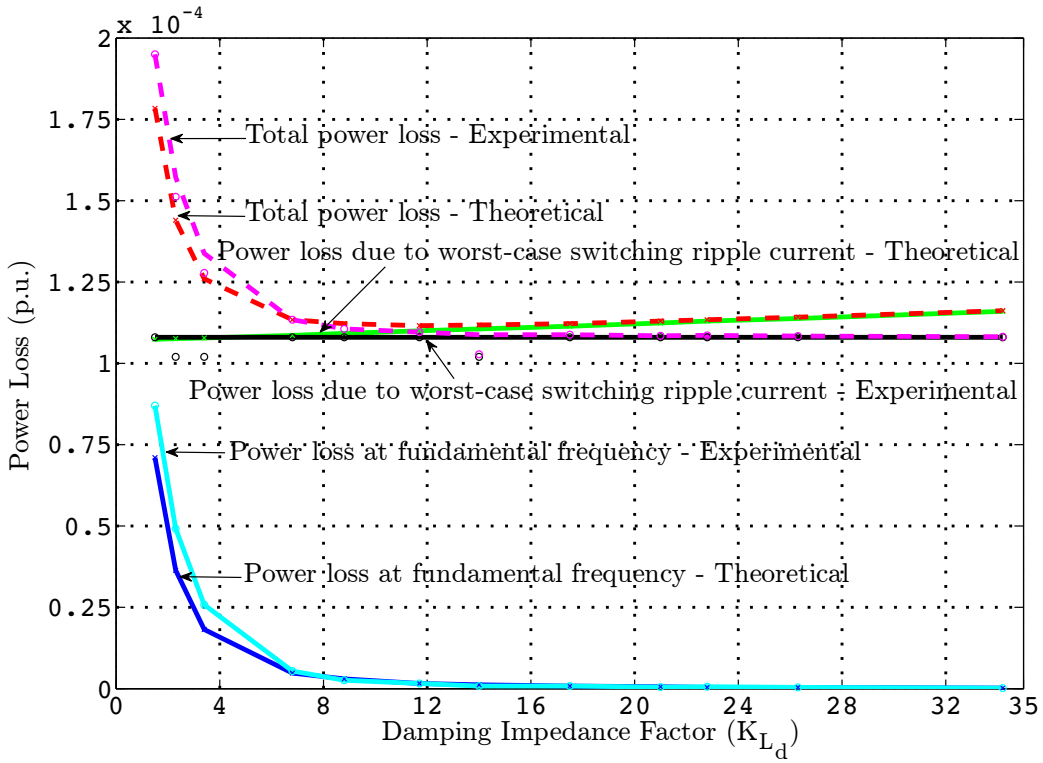


Figure 2.20: Theoretical and experimental power loss comparison as a function of the damping impedance factor K_{L_d}. Curves for the fundamental loss component, switching loss component and total loss are indicated.

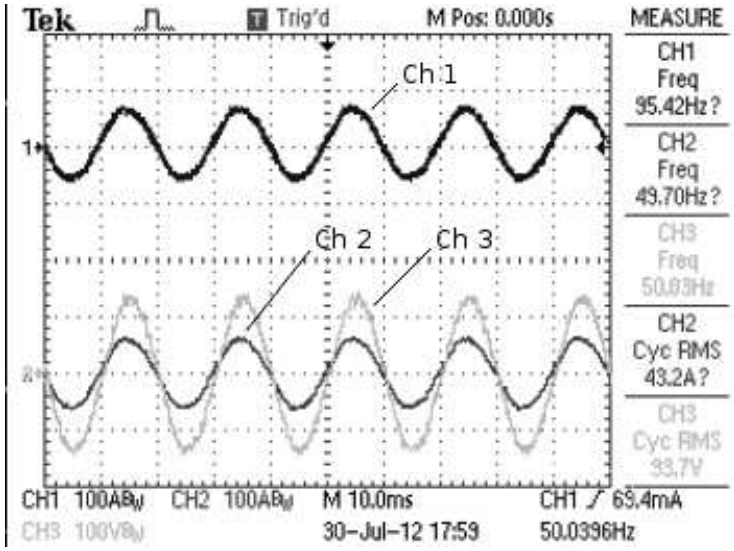


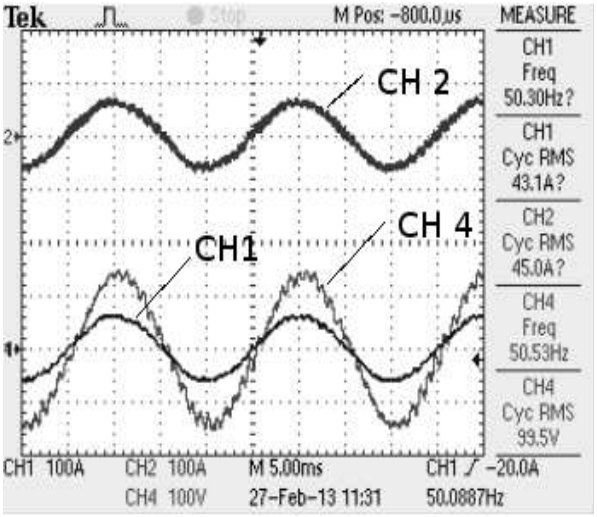
Figure 2.21: Operation of the inverter with LCL filter at an output of 100 V (rms), 40 A (rms) at unity power factor. Ch1: Inverter-side inductor current (100 A/div); Ch2: Grid-side inductor current (100 A/div); Ch3: voltage across capacitor V_c (100 V/div).

Fig. 2.20 shows the theoretical and experimental power loss curves for fundamental component, ripple component and the total power loss. The experimental power loss curves closely match the values from the theoretical analysis for both fundamental and switching frequency components. As suggested in Section 2.4.4.4, a selection of $K_{L_d} = 12.5$ based on (48) is a good choice in terms of QF and P_T as observed from Fig. 2.19 and Fig. 2.20 respectively. Further, it can be observed that both the curves being flat around the chosen value of K_{L_d}, slight variations of say 10% in the damping inductor value and hence a deviation in the K_{L_d} will not affect the expected QF and P_T. However, sensitivity to component tolerances involving all the filter components need a detailed study.

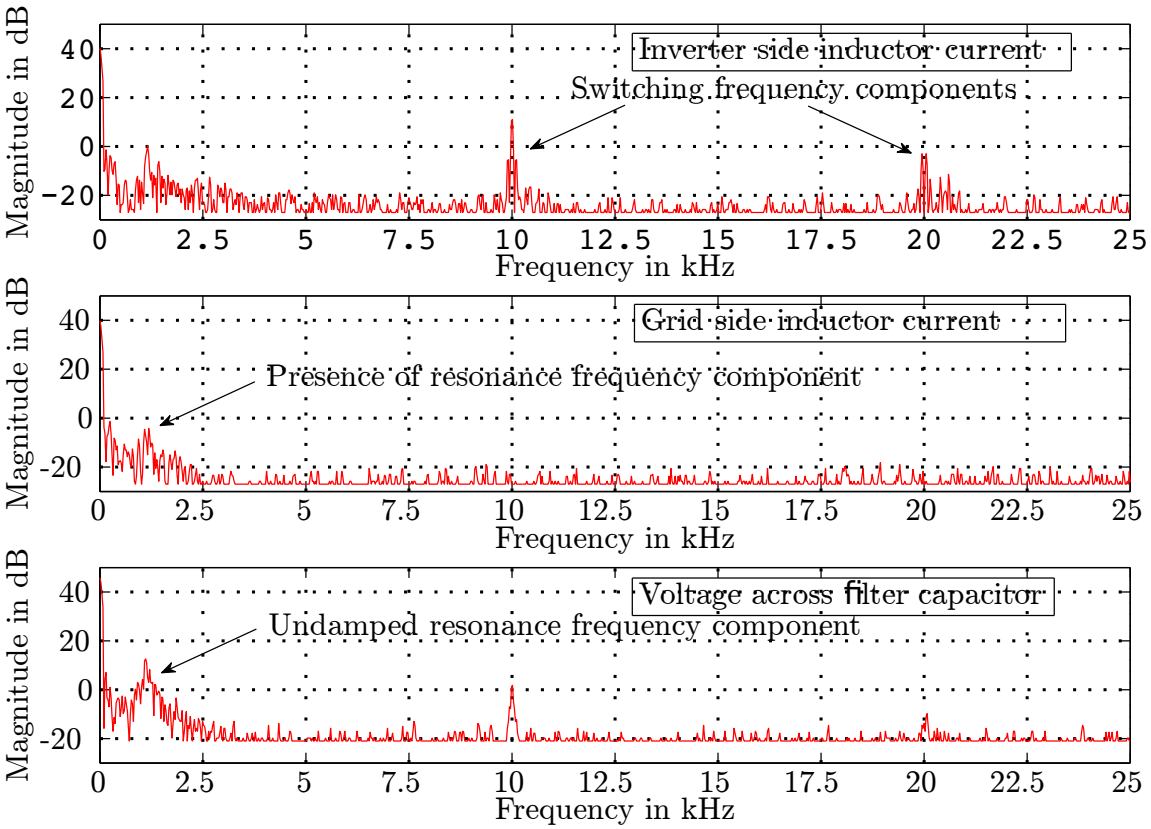
Fig. 2.21 shows the inverter-side inductor current, filtered grid-side inductor current and output filter capacitor voltage, v_C. The waveform was captured with the inverter giving a sinusoidal output of 100V rms at unity power factor and carrying a line current of 40A. The damping inductor used was $390\mu H$.

2.4.6.3 Filtering Performance

Fig. 2.22(a) and Fig. 2.23(a) show the inverter-side inductor current, filtered grid-side inductor current and output filter capacitor voltage, v_C without and with the passive damping

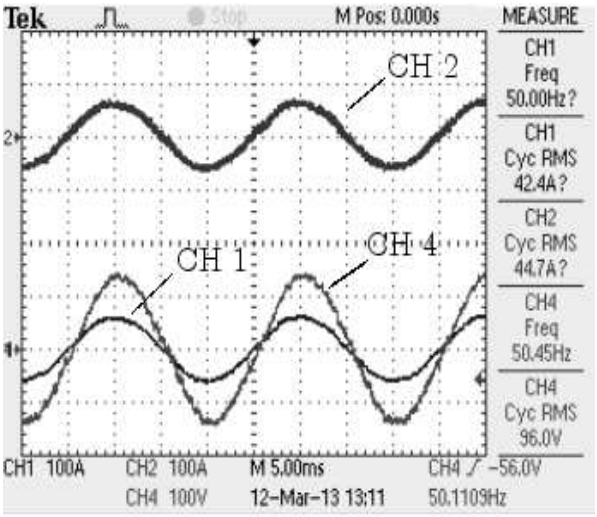


(a)

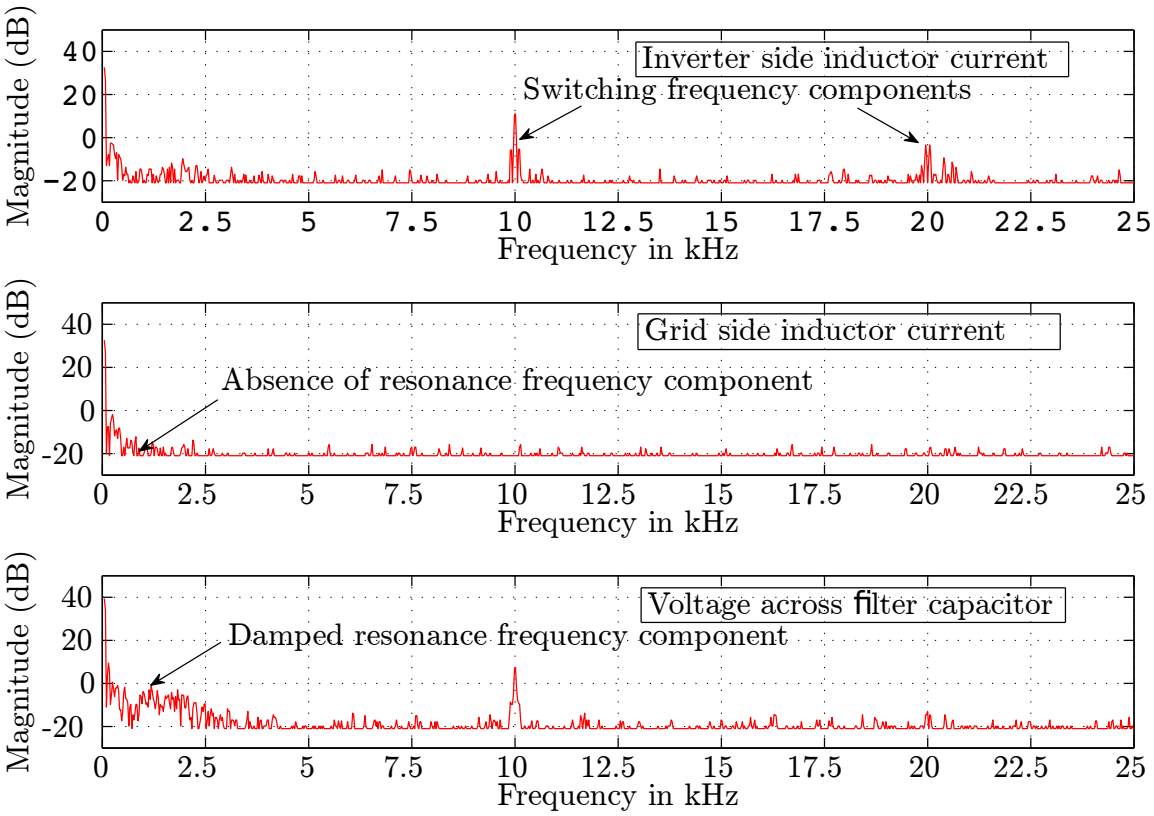


(b)

Figure 2.22: Power converter waveforms and spectrum at an output of 100 V (rms), 40 A (rms) and unity power factor at the inverter output terminal without the SC-RL passive damping circuitry. (a) Operation of the inverter with undamped LCL filter. Ch1: Grid-side inductor current (100 A/div); Ch2: Inverter-side inductor current (100 A/div); Ch4: voltage across capacitor V_c (100 V/div). (b) Spectrum of waveforms in (a).



(a)



(b)

Figure 2.23: Power converter waveforms and spectrum at an output of 100 V (rms), 40 A (rms) and unity power factor at the inverter output terminal with the SC-RL passive damping circuitry. (a) Operation of the inverter with damped LCL filter. Ch1: Grid-side inductor current (100 A/div); Ch2: Inverter-side inductor current (100 A/div); Ch4: voltage across capacitor V_c (100 V/div). (b) Spectrum of waveforms in (a).

circuitry respectively. The waveforms have been captured with the inverter giving a sinusoidal output of 100 V and unity power factor at the inverter output terminals. The line current is 40 A. In the case of damped LCL filter, the damping inductor used was 1.17 mH which gives very low QF as shown in Fig. 2.19 corresponding to $K_{L_d} = 11.7$.

Fig. 2.22(b) and Fig. 2.23(b) show the FFT spectrum of the waveforms in Fig. 2.22(a) and Fig. 2.23(a) respectively. The FFT spectrums show the filtering performance of the LCL filter and the effect of the passive damping circuitry at the resonance frequency. With damping, the grid side current ripple is 0.085 A and the inverter side current ripple is 4.01 A at the switching frequency. The corresponding filter attenuation (i_g/v_i) at the switching frequency is -64.25 dB. The experimentally obtained attenuation is close to the analytically computed attenuation of -66.8 dB. The capacitor voltage has oscillations of magnitude 2.58 V at the resonance frequency without damping. With the SC-RL damping network, the magnitude is reduced to 0.28 V. The rms switching ripple current in the damping resistor analytically obtained under the mentioned operating conditions is 0.484 A. The experimental measurement is 0.479 A which has an error of 1.03%.

2.5 Summary

A detailed study of LCL filter design with specific emphasis on passive damping network design has been presented. SC-RL passive damping is the passive damping network considered for the study. The SC-RL damped LCL filter has been modelled using state space approach. Using this model, expressions have been derived for quality factor and total power loss in the damping resistor. The expressions are used to show the lower total power loss in the damping resistors in the SC-RL damping method as compared to the purely resistive damping and SC-R damping cases. This makes the SC-RL damping a good choice of LCL filter damping method for high power inverters connected to the grid. Also, the normalised quantitative total power loss evaluated for the same level of damping is useful for the designers to make a choice on the passive damping method that can be employed.

A procedure for SC-RL damping circuit design has been proposed with the intent of keeping the QF low in the range of 2.0 to 2.5 and while maintaining the total power loss in the damping resistor to be in the range of 0.05% to 0.1%. The trade-off involved in systematically designing the passive damping circuit, with choice for C_1, C_d and R_d, is provided. A damping impedance factor, K_{L_d}, has been introduced in the process of developing the design procedure

and is used to select L_d. An expression for a suitable value of K_{L_d} is provided. This value of K_{L_d} is shown to give a low quality factor along with low losses in the damping resistors. This is verified analytically over a wide range of switching frequencies, power levels and choice of inductance and capacitance values of the filter. The outlined method is useful for high power inverters connected to the grid. Experimental measurements were made using a large number of inductors to vary K_{L_d} for practical evaluation of its impact on the filter damping performance. The filter was used in a power converter at an output of 100 Vrms, 40 Arms, 50 Hz and the filtering performance closely matched the analysis.

Chapter 3

Thermal Performance Evaluation of High Power Grid-Connected Inverters

For improved reliability, it is desirable to evaluate the thermal performance of grid-connected inverters at their rated operating conditions. It is particularly useful in the present day scenario where power levels of grid-connected inverters have increased to MW range. With this motivation, a novel test method to test high power grid-connected inverters has been developed. In an inverter, the semiconductor devices are prone to frequent failures compared to the associated passive components. So, thermal performance evaluation generally focuses on the thermal testing of the semiconductor switches [82, 92] only. In the proposed method too, the primary focus is on thermal testing of the semiconductor switches. However, the method being developed for high power inverters, the thermal response of the output filter inductors, the dc bus capacitors and the output filter capacitors also need attention. While high temperatures can lead to insulation failure in inductors, the operating life of the capacitors depend on the thermal effects of the current through them [16]. So, the usefulness of the proposed method to test the dc bus capacitors and output filter inductors and capacitors has also been studied.

This Chapter discusses the thermal test method in detail. In Section 3.1, the various inverter testing methods available in literature are explained. Section 3.2 details the proposed test method. Phasor analysis has been provided in Section 3.3 to get a better physical insight into the operation of the proposed test method. In Section 3.4, Common Mode (CM) and Differential Mode (DM) equivalent circuits are developed for the actual system and the proposed test configuration. Section 3.5 uses the equivalent circuits to design the closed loop control for the proposed test method. Section 3.6 gives the details of the hardware configuration used to validate the method experimentally. In Section 3.7, the low frequency

voltage ripple in the dc bus due to the test method is analysed. Section 3.8 and Section 3.9 provides the analysis and experimental results of the various tests for the 4-wire and 3-wire configurations respectively. Section 3.10 summarises the Chapter.

3.1 Inverter Testing Methods - A Survey

A rich literature is available on testing of inverters [73–82, 92–96]. The development of these test methods can be traced to the increasing use of UPS and chargers. Burn-in tests of UPS and chargers are run typically for 72 hours [73, 93]. The need to reduce the energy costs involved in the burn-in tests led to the development of several testing methods starting from the late 1980s.

The various methods available in literature can be classified as shown in Table. 3.1. As seen in the table, the basis for classification can be the control method, power level, topology, nature of additional hardware or the principle of operation of the test method. The remarks column in the table indicate the salient points of each classification. In this thesis, the classification based on ' the principle of operation of the test method' is used as the basis for explaining the methods available in literature since all available methods are based on one of the two principles of operation listed in the table.

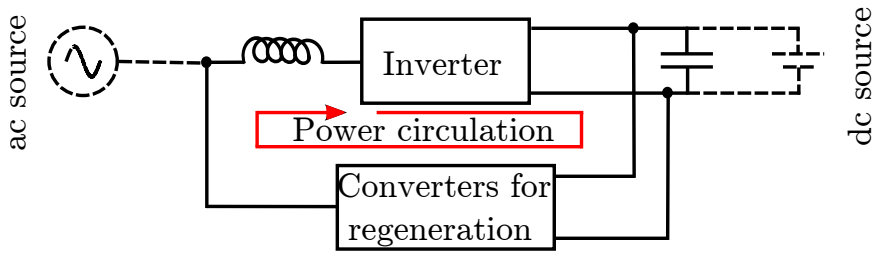
Classification	Remarks	References
Based on Control Method		
Open loop and closed loop	Open loop control is simple but cannot be automated.	Open loop – [76, 93, 94] Closed Loop – [73–75, 77–79]
Digital control and analog control	Analog control is used at low power levels while a precise digital control is suitable at high power levels.	Analog – [73, 74] Digital – [76, 77, 81, 94]
Voltage mode control and current mode control	Current mode control inherently provides over current protection.	Voltage Mode – [93] Current Mode – [75, 77–80]
Based on Power Level		
High power	Developed specifically for high power inverter testing.	[92, 95]
Continued in the next page		

Classification	Remarks	References
Based on Topology		
Single phase and three phase	Methods specific to single phase and three phase inverters.	Single-Phase – [74, 78, 93, 94] Three-Phase – [75, 77, 79, 94]
Series connected inverter and Shunt connected inverter	Series connected inverter is used in online UPS and DVR. Shunt connected inverters find application as STATCOM and Active power filters.	Series-Connected Inverter – [74, 75, 78–80, 93, 94] Shunt-Connected Inverter – [77]
Based on Nature of Additional Hardware		
Motor-Generator set	Motor acts as the load for the inverter while the generator regenerates the power back to the grid.	[95]
Passive components	The load current is regulated by adjusting the opposition voltage created by an auto-transformer. This requires manual intervention.	[93, 94]
Converters	A converter of atleast the same rating as the inverter being tested is used to regenerate the power back to the grid.	[73–80, 96]
Based on Principle of Operation of the Test Method		
Regenerative method	Regenerative principle [Section 3.1.1]	[73–80, 93–96]
Opposition method	Opposition principle [Section 3.1.2]	[81, 82]

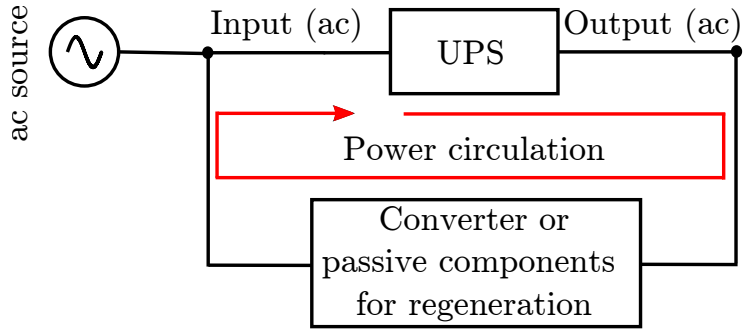
Table 3.1: Classification of testing methods available in literature.

3.1.1 Regenerative Method

In this method, an additional system of similar rating as the system under test is used to regenerate the power consumed, except for the losses which are supplied by an ac or dc source. Fig. 3.1(a) and Fig. 3.1(b) show two generic block diagrams of a regenerative set-up



(a)



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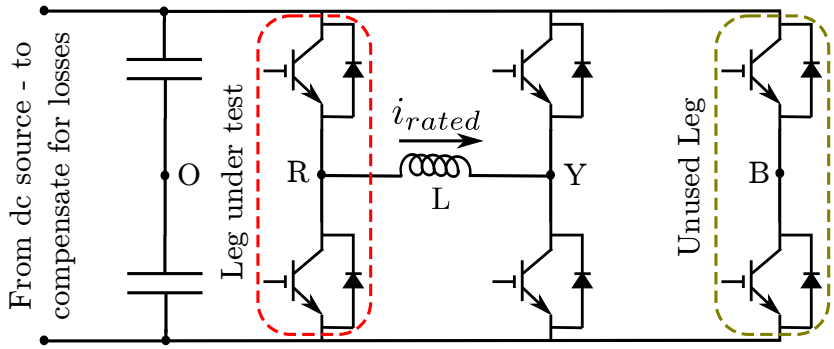


(c)

Figure 3.1: Regenerative and opposition test methods. (a) Regenerative configuration for inverter testing where either an ac source or a dc source shown in dashed lines will supply the losses in the system. (b) Regenerative configuration for UPS testing where only an ac source can be used for supplying the losses as both the input and output of the UPS are ac. (c) Opposition method for testing an inverter. The three legs of the inverter are tested one at a time.

where the power circulates within the two systems - the inverter under test and the additional hardware used to regenerate the power. References [73–80, 93–96] use the regenerative method. References [93] and [94] suggest using simple passive components for regeneration. References [73–80] all use additional converters for regeneration with differences in their topology. References [73, 74] and [76] achieve unity power factor (UPF) along with regeneration. References [95] and [96] discuss regenerative methods developed specifically for high power inverters. While [95] uses a motor-generator set to regenerate power, [96] uses two back-to-back connected inverters for regeneration.

The drawback of this method is that it requires additional systems – converters or passive components – that are rated equal or higher than the system under test.

3.1.2 Opposition Method

In this method, one leg of the inverter is tested at a time. As shown in Fig. 3.1(c) an inductive filter is connected between two legs of the inverter and the third leg is left unused. First, rated voltage is set at the output of the leg under test. Then, the voltage at the output of the other leg is adjusted to set a differential voltage that drives the rated current.

For example, let R-phase leg be the leg under test as shown in Fig. 3.1(c). Let the rated voltage and rated current at its output for a given grid power factor angle, ϕ be represented by the phasors $\overline{V}_{R,rated}$ and $\overline{I}_{R,rated}$ respectively. 'ϕ' is the angle between the voltage and current at the point of common coupling with the grid. Then, first v_R is set to $\overline{V}_{R,rated}$. So, we have – assuming rated current to flow between R and Y phases,

$$\overline{V_R} = \overline{V}_{R,rated} = \overline{V_Y} + \jmath\omega L \cdot \overline{I}_{R,rated} \tag{49}$$

where, $\overline{V_R}$, $\overline{V_Y}$ are the voltage phasors of the voltages at R and Y with respect to dc bus mid-point 'O' respectively.

From (49), to achieve rated current at the output of the R-phase leg, the Y-phase voltage has to be,

$$\overline{V_Y} = \overline{V}_{R,rated} - \jmath\omega L \cdot \overline{I}_{R,rated} \tag{50}$$

From, (49) and (50), the common mode and differential mode components of voltages can be found to be,

$$\overline{V}_{cm} = \overline{V}_{R,rated} - \frac{1}{2} \cdot \jmath\omega L \cdot \overline{I}_{R,rated} \tag{51}$$

$$\overline{V}_{R,dm} = \frac{1}{2} \cdot \jmath\omega L \cdot \overline{I}_{R,rated} \tag{52}$$

$$\overline{V}_{Y,dm} = -\frac{1}{2} \cdot \jmath\omega L \cdot \overline{I}_{R,rated} \tag{53}$$

By applying the common mode and differential mode voltages as given by (51), (52) and (53), rated voltage and rated current can be obtained at the output of the leg under test at a given grid power factor angle ϕ.

Since the load is an inductor, the power drawn from the source compensates only for the semiconductor losses and the losses in the small resistance associated with the inductor. Hence, the power drawn is minimal. References [81] and [82] use the opposition method. As one leg is not switched at all during the test, with a common cooling arrangement, the temperature rise in the heatsink over ambient will not match that of the actual system where all three legs are switching. So, this method can be used only when the three legs of the inverter have independent cooling arrangement. Apart from the regenerative and opposition methods, [92] explores the use of series-resonance principle for inverter testing.

From the above discussion, it can be seen that all regenerative methods require passive components [93, 94] or converters [73–80, 95, 96] of similar or higher rating than the inverter under test. This may suit testing of low power mass-produced inverters but can be impractical for high power converters, especially the ones that are custom built. The opposition method, also known as the two leg test [81, 82], and the series resonant approach [92] are the two available self-test methods that do not require additional systems of similar or higher power rating as the inverter under test. However, the usefulness of the opposition method and series-resonance approach are limited to systems where each leg is mounted on a separate heatsink or where the thermal cooling loop for each phase leg is independent. Also, like the regenerative methods discussed in Section 3.1.1, these have been developed only for thermal testing of the semiconductor devices. The possibility of using the methods to test the dc bus capacitors and output filter components has not been studied.

3.1.3 Focus of Work

The test method proposed in this thesis aims at addressing the issues in the methods available in literature while retaining their advantages. The focus of the work can be listed as given below:

1. To develop a test method that can evaluate the thermal performance of the semiconductor switches.

2. To ensure that the proposed method meets the following requirements:

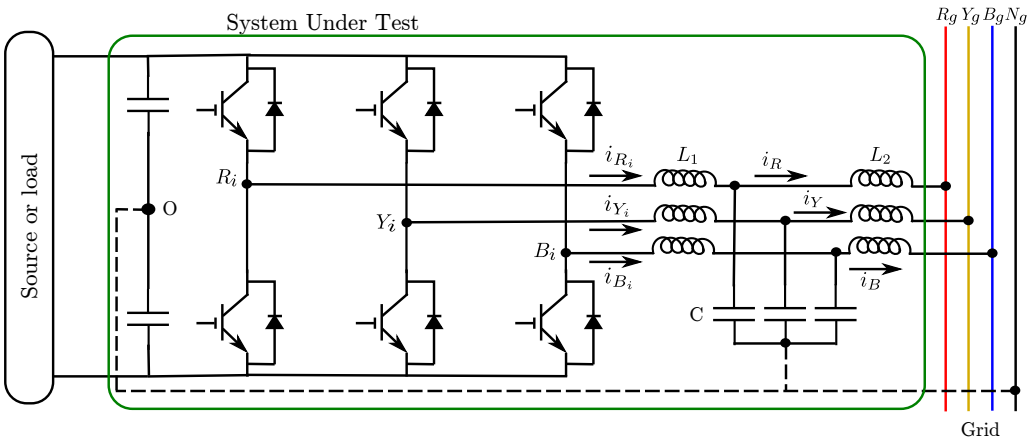
   - It does not require high power source or load. Only the losses in the system is required to be supplied during the test.
   - It does not require any additional converters or passive components of high power for power circulation.
   - It can be used in either case of the IGBT modules mounted on a common heatsink or separate individual heatsinks.
   - It can be used for testing of both three-phase 4-wire and three-phase 3-wire systems. This would make it useful for a wide variety of PWM techniques.
   - It can be used without significant changes in the hardware.

3. To study the usefulness of the proposed method to evaluate the thermal performance of the dc bus capacitors and the output filter components.

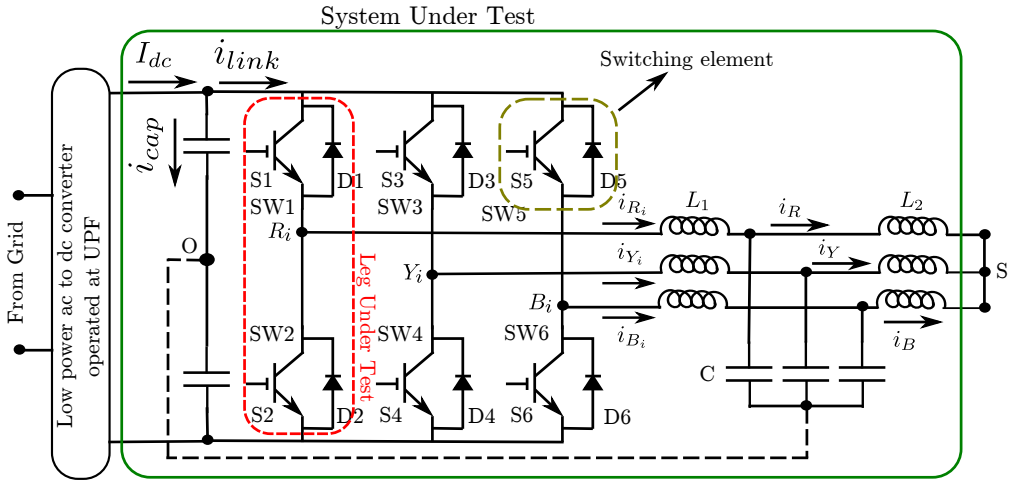
3.2 Proposed Test Method

3.2.1 Actual System and Test Configuration

Fig. 3.2(a) shows the actual system to be tested - a generic high power three-phase grid-connected inverter. An LCL filter is considered at the output as it is generally required [33,89] to meet the IEEE standards [28, 65] for grid-connection. Both 3-wire connection shown in solid lines and 4-wire connection shown in dashed lines are possible. The configuration shown represents a wide range of practical systems such as a DSTATCOM, shunt active filter, front-end converter, inverter interfacing a distributed source with the grid and the like. In case of



(a)



(b)

Figure 3.2: Actual system and test configurations. Solid lines indicate a 3-wire system and dashed lines indicate a 4-wire system. (a) Actual system consisting of a generic three-phase grid-connected inverter with output LCL filter. (b) Proposed test configuration consisting of a three-phase inverter with output LCL filter shorted. R-phase leg is considered to be the Leg Under Test (LUT). A low power ac-dc converter feeds the losses at UPF.

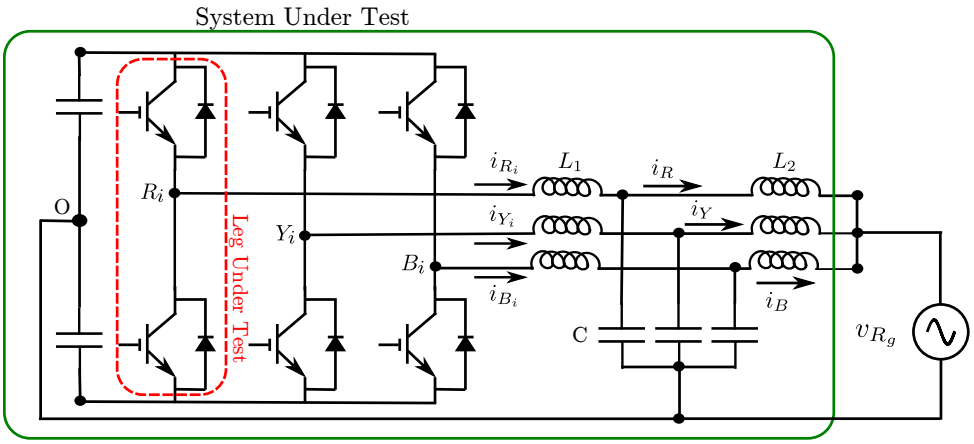


Figure 3.3: Alternative test configuration consisting of a three-phase inverter with output LCL filter synchronized to a single-phase grid. This configuration is applicable only to 4-wire systems.

a DSTATCOM and shunt active filter, neither a source nor a load would be present on the dc bus side.

Fig. 3.2(b) shows the proposed test configuration. The test configuration consists of a low power front-end converter operating at unity power factor (UPF) to power the dc bus and a high power three-phase inverter with the output LCL filter which is the system under test (SUT). As shown in the figure, one end of the 3-phase LCL filter is shorted. Only the losses in the system will be supplied by the front-end converter. Thus, the configuration does not need a high-power source and load. The proposed method in discussed in detail using a 4-wire configuration. Section 3.9 discusses the modifications required for a 3-wire configuration.

Fig. 3.3 shows an alternative test configuration which eliminates the need for the low power ac to dc converter shown in Fig. 3.2(b). As shown, the alternative configuration has the three legs of the inverter synchronized to a single phase ac grid. The grid supplies only the losses in the system. Unlike the opposition method and the series-resonance approach, this can be used for the thermal testing of the semiconductor devices even when the three legs are mounted on a common heatsink. However, this configuration can be used only for 4-wire systems. Hence, this configuration is not discussed in detail in the present work.

3.2.2 Test Method

In the proposed method, each leg of the three-phase inverter is tested one at a time. Fig. 3.4 represents the equivalent circuit of the test configuration shown in Fig. 3.2(b) under the proposed method of operation. As shown in the figure, the Leg Under Test (LUT) is operated as an open loop voltage source and the other two legs are operated in closed loop current control mode. Since the LCL filters are shorted at one end as shown in Fig. 3.2(b) and the LCL filter capacitors draw only a small amount of current at the fundamental frequency, the current through the LUT is almost the sum of the currents through the current controlled legs. Thus, by appropriate choice of open loop voltage and closed loop currents, rated terminal voltage and rated current can be set at the LUT, thus emulating that leg of the actual system. Detailed test procedures for thermal testing of semiconductor devices, dc bus capacitors and output filter components appear in Sections 3.8 and 3.9.

The alternative method shown in Fig. 3.3 also tests one leg at a time. Here, the synchronization with the single phase grid ensures rated voltage at the output of the LUT. All the three legs are current controlled to get a set of balanced rated currents. An outer dc bus voltage control loop is used to draw a small in-phase current from the single phase mains to supply the losses in the inverter.

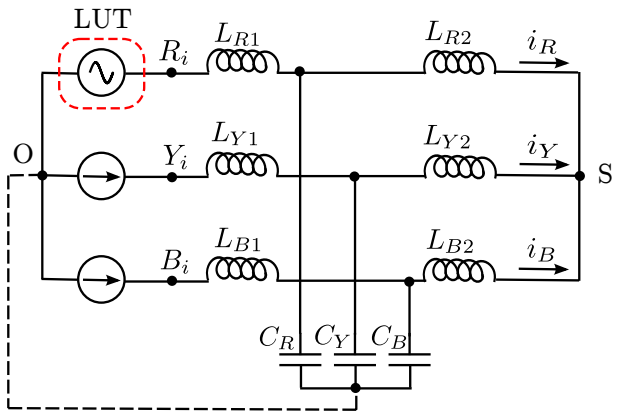


Figure 3.4: Equivalent circuit of test configuration under proposed method of operation. L_{R1}, L_{Y1} and L_{B1} represent the inverter-side output inductors of the three phases, L_{R2}, L_{Y2} and L_{B2} represent the grid-side output inductors of the three phases and C_R, C_Y and C_B represent the output filter capacitors of the three phases.

3.2.3 Choice of Current References

From Fig. 3.4,

$$i_R(t) = -(i_Y(t) + i_B(t)) \tag{54}$$

From (54), by forcing i_Y and i_B to follow appropriately set current references, i_R can be controlled to be the same as in the actual system. There are theoretically infinite possible combinations of i_Y and i_B that give the required i_R. In the proposed method, i_Y and i_B are chosen so as to form a three-phase balanced system of currents with i_R. As can be seen in Section 3.8.2, this selection of currents help in semiconductor device thermal test even when the power semiconductor devices or modules are mounted on a common heatsink. Also, from Section 3.8.3, this particular selection of current references can be seen to be useful for the testing of dc bus capacitors. It may be noted that the two-leg test [81, 82] shown in Fig. 3.1(c) is a particular case of the proposed test method with $i_B = 0$ and $i_Y = -i_R$. So, the proposed test method can be viewed as a 'generalized opposition method'.

3.3 Phasor Analysis

Let, $\mathbf{V_{R_g}}$, $\mathbf{V_{Y_g}}$, $\mathbf{V_{B_g}}$, $\mathbf{V_{R_i}}$, $\mathbf{V_{Y_i}}$, $\mathbf{V_{B_i}}$ and $\mathbf{V_S}$ represent the fundamental frequency voltage phasors at the respective nodes R_g, Y_g, B_g, R_i, Y_i, B_i and S with respect to the dc bus mid-point O in Fig. 3.2(a) and Fig. 3.2(b). Further, let $\mathbf{V_{L_R}}$, $\mathbf{V_{L_Y}}$ and $\mathbf{V_{L_B}}$ be the fundamental frequency phasors representing the phasor sum of the voltage drops across the two output filter inductors in R, Y and B phase respectively.

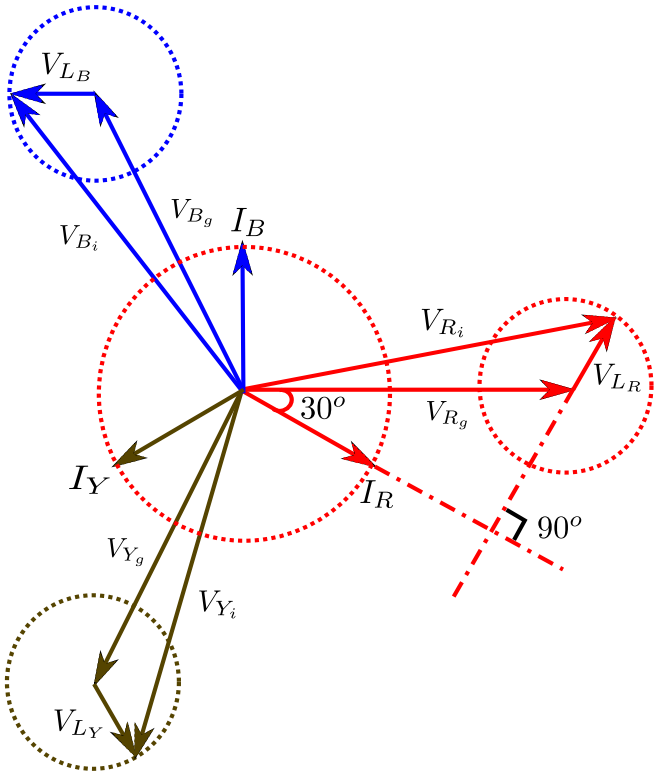
Then, from Fig. 3.2(a), we have for the actual system,

$$\mathbf{V_{R_i}} = \mathbf{V_{R_g}} + \mathbf{V_{L_R}} \tag{55}$$

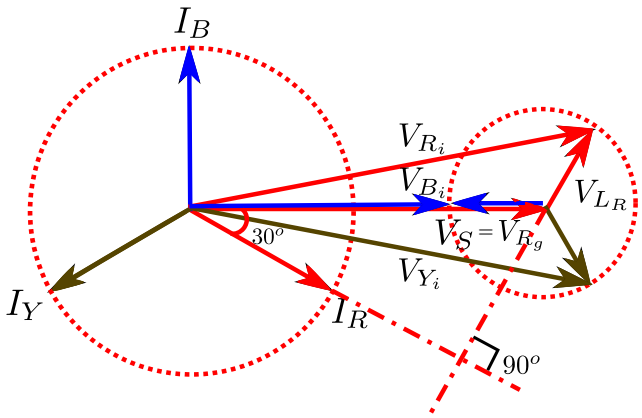
And, from Fig. 3.2(b), we have for the test configuration,

$$\mathbf{V_{R_i}} = \mathbf{V_S} + \mathbf{V_{L_R}} \tag{56}$$

Similar phasor expressions can be written for the other legs of the actual system and the test configuration. In the test configuration, to achieve the same voltage as the actual system at the inverter output terminal of the LUT, $\mathbf{V_S}$ is made equal to the grid-side voltage of the LUT in the actual system. For example, when R-phase leg is the LUT, $\mathbf{V_S}$ is set to $\mathbf{V_{R_g}}$, so



(a)



(b)

Figure 3.5: Phasor representations corresponding to the fundamental frequency when R-phase is the LUT. (a) For the actual system. (b) For the proposed test configuration. The phasor diagram has been drawn for a lagging grid power factor angle of 30^o. The small fundamental frequency current through the output filter capacitors has been neglected in drawing this phasor diagram.

that the test configuration represented by (56) is identical to the actual system represented by (55). $\mathbf{V_S} = \mathbf{V_{R_g}}$ is a common mode voltage.

Fig. 3.5 shows the fundamental frequency phasor representation of the actual system and the test configuration. Vectors corresponding to $\mathbf{V_{L_R}}$, $\mathbf{V_{L_Y}}$ and $\mathbf{V_{L_B}}$ have been shown greater in magnitude than they actually are, for the sake of clarity of the diagrams. Their magnitudes are typically around 10% of the grid voltage magnitude at the rated current [33, 89]. The fundamental frequency component of current through the output LCL filter capacitors is small and has not been included in these phasor diagrams. Fig. 3.5 is used to get better physical understanding of the actual and test circuits. It may be noted that the fundamental frequency current through the output filter capacitors depend on the nominal fundamental frequency grid voltage and the LCL filter capacitance. It does not depend directly on the power level. The only influence of power level comes through the chosen value of capacitance as the capacitor value varies with the power level. For, the range of switching frequencies and resonant frequencies considered in this thesis, the fundamental frequency component of current is usually negligible. Also, though it has been neglected in the phasor analysis, it has been included in the experiments by computing the current through the capacitor at fundamental frequency and adding the same vectorially with the set reference current for more accuracy.

In Fig. 3.5, the phasor diagrams have been drawn for a lagging grid power factor angle of 30^o when R-phase is the LUT. As the grid current phase angle varies, the three-phase grid currents trace the circumference of the bigger circle and the inverter terminal voltages trace the circumference of the smaller circles in the figure.

3.3.1 Operation of the Actual System and Test Configuration – A Physical Insight

In the actual system, the three-phase grid voltages ($v_{R_g}, v_{Y_g}, v_{B_g}$) appear on the grid side of the LCL filters. The grid can be balanced by maintaining the same voltage as the grid voltages on the inverter side of the LCL filters. Ideally, zero fundamental frequency current flows from the inverter into the grid under this balanced condition. Now, rated three-phase balanced currents can be made to flow from the inverter to the grid by adding a set of balanced three-phase voltages of small magnitude to the inverter side. The three-phase balanced voltages to be added correspond to the voltage drop in the filter inductors

$(v_{L_R}, v_{L_Y}, v_{L_B})$ at the rated current. This can be observed from Fig. 3.5(a).

In the test configuration, to achieve the same voltage as the actual system in the LUT, a common mode voltage corresponding to the grid voltage at the LUT in the actual system is maintained at the output of all three legs of the inverter. For example, when R phase leg is the LUT, v_{R_g} is produced at the output of all the three legs of the inverter as common mode voltage. This ideally leads to zero fundamental frequency current in the shorted inductors as voltage at the output of the three legs balance each other. Now, rated currents can be made to flow in the shorted inductors by adding a set of balanced three-phase voltages of small magnitude to the common mode voltage at the inverter outputs. The three-phase balanced voltages to be added corresponds to the voltage drop in the filter inductors $(v_{L_R}, v_{L_Y}, v_{L_B})$ at the rated current. This can be observed from Fig. 3.5(b).

The common mode and differential mode analysis gives an intuitive understanding of the actual system and test configuration. So, the common mode and differential mode equivalent circuits have been developed in the next Section and used in the rest of the analysis.

3.4 Common Mode and Differential Mode Equivalent Circuits

In Fig. 3.5(a), the inverter terminal voltages are balanced. So, the fundamental frequency common mode voltage at the inverter output terminals is zero. The fundamental frequency voltage is completely a differential mode component only. However, high frequency common mode voltages at switching frequency, their multiples and sidebands can be present depending on the PWM switching method used [97]. Differential mode voltages are also present at these frequencies. In Fig. 3.5(b), $\mathbf{V_S}$ is a fundamental frequency common mode voltage. A fundamental frequency differential mode component is also present at the inverter terminals and helps drive a balanced system of currents suggested in Section 3.2.3. As in the actual system, at high frequencies both common mode and differential mode voltages can be present depending on the PWM switching method used.

In general, besides the reference low frequency (LF) fundamental voltage, PWM inverter output contains high frequency (HF) ripple voltages at the switching frequency, their multiples and side-bands. At every frequency, the voltage can further have common mode (CM) and differential mode (DM) components. Combining the two different classifications of voltage components, there can be low frequency common mode (LFCM), low frequency differen-

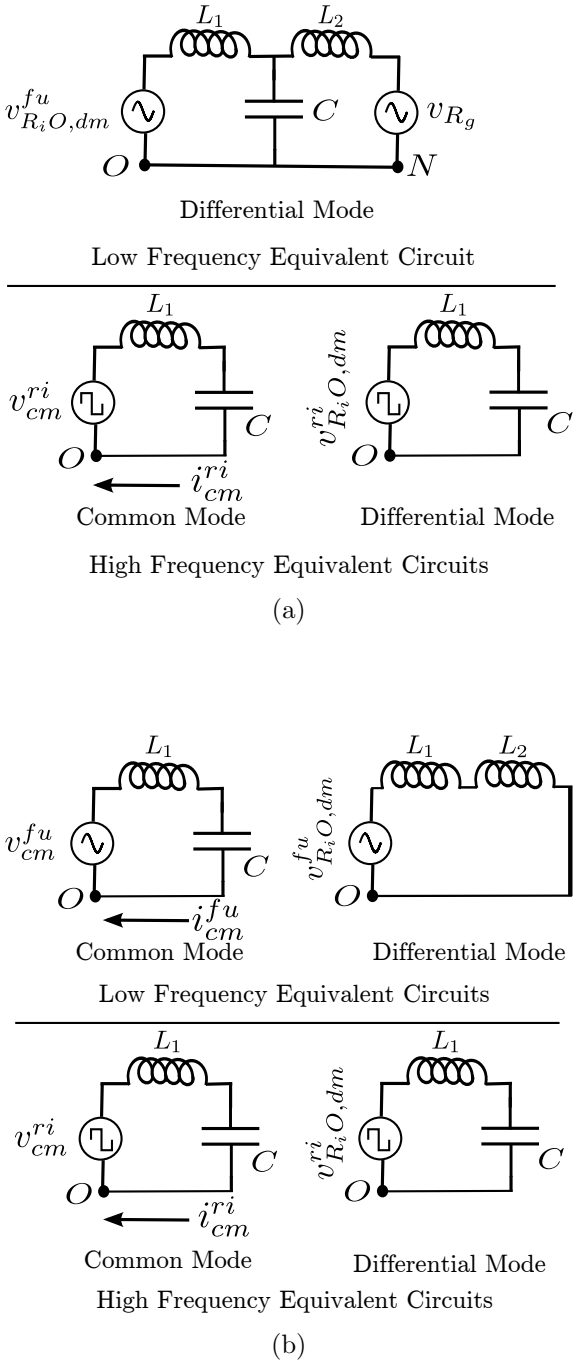


Figure 3.6: Per-phase common mode and differential mode equivalent circuits of the inverter output filter for a three-phase 4-wire configuration. (a) For the actual system. (b) For the proposed test configuration. R-phase has been used as a representative phase. The circuits are applicable for the other phases also.

tial mode (LFDM), high frequency common mode (HFCM) and high frequency differential mode (HFDM) components at the output of an inverter.

Based on the predominant current flow paths of these components, simple equivalent circuits can be drawn as shown in Fig. 3.6(a) and Fig. 3.6(b) for the output LCL filter of the actual system and the test configuration respectively. The circuits have been shown on an equivalent per-phase basis. Section 3.4.1 gives the definition of CM and DM voltages and currents. The circuits can be arrived at using the simplifying assumptions given in Section 3.4.2 and Section 3.4.3.

In the following Sections, the CM and DM equivalent circuits are used to derive the control block diagram in Section 3.5, to analyse the low frequency voltage ripple in the dc bus capacitor due to the proposed test method in Section 3.7 and to analyse the ripple current in the output filter components in Section 3.8.4.

3.4.1 Common Mode and Differential Mode Voltages and Currents - Defined

In Fig. 3.2, the common mode voltage (v_{cm}) is defined as,

$$v_{cm}(t) \triangleq \frac{v_{R_iO}(t) + v_{Y_iO}(t) + v_{B_iO}(t)}{3} \tag{57}$$

The differential mode voltage at R-phase output ($v_{R_iO,dm}$) is defined as,

$$v_{R_iO,dm}(t) \triangleq v_{R_iO}(t) - v_{cm}(t) \tag{58}$$

Similar expressions can be written for Y and B phases.

The common mode current (i_{cm}) at the inverter output terminals is defined as,

$$i_{cm}(t) \triangleq \frac{i_{R_i}(t) + i_{Y_i}(t) + i_{B_i}(t)}{3} \tag{59}$$

The differential mode current at the output terminal of R-phase ($i_{R_i,dm}$) is defined as,

$$i_{R_i,dm}(t) \triangleq i_{R_i}(t) - i_{cm}(t) \tag{60}$$

Similar expressions can be written for Y and B phases.

3.4.2 Equivalent Circuits of the Actual System

Fig. 3.6(a) shows the equivalent circuits for the actual system.

3.4.2.1 For Low Fundamental Frequency Component

The fundamental frequency CM component being zero, the CM equivalent circuit has not been shown.

The DM component of fundamental frequency voltage at the inverter output terminal balances the grid voltage and the filter drop. So, the DM equivalent circuit has the LCL filter with the inverter voltage and the grid voltage applied one on each side.

3.4.2.2 For High Frequency Switching Ripple Components

At frequencies other than the fundamental, the grid is ideally a short. Assuming a switching frequency of 2 kHz or above, the IEEE recommendations [28, 65] require the ripple current at each of the frequencies – the switching frequency, its multiples and their side-bands – to be less than 0.3% of the rated current of the inverter. So, for both CM and DM, current through the inductor L_2 can be neglected and hence we have only L_1 and C connected in series.

3.4.3 Equivalent Circuits of the Proposed Test Configuration

Fig. 3.6(b) shows the equivalent circuits for the test configuration.

3.4.3.1 For Low Fundamental Frequency Component

The common mode components do not have a closed path to flow through L_2. So, L_2 appears as open in the common mode circuit.

As explained in Section 3.3, the test configuration has mainly a common mode voltage at the fundamental frequency. The DM component of voltage is around 10% of the CM component at the rated current. Further, the impedance of the LCL filter capacitor is high at the fundamental frequency. So, the DM current through the LCL filter capacitor is negligible and the capacitor can be assumed to be open for the DM. However, unlike CM, DM currents can flow through L_2. Hence, L_2 cannot be neglected.

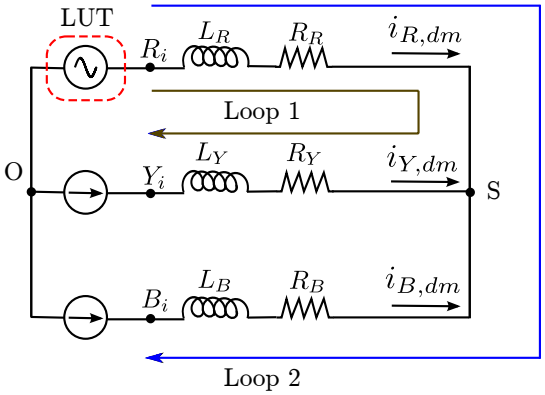


Figure 3.7: Differential mode equivalent circuit for controller design of test configuration. $L_R = L_{R1} + L_{R2}$; $L_Y = L_{Y1} + L_{Y2}$; $L_B = L_{B1} + L_{B2}$. R_R, R_Y, R_B are the resistances associated with L_R, L_Y and L_B respectively.

3.4.3.2 For High Frequency Switching Ripple Components

From Fig. 3.2(b), L_2 is open for CM. Assuming a switching frequency of greater than 2 kHz, the IEEE recommendations [28, 65] require the ripple current through L_2 at each individual frequency – the switching frequency, its multiples and their side-bands – to be less than 0.3% of the rated current of the inverter and hence the HFDM current through L_2 can be neglected. So, for both CM and DM, L_2 appears to be open and hence we have only L_1 and C connected in series as shown in Fig. 3.6(b).

3.5 Current Control for the Proposed Test Configuration

Two legs of the inverter are current controlled in the proposed test configuration. The current control block diagram is developed in this Section. A CM voltage equal to the grid voltage of the LUT in the actual system is added to each of the inverter output terminals. The balanced three-phase currents through the shorted inductors in the test configuration are due to the DM voltages superimposed on this CM voltage. The CM voltage is given as feed-forward in the control and the controller outputs are only the DM voltage references. So, the LFDM equivalent circuit is used in the design of the controller. Using Fig. 3.4 and

Fig. 3.6(b) the DM equivalent circuit for current control is shown in Fig. 3.7.

By Kirchhoff's Current Law (KCL), $i_{R,dm} = -(i_{Y,dm} + i_{B,dm})$. So, by applying Kirchhoff's voltage law (KVL) around loop 1 and loop 2 shown in Fig. 3.7 and using the subscripts *'cm'* and *'dm'* to represent the common mode and differential mode components respectively of currents and voltages, we have the following system of equations:

$$\begin{aligned}\begin{bmatrix} v_{Y_iO,dm} \\ v_{B_iO,dm} \end{bmatrix} &= \begin{bmatrix} (R_R + R_Y) & R_R \\ R_R & (R_R + R_B) \end{bmatrix} \begin{bmatrix} i_{Y,dm} \\ i_{B,dm} \end{bmatrix} \\ &+ \begin{bmatrix} (L_R + L_Y) & L_R \\ L_R & (L_R + L_B) \end{bmatrix} \begin{bmatrix} di_{Y,dm}/dt \\ di_{B,dm}/dt \end{bmatrix} \\ &+ \begin{bmatrix} v_{R_iO,dm} \\ v_{R_iO,dm} \end{bmatrix} \end{aligned} \tag{61}$$

where, R_R, R_Y and R_B are the resistances associated with the inductors and $L_R = L_{R1} + L_{R2}$, $L_Y = L_{Y1} + L_{Y2}$, $L_B = L_{B1} + L_{B2}$.

The above equations represent a multiple input $(i_{Y,dm}, i_{B,dm}, v_{R_iO,dm})$ multiple output $(v_{Y_iO,dm}, v_{B_iO,dm})$ system. The following substitution is used to convert the system into two independent decoupled systems.

$$\begin{aligned}\begin{bmatrix} v'_Y \\ v'_B \end{bmatrix} &= \begin{bmatrix} v_{Y_iO,dm} \\ v_{B_iO,dm} \end{bmatrix} - \begin{bmatrix} R_R & R_R \\ R_R & R_R \end{bmatrix} \begin{bmatrix} i_{Y,dm} \\ i_{B,dm} \end{bmatrix} \\ &- \begin{bmatrix} L_R & L_R \\ L_R & L_R \end{bmatrix} \begin{bmatrix} di_{Y,dm}/dt \\ di_{B,dm}/dt \end{bmatrix} \\ &- \begin{bmatrix} v_{R_iO,dm} \\ v_{R_iO,dm} \end{bmatrix} \end{aligned} \tag{62}$$

Using (61), (62) and assuming an equal inductance (L) and associated resistance (R) in each of the phases, we have,

$$\begin{bmatrix} v'_Y \\ v'_B \end{bmatrix} = \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} i_{Y,dm} \\ i_{B,dm} \end{bmatrix} + \begin{bmatrix} L & 0 \\ 0 & L \end{bmatrix} \begin{bmatrix} di_{Y,dm}/dt \\ di_{B,dm}/dt \end{bmatrix} \tag{63}$$

The requirement is to regulate the currents $i_{Y,dm}$ and $i_{B,dm}$. The control is similar to the current control of a RL circuit. Fig. 3.8 shows the control block diagram. The block diagram

has been shown for Y leg. The same is applicable to B leg also. A proportional resonant (PR) controller has been used. In Fig. 3.8, $i^*_{Y,dm}$ represents the set reference current. K_p and K_r are the PR controller constants. $\omega_r = 2 \cdot \pi \cdot 50\ rad/s$. References [98–100] discuss in detail the selection of controller constants for the PR controller and the digital implementation of the same.

From (62) and (63), assuming an equal inductance (L) and associated resistance (R) in all the phases, the differential mode component of the voltage references $v_{Y_iO,dm}$ and $v_{B_iO,dm}$ for the current controlled legs are given by,

$$v_{Y_iO,dm} = 2 \cdot v'_Y + v'_B + v_{R_iO,dm} \tag{64}$$

$$v_{B_iO,dm} = 2 \cdot v'_B + v'_Y + v_{R_iO,dm} \tag{65}$$

The actual voltage references for the current controlled legs including the common mode voltage component are given by,

$$v_{Y_iO} = v_{Y_iO,dm} + v_{cm} \tag{66}$$

$$v_{B_iO} = v_{B_iO,dm} + v_{cm} \tag{67}$$

Considering the R-phase leg as the LUT, $v_{cm} = v_{R_g}$. The complete control block diagram is shown in Fig. 3.9.

3.6 Base Values, System Parameters and Control Parameters

Analysis and experimental validation of the proposed method was carried out on an inverter at a rating of 24 kVA. A single-phase front-end converter was used to charge the dc bus. Both the front-end converter and the inverter were controlled using a single TMS320F2812 DSP board. Sine-triangle modulation was used for the case of three-phase 4-wire system and conventional space vector PWM (CSVPWM) was used for the case of three-phase 3-wire system. The dc bus voltage was set to 800 V in case of sine-triangle PWM and was lowered to 700 V in case of CSVPWM to have similar modulation indices in both the cases. Passive damping was used to suppress resonance in the output LCL filter. The base values

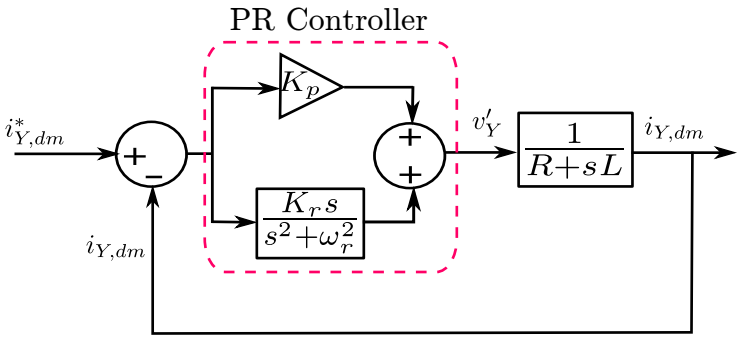


Figure 3.8: Block diagram for current control shown for Y phase. The current control is implemented for two phases of the inverter.

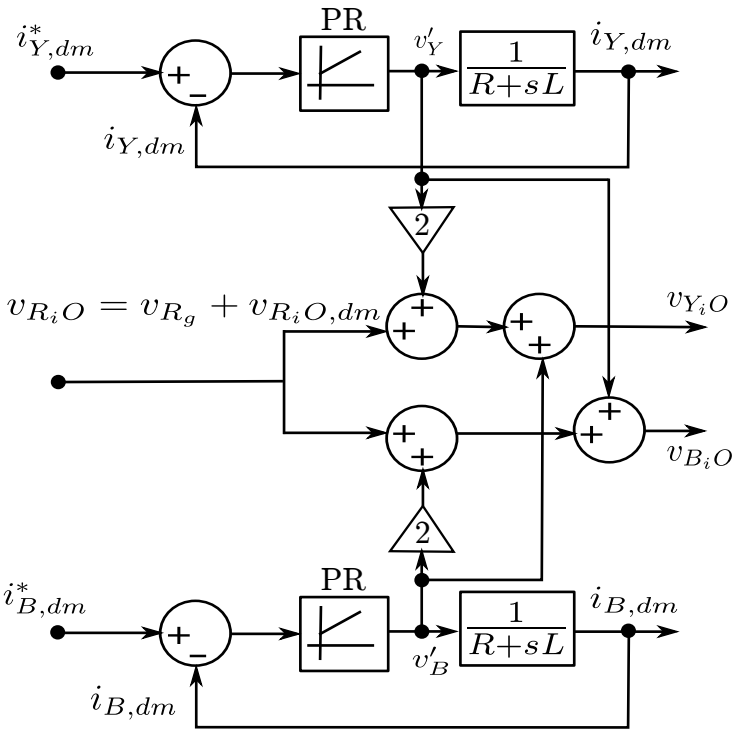


Figure 3.9: Complete control block diagram for the test configuration. R-phase is assumed to be the LUT. v_{R_iO} is an open loop voltage. v_{R_iO} is set to be the same as the voltage at the R-phase output terminal of the inverter in the actual system.

have been listed in Table. 3.2 and the various parameters of the experimental set-up have been listed in Table. 3.3. Table. 3.4 lists the proportional-resonant (PR) current controller parameters used in the experiments.

From the values in the table, at switching frequency, the impedance of L_1 is 6.9 p.u. and that of C is 0.053 p.u. So, the capacitor C can be assumed to be shorted in the HFCM and HFDM equivalent circuits shown in Fig. 3.6. Also, at the fundamental frequency, the impedance of L_1 is 0.035 p.u. and that of C is 10.6 p.u. So, the inductor L_1 can be assumed to be shorted in the LFCM equivalent circuit shown in Fig. 3.6(b).

3.7 Analysis of Low Frequency Voltage Ripple in DC Bus Capacitor

In the actual system, ideally there is zero low frequency ripple current in the dc bus capacitors. The lowest frequency component present in the dc bus current is around the switching frequency. However, in the test configuration a small low frequency ripple at twice the fundamental frequency is present in the dc bus current. This is reflected in the dc bus voltage also. In this section, analysis has been provided to show that the ripple in voltage due to this component is negligible.

Quantity	**Notation**	**Base Value**
Power	P_{base}	24 kVA
Voltage	V_{base}	200 V
Current	I_{base}	40 A
Impedance	Z_{base}	5 Ω
Frequency	ω_{base}	$2.\pi.50\ rad/s$
Inductance	$L_{base} = Z_{base}/\omega_{base}$	15.92 mH
Capacitance	$C_{base} = 1/(Z_{base}.\omega_{base})$	636.62 μF

Table 3.2: Base Values

Quantity	**Notation**	**Value**	**Per Unit**
Inverter 3-phase power	P_{rated}	24 kVA	1.0
Fundamental frequency	f_{fu}	50 Hz	1.0
Switching frequency	f_{sw}	10 kHz	200
DC bus voltage (Sine-triangle)	V_{dc}	800 V	4.0
DC bus voltage (CSVPWM)	V_{dc}	700 V	3.5
Grid phase voltage	V_g	200 V	1.0
Rated line current	I_{rated}	40 A	1.0
DC bus capacitance	C_{DC}	9400 μF	14.77
Inverter-side inductor	L_1	550 μH	0.035
Grid-side inductor	L_2	550 μH	0.035
Filter capacitance	C_1	30 μF	0.047
Damping branch capacitance	C_d	30 μF	0.047
Total filter capacitance	$C = C_1 + C_d$	60 μF	0.094
Damping inductance	L_d	390 μH	0.025
Damping resistance	R_d	3 Ω	0.6

Table 3.3: System Parameters

Control Parameter	Value
K_p	1.42 Ω
K_r	138.39 $V/A-s$

Table 3.4: Current Controller Parameters

3.7.1 Low Frequency Ripple due to Output Fundamental CM Component

Using the LFCM equivalent circuit shown in Fig. 3.6(b) and shorting the inductor L_1 as suggested in the previous Section, the LFCM circuit reduces to a voltage applied to a simple capacitor. The grid voltage is the CM voltage in the test configuration as shown in Fig. 3.5(b).

Considering R-phase to be the LUT, let the grid voltage and hence the CM voltage $v_{cm}(t)$ at the output of the test configuration be given by,

$$v_{cm}(t) = v_{R_g}(t) = V_m sin(\omega t) \tag{68}$$

where, $V_m = V_g\sqrt{2}$ and $\omega = 2 \cdot \pi \cdot f_{fu}$. At steady state, the current $i_{cm}(t)$ due to this CM voltage is,

$$i_{cm}(t) = V_m \cdot \omega C \cdot sin(\omega t + 90^o) \tag{69}$$

So, the total instantaneous ac side power due to the CM voltage and current in the three phases is,

$$p_{cm}(t) = -\frac{3}{2} \cdot V_m^2 \cdot \omega C \cdot cos(2\omega t + 90^o) \tag{70}$$

By equating the above to the input side power, the input side low frequency current ripple and the corresponding input side low frequency voltage ripple can be computed. The peak-to-peak low frequency voltage ripple $V_{ripple,pk-pk}$ in the dc bus can be derived to be,

$$V_{ripple,pk-pk} = \frac{3 \cdot V_g^2 \cdot C}{V_{dc} \cdot C_{DC}} \tag{71}$$

Using values in Table. 3.3, $V_{ripple,pk-pk} = 0.957$V or 0.0048p.u. which is negligible.

3.7.2 Low Frequency Ripple due to Output Fundamental DM Component

Let the fundamental frequency component of currents at the output be given by,

$$i_R(t) = I_m sin(\omega t - \phi) \tag{72}$$

$$i_Y(t) = I_m sin(\omega t - \phi - 120^o) \tag{73}$$

$$i_B(t) = I_m sin(\omega t - \phi + 120^o) \tag{74}$$

where, $I_m = I_{rated}\sqrt{2}$, $\omega = 2 \cdot \pi \cdot f_{fu}$ and ϕ is the phase angle measured with respect to the R-phase grid voltage.

Using the LFCM equivalent circuit shown in Fig. 3.6(b), at steady state, the fundamental frequency voltages across the output filter inductors are given by,

$$v_{L_R}(t) = \omega(L_{R1} + L_{R2}) \cdot I_m sin(\omega t - \phi + 90^o) \tag{75}$$

$$v_{L_Y}(t) = \omega(L_{Y1} + L_{Y2}) \cdot I_m sin(\omega t - \phi - 120^o + 90^o) \tag{76}$$

$$v_{L_B}(t) = \omega(L_{B1} + L_{B2}) \cdot I_m sin(\omega t - \phi + 120^o + 90^o) \tag{77}$$

So, the total instantaneous ac side power due to the DM voltage and current in the three phases is,

$$p_{dm}(t) = v_{L_R}(t) \cdot i_R(t) + v_{L_Y}(t) \cdot i_Y(t) + v_{L_B}(t) \cdot i_B(t) \tag{78}$$

(78) on simplification shows the total instantaneous power due to the DM components of voltage and current at the inverter output to be zero. Hence, the low frequency dc bus voltage ripple due to DM component is zero. This indicates that ideally power circulates among the three phases and only the losses are drawn from the dc side in case of the DM component.

From Section 3.7.1 and Section 3.7.2, it can be concluded that only the CM component of currents at the output lead to low frequency ripple in the dc bus and the magnitude of the ripple is negligible.

3.8 Analysis and Experimental Results – 4-Wire Configuration

3.8.1 Current Control

Fig. 3.10 shows the three phase currents i_R, i_Y, i_B and the voltage v_C across the R-phase LCL filter capacitor while emulating a grid-connected inverter that injects a 90^o lagging current, an in-phase current, a 90^o leading current and an 180^o out-of-phase current at the point of common coupling with the grid using the control method discussed in Section 3.5. The experimental parameters are as shown in Table. 3.3.

3.8.2 Thermal Testing of Semiconductor Devices

The thermal testing of semiconductor devices aims at subjecting the individual semiconductor devices to similar junction thermal stress as the actual system operating at the rated conditions. Usually the device junction is not accessible for temperature measurement. So, the junction temperature is estimated from the heatsink temperature using simple steady-state thermal models [101]. In some IGBT modules, the case temperature can be measured using in-built temperature sensors [101]. In such cases, the case temperature can be used for more accurate estimation of the junction temperature. In this thesis, the heatsink temperature is used. Fig. 3.11 shows the thermal model of the system under test (SUT) shown in Fig. 3.2. From Fig. 3.11, it can be observed that, to have the same junction temperature as the actual system in the test configuration, it is required that,

- The heatsink temperature in the test configuration is the same as that of the actual system operating at the rated conditions.
- The power loss in the individual semiconductor device being tested is the same as the actual system operating at the rated conditions.

Further, it must be ensured that the power loss in the semiconductor devices other than the device being tested do not exceed the maximum loss for that device in the actual system.

Section 3.8.2.1 and Section 3.8.2.2 analyses the heatsink temperature and the power loss in individual semiconductor devices in the actual system and the test configuration.

3.8.2.1 Heatsink Temperature

The heatsink temperature can be analytically estimated from the total losses generated by the semiconductor devices mounted on the heatsink using the thermal resistance of the heatsink. In the experimental set-up, three SKM150GB12T4G [102] IGBT modules - one for each leg of the three-phase inverter - are used. All the modules are mounted on a

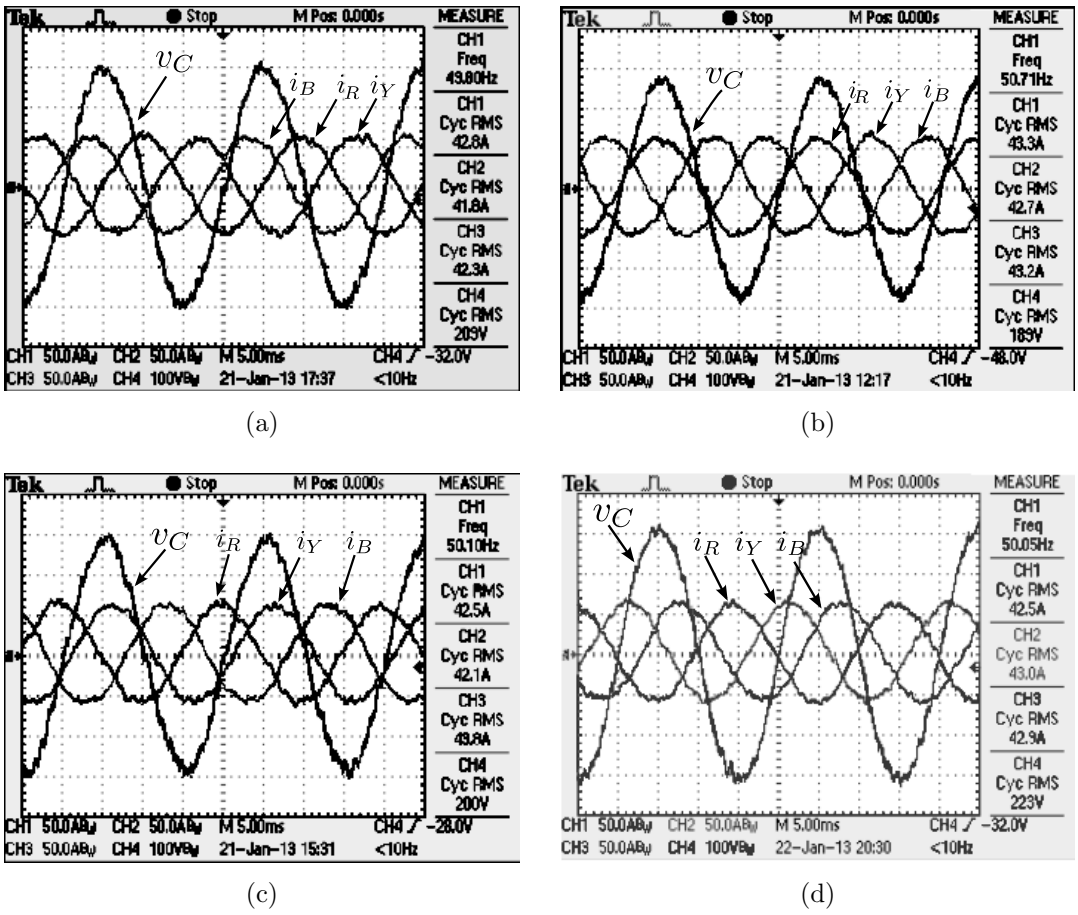


Figure 3.10: Three phase currents CH1: i_R, CH2: i_Y, CH3: i_B and R-phase LCL filter capacitor voltage CH4: v_C in the test configuration while emulating a grid-connected inverter that injects (a) a 90^o lagging current (b) an in-phase current (c) a 90^o leading current (d) an 180^o out-of-phase current at the point of common coupling with the grid. Experimental parameters are as shown in Table. 3.3. CH1, CH2, CH3: 50A/div; CH4: 100V/div.

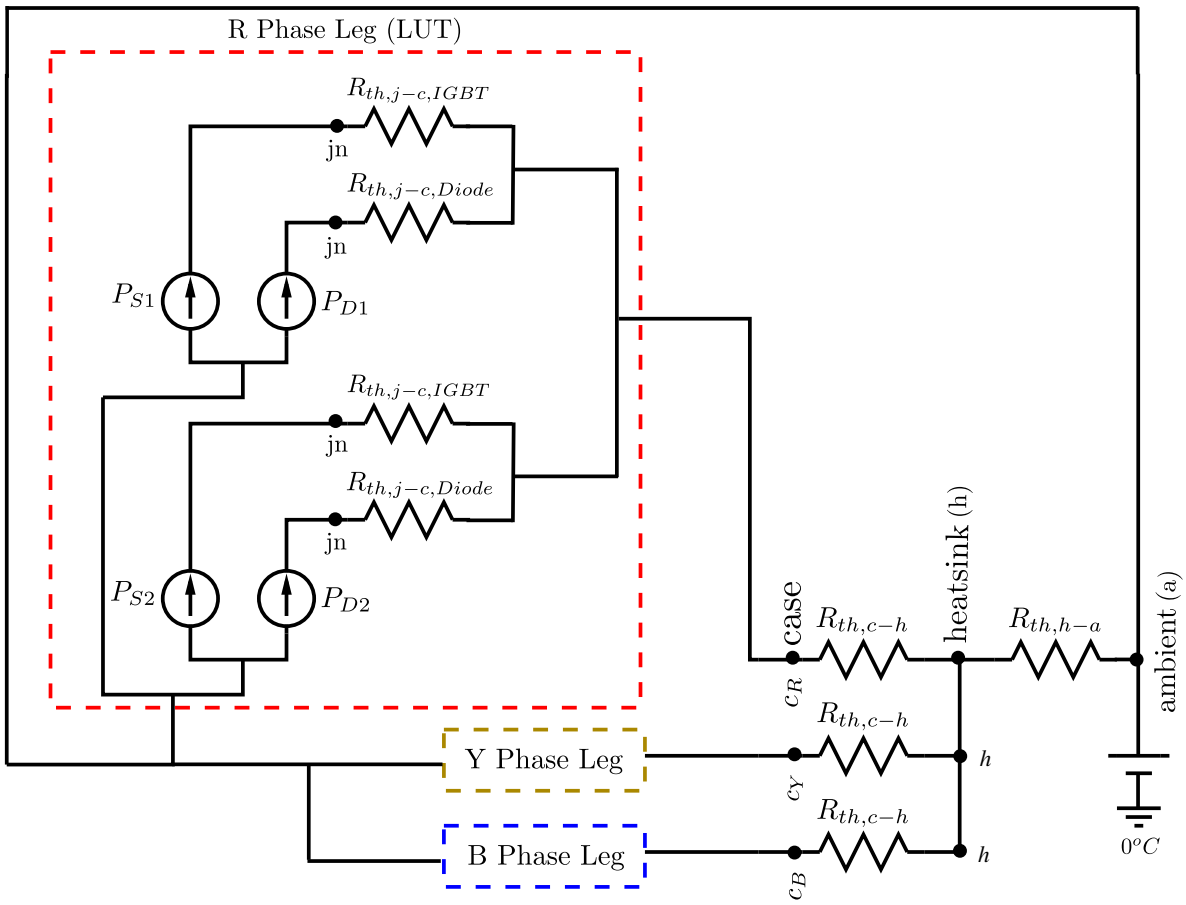


Figure 3.11: Thermal model of the three-phase inverter shown in Fig. 3.2. The detailed model of one leg is shown. The blocks 'Y Phase Leg' and 'B Phase Leg' also have the same thermal model as the R-phase leg. $R_{th,h-a}$, $R_{th,c-h}$, $R_{th,j-c,IGBT}$, $R_{th,j-c,Diode}$ are the thermal resistances of heatsink, case to heatsink including heatsink paste, IGBT junction to case and Diode junction to case respectively. P_{S1}, P_{D1}, P_{S2} and P_{D2} are the average power loss in the devices S1, D1, S2 and D2 shown in Fig. 3.2.

common heatsink. The total loss in each switching element SW1 through SW6 shown in Fig. 3.2(b) consists of the IGBT conduction loss (P_{S_cond}), diode conduction loss (P_{D_cond}), IGBT switching loss (P_{S_sw}) and the diode reverse recovery loss (P_{D_rr}). At higher currents, the terminal losses of the modules (P_{Mod_term}) are also included. The analytical computation of the various power loss components in the IGBT and anti-parallel diode has been done using the datasheet parameters based on [101, 103, 104]. The effect of output current ripple on the heatsink temperature rise over ambient is negligible as discussed in [101, 103] and hence has been neglected in the power loss computations. Appendix E gives the equations related to the power loss computations.

The datasheet parameters required to compute the power loss components are dependent on the gate drive resistance, operating current and the maximum operating junction temperature. The various values of the datasheet parameters used for analytical computation of the heatsink temperature are listed in Table 3.5.

Power Loss in One Leg of Inverter: Fig. 3.12(a) shows the plot of the analytically computed loss components in one leg of the inverter for varying load angle or power factor angle, ϕ. ϕ is the angle between fundamental frequency voltage and current at the grid-end of the inverter output filter. In Fig. 3.2(a), ϕ is computed from the voltage and current measured at one of the nodes R_g, Y_g or B_g and in Fig. 3.2(b), the measurement node is 'S'. The current direction for ϕ is assumed to be outward from the inverter as indicated by one of the currents i_R, i_Y or i_B in Fig. 3.2(a) and Fig. 3.2(b). The voltages measurement at the grid-end is considered with respect to the dc bus mid-point 'O'. As seen in the plot, the IGBT switching loss and the diode reverse recovery loss are constant for a chosen switching frequency. But, the conduction losses in the IGBT and diode vary sinusoidally with load angle as the average conduction period of the IGBT and diode varies with the load angle. The sinusoidal variation in the total loss with varying ϕ can be observed from the magnified view of the total power loss curve shown in Fig. 3.12(b) as well as from the expressions given in Appendix E.

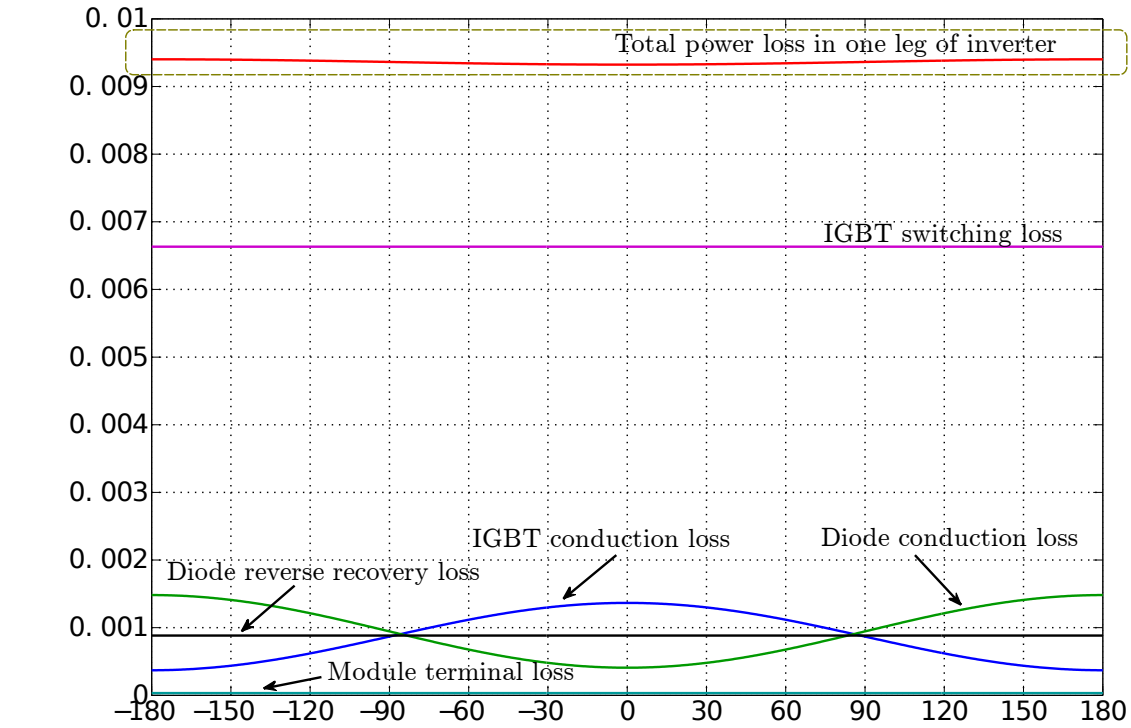
This sinusoidal variation in the total power loss in one leg of the inverter can be represented as,

$$P(\phi) = P_o + P_m sin(\phi - 90^o) \tag{79}$$

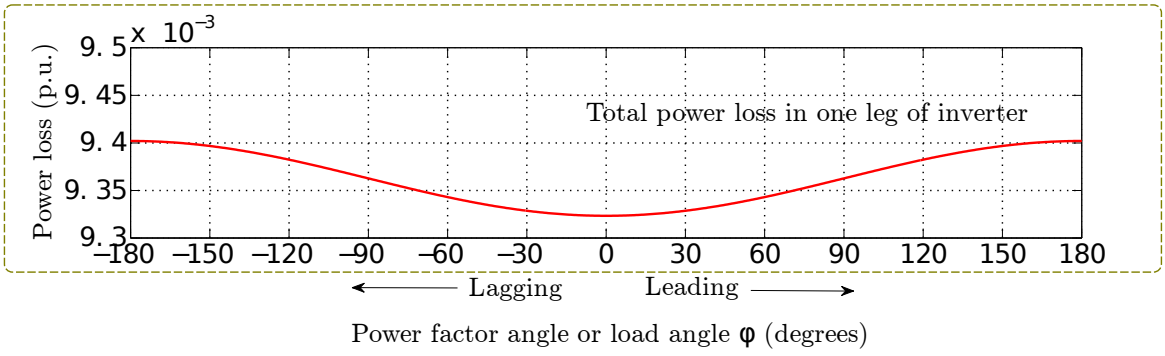
$P(\phi)$ represents the total power loss at a given ϕ. P_o represents the average total power loss and P_m represents the peak of the sinusoidal component of total power loss for varying

Symbol	Value
IGBT	
V_{CE0}	0.7 V
r_{CE}	10.3 $m\Omega$
E_{on}	13.75 mJ
E_{off}	5 mJ
$R_{th,j-c,IGBT}$	0.2 $^oC/W$
Diode	
V_{F0}	0.9 V
r_F	8.1 $m\Omega$
E_{rr}	2.5 mJ
$R_{th,j-c,Diode}$	0.32 $^oC/W$
Module	
$R_{CC'+EE'}$	0.5 $m\Omega$
$R_{th,c-h}$	0.02 $^oC/W$
$V_{dc,test}$	600 V
T_j	175^oC
Heatsink	
$R_{th,h-a}$	0.013 $^oC/W$
Operating Conditions	
V_{dc}	800 V
I_{rated}	40 A
$R_{g,on}, R_{g,off}$	12Ω

Table 3.5: Device Parameters Used in Analytical Computations for Semikron IGBT Module SKM150GB12T4G [102]



(a)



(b)

Figure 3.12: Analytical power loss curves for varying grid power factor angle, ϕ. (a) Power loss in actual system shown in Fig. 3.2(a). The power loss components in one leg has been shown. The power loss curves are the same for all the legs. (b) A magnified view of the total power loss encircled in dashed lines in Fig. 3.12(a).

ϕ.

Total Power Loss in Actual System and Test Configuration: The power factor angle ϕ is the same for the three legs in the actual system as the three-phase grid voltages and the three-phase grid currents are balanced. This can also be observed in Fig. 3.5(a) from phasors $\mathbf{V_{R_g}}$, $\mathbf{V_{Y_g}}$, $\mathbf{V_{B_g}}$, $\mathbf{I_R}$, $\mathbf{I_Y}$ and $\mathbf{I_B}$. Thus, the power loss in the inverter for the actual system is $3 \cdot P(\phi)$.

In the test configuration, the voltage at the short circuit point corresponds to the grid voltage of the LUT and the three-phase currents are balanced. So, the power factor angle is ϕ for the LUT and are $(\phi - 120^o)$ and $(\phi + 120^o)$ for the other two legs. This can also be observed in Fig. 3.5(b) from phasors $\mathbf{V_S}$, $\mathbf{I_R}$, $\mathbf{I_Y}$ and $\mathbf{I_B}$. Thus, the power loss in the inverter for the test configuration is $P(\phi) + P(\phi - 120^o) + P(\phi + 120^o) = 3 \cdot P_o$. The power loss curves for the individual phase legs in the test configuration has been shown in Fig. 3.13.

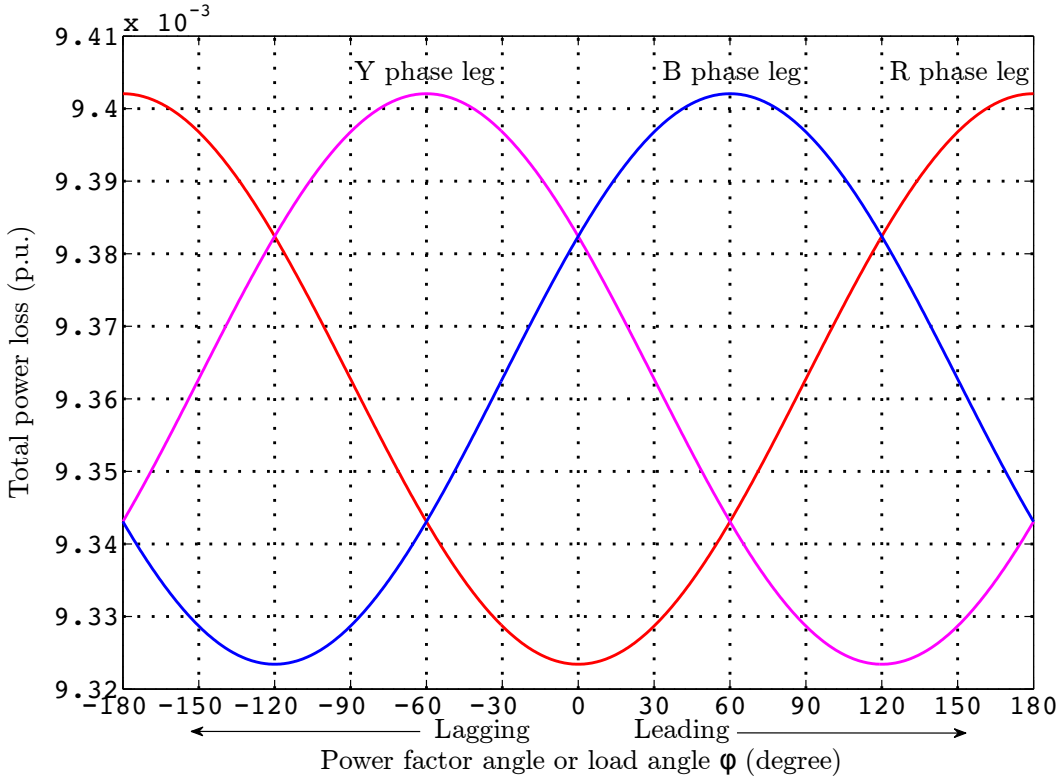


Figure 3.13: Analytical power loss curves in test configuration shown in Fig. 3.2(b) for the phases R,Y and B. The power loss has been shown for varying grid power factor angle, ϕ.

Power Loss Parameters (p.u.)	
P_o	93.63×10^{-4}
P_m	0.395×10^{-4}
Total Power Loss (p.u.)	
Actual System	$3 \cdot 10^{-4} \times (93.63 + 0.395 sin(\phi - 90^o))$
Test Configuration	$3 \cdot (93.63 \times 10^{-4})$
Maximum Error	$3 \cdot P_m = 3 \cdot (0.395 \times 10^{-4}) = 0.42\%$

Table 3.6: Analytical Power Loss in Actual System and Test Configuration with the Three Legs Mounted on a Common Heatsink

Table 3.6 shows the analytically computed power loss parameters, total power loss in the actual system, total power loss in the test configuration and the maximum error in the total power loss for the experimental set-up used. The maximum error in the total power loss is less than 0.5%. A corresponding error exists in the heatsink and junction temperatures also. The maximum error in the total power loss depends on the switching frequency. At lower switching frequencies, the conduction loss is comparable with the switching loss and hence the percentage error is higher. However, even at lower switching frequencies, the percentage error is seen to be small. With the other parameters remaining the same, at switching frequencies of 5 kHz and 2.5 kHz the analytically computed maximum percentage error is 0.7% and 1.05% respectively. The percentage errors indicate that the maximum error percentage in the total power loss in the actual system versus the proposed method is negligible even when the conduction loss is comparable to the switching loss.

In the above discussion, it is assumed that all the three legs of the inverter are mounted on the same heatsink. If each switching element consisting of an IGBT and an anti-parallel diode or each leg of the inverter are mounted on individual heatsinks, the power loss in the LUT is $P(\phi)$ for both the actual system and the test configuration. Hence, the heatsink and junction temperatures also match exactly for the LUT in both the cases.

Fig. 3.14 shows the analytical and experimental heatsink temperature rise over ambi-

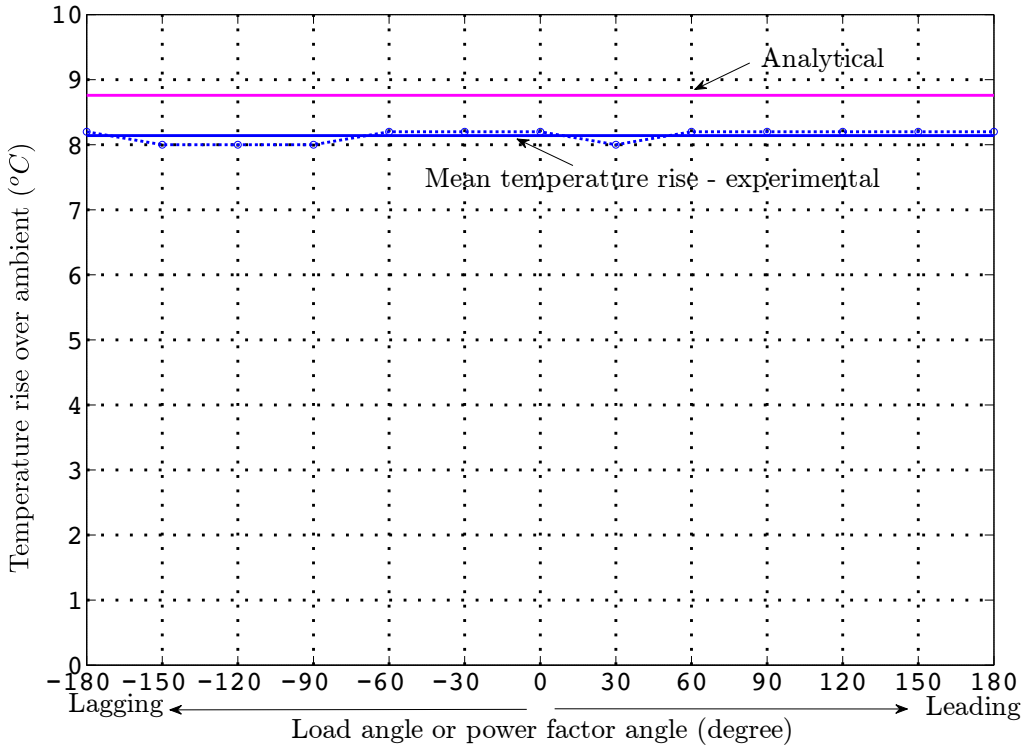


Figure 3.14: Plot of analytical and experimental heatsink temperature rise over ambient for varying ϕ with the three legs of the inverter mounted on the same heatsink and modulated using sine-triangle PWM.

ent for the test system. The experimental temperature rise was measured using 'T' type thermocouples mounted on the heatsink. For the thermal studies, the temperature data was continuously recorded using a data logger till the temperatures reached steady-state condition. The temperatures have been shown for varying grid power factor angles. The error in the heatsink temperature rise over ambient between the analytical and experimental measurement is 0.62^oC. From Fig. 3.14, it can be seen that the nature of the analytical and experimental curves is similar though there is a 7% error between the two curves. The analytical computations of the power loss are done using datasheet specified values extrapolated to the actual gate resistances and dc bus voltage used in the hardware set-up. This can be a source of error observed in the plot as there are various parameters that influence the datasheet values. The analytical computation can be taken only as an indicative number and not as exact since the datasheet graphs and parameters are specified only at specific values

of junction temperatures of the IGBT and diode. The worst case junction temperature is considered for the analytical estimates.

3.8.2.2 Power Loss in Individual Semiconductor Devices

Besides the datasheet parameters of the semiconductor devices, the power loss in the individual semiconductor devices are dependent on the modulation index m, $I_m = I_{rated} \cdot \sqrt{2}$, angle ψ between the voltage and current at the inverter output terminal, switching frequency f_{sw} and the dc bus voltage V_{dc}. The output voltage and current are maintained the same for the LUT in both the actual system and the test configuration. So, all the above mentioned parameters and hence the power loss in the individual semiconductor devices are the same for the LUT in both the cases.

Further, as mentioned in the previous subsection, the other two legs resemble the LUT except for the power factor angles which are $(\phi - 120^o)$ and $(\phi + 120^o)$ respectively. So, for the test configuration, it is ensured that the power loss in the individual semiconductor devices of these legs do not exceed the maximum values expected in the actual system if the inverter is expected to operate in the full range of power factors. The same can be observed from Fig. 3.13. The peak power loss is the same for the three individual legs.

Thus, the semiconductor device thermal testing can be performed satisfactorily using the test configuration for either case of a common or an individual heatsink for the switching elements or modules.

3.8.2.3 Input Power

The input power requirement is less since only the losses in the test configuration needs to be supplied from the input. The input power drawn varied between $1038W$ to $1108W$ for load angle variations from -180^o to $+180^o$ with the output power being $24kVA$. The input power is $\simeq 4.5\%$ of the output VA and corresponds to the losses in the test configuration including the front-end converter. The losses in the front-end converter is less as the current drawn from the input is less. Thus, there is a near 50% reduction in the total power consumed by the proposed thermal test as compared to using two inverters of same rating to perform the thermal test as suggested in existing literature [96].

3.8.3 Testing of DC Bus Capacitors

The temperature rise and hence the life of the dc bus electrolytic capacitors is dependent on the rms current flowing through the capacitor [16]. The equivalent series resistance (ESR) that causes the temperature rise is frequency-dependent [105, 106]. Hence, the frequency spectrum of the current is also equally important along with the rms value. The rms current and the current spectrum of the dc bus capacitor current in the test configuration will be the same as that of the actual system if $i_{cap}(t)$, the instantaneous dc bus capacitor current, is the same in both the cases. $i_{cap}(t)$ is indicated in Fig. 3.2(b). Equivalently, the ac component of the instantaneous dc link current $i_{link}(t)$ shown in Fig. 3.2(b) can also be considered.

From Fig. 3.2(b), the instantaneous dc link current ($i_{link}(t)$) in a two-level inverter is given by [16],

$$i_{link}(t) = S_R(t) \cdot i_{R_i}(t) + S_Y(t) \cdot i_{Y_i}(t) + S_B(t) \cdot i_{B_i}(t) \tag{80}$$

where, $S_R(t)$, $S_Y(t)$ and $S_B(t)$ are the instantaneous switch states of the top IGBTs S1, S3 and S5 respectively of the three phase legs R, Y and B of the inverter shown in Fig. 3.2(b). The switch state of an IGBT is '1' when it is ON and is '0' when it is OFF. $i_{R_i}(t)$, $i_{Y_i}(t)$ and $i_{B_i}(t)$ are the instantaneous fundamental frequency currents in the inverter-side inductors of the inverter as shown in Fig. 3.2. The effect of the inverter output ripple current on the dc bus capacitor current is negligible [16] and has been ignored. The fundamental frequency current through the output filter capacitors is negligible. Hence, currents i_{R_i}, i_{Y_i} and i_{B_i} can be replaced by i_R, i_Y and i_B respectively. Then, we have,

$$i_{link}(t) = S_R(t) \cdot i_R(t) + S_Y(t) \cdot i_Y(t) + S_B(t) \cdot i_B(t) \tag{81}$$

From (81), if the test method ensures that the instantaneous switch states and the instantaneous output grid-side inductor currents are the same as the actual system, then the ac component of $i_{link}(t)$ and hence $i_{cap}(t)$ will be identical for the test configuration and the actual system. The dc component of $i_{link}(t)$ is dependent on the losses in the switching devices and on the losses at the output. However, since the dc component of $i_{link}(t)$ is supplied by the front-end converter or any dc source that is connected to the dc bus capacitors to supply the losses in the system, it is not of interest in the thermal testing of dc bus capacitors.

Fig. 3.15(a) and Fig. 3.15(b) show the three-phase inverter output voltages and output grid-side inductor currents for the actual system and the test configuration for a represen-

tative lagging grid power factor angle of 30^o. The instantaneous switch states of the top devices are dependent on the inverter output three-phase voltages. Hence, Fig. 3.15 is a representation of the instantaneous switch states and the instantaneous output grid-side inductor currents. It can be observed from the figure that the dc bus capacitor currents are not the same for the actual system and the test configuration. This is clarified further through Fig. 3.16 which shows the switch states for the actual system and the test configuration at a representative angle of 60^o of the waveforms shown in Fig. 3.15. The instantaneous switch states can be observed to be different for the actual system and the test configuration though the instantaneous currents are the same in both the cases.

In the following Sections 3.8.3.1 and 3.8.3.2, the instantaneous switch states and the instantaneous output grid-side inductor currents are analysed in detail to propose a method to test the dc bus capacitors.

3.8.3.1 Instantaneous Switch States

The instantaneous switch states are dependent on the instantaneous duty ratios of the switches. Hence, it is equivalent to analyze the instantaneous duty ratios of the top switches.

Let the grid voltages be given by,

$$\begin{aligned} v_{R_g}(t) &= V_m sin(\omega t) \\ v_{Y_g}(t) &= V_m sin(\omega t - 120^o) \\ v_{B_g}(t) &= V_m sin(\omega t + 120^o) \end{aligned} \tag{82}$$

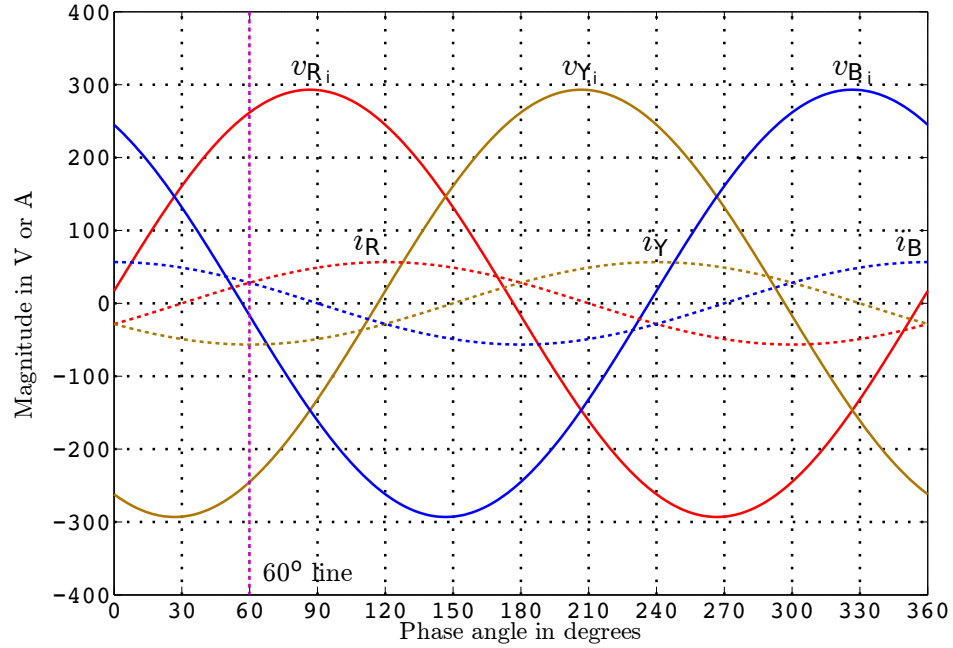
where, $V_m = V_g\sqrt{2}$.

And, let the three phase currents flowing into the grid be given by,

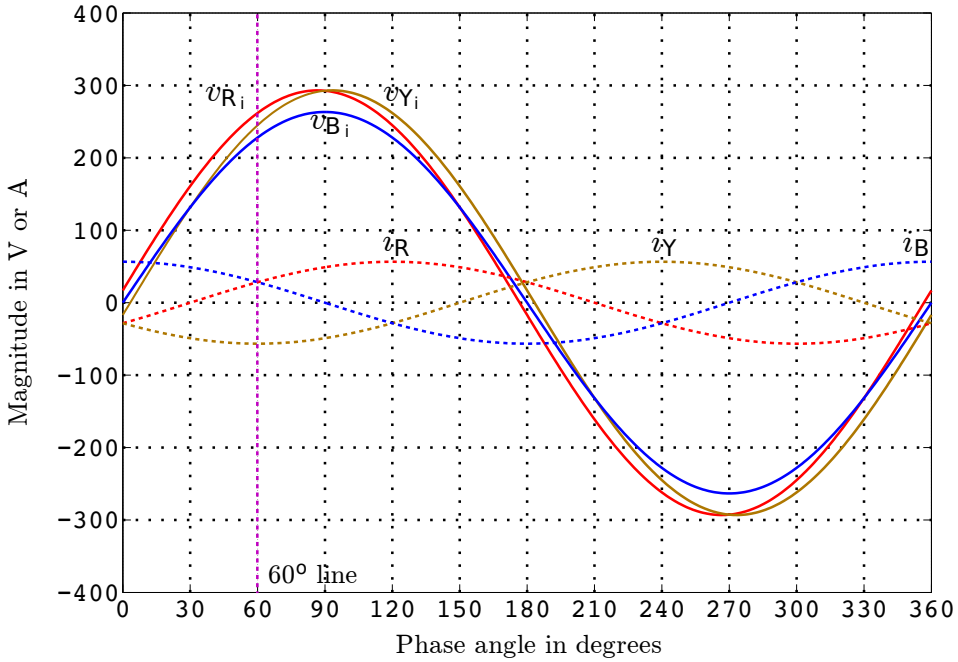
$$\begin{aligned} i_R(t) &= I_m sin(\omega t - \phi) \\ i_Y(t) &= I_m sin(\omega t - \phi - 120^o) \\ i_B(t) &= I_m sin(\omega t - \phi + 120^o) \end{aligned} \tag{83}$$

where, $I_m = I_{rated}\sqrt{2}$.

Let, $D_R(t)$, $D_Y(t)$ and $D_B(t)$ be the instantaneous duty ratios of devices S1, S3 and S5 respectively. Then, we have for the actual system under steady state neglecting the small fundamental frequency current through the filter capacitors,

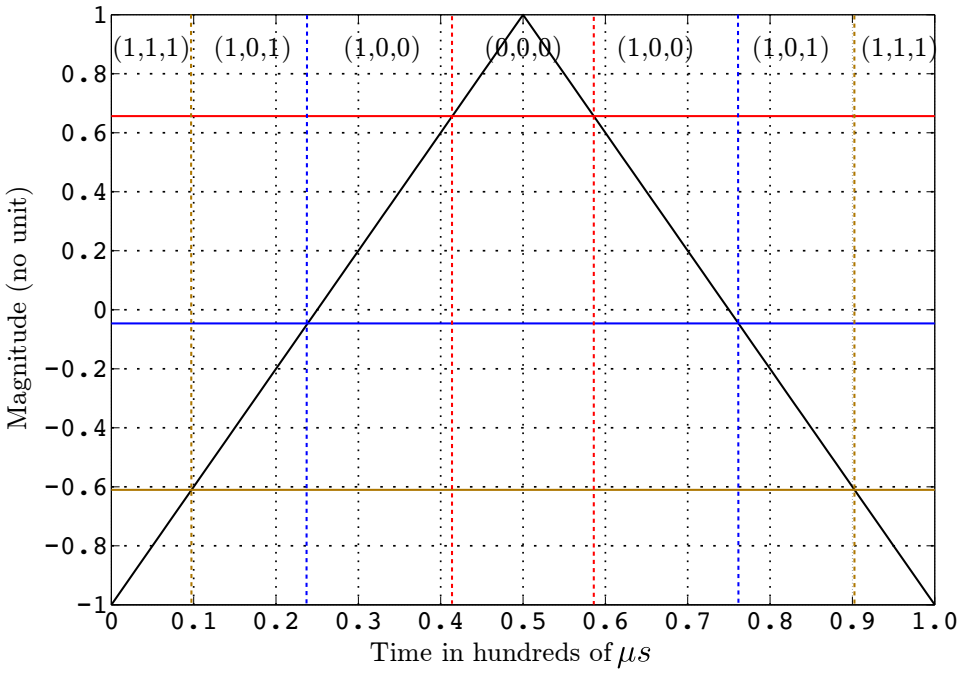


(a)

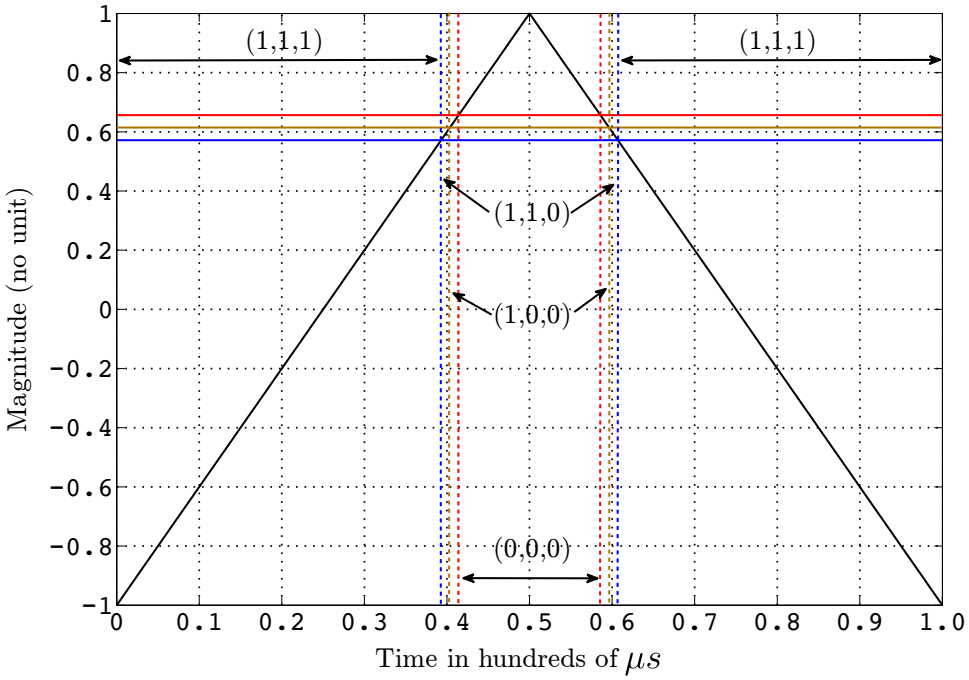


(b)

Figure 3.15: Three-phase inverter voltages (v_{R_i}, v_{Y_i} and v_{B_i}) and three-phase grid-side inductor currents (i_R, i_Y and i_B) for a lagging grid power factor angle of 30^o. (a) In the actual system. (b) In the test configuration.



(a)



(b)

Figure 3.16: Switching cycle at the 60^o line shown in Fig. 3.15. The switching states S_R, S_Y and S_B during the different intervals are indicated in the format (S_R, S_Y, S_B). (a) For actual system. (b). For test configuration.

$$
\begin{aligned}
D_R(t)_{act} &= \frac{1}{2} + \frac{1}{2} \cdot \frac{V_m}{V_{dc}/2} \cdot sin(\omega t) + \frac{1}{2} \cdot \frac{\omega L I_m}{V_{dc}/2} \cdot sin(\omega t - \phi + 90^o) \\
D_Y(t)_{act} &= \frac{1}{2} + \frac{1}{2} \cdot \frac{V_m}{V_{dc}/2} \cdot sin(\omega t - 120^o) + \frac{1}{2} \cdot \frac{\omega L I_m}{V_{dc}/2} \cdot sin(\omega t - \phi - 120^o + 90^o) \\
D_B(t)_{act} &= \frac{1}{2} + \frac{1}{2} \cdot \frac{V_m}{V_{dc}/2} \cdot sin(\omega t + 120^o) + \frac{1}{2} \cdot \frac{\omega L I_m}{V_{dc}/2} \cdot sin(\omega t - \phi + 120^o + 90^o) \quad (84)
\end{aligned}
$$

And, for the test configuration under steady state,

$$
\begin{aligned}
D_R(t)_{test} &= \frac{1}{2} + \frac{1}{2} \cdot \frac{V_m}{V_{dc}/2} \cdot sin(\omega t) + \frac{1}{2} \cdot \frac{\omega L I_m}{V_{dc}/2} \cdot sin(\omega t - \phi + 90^o) \\
D_Y(t)_{test} &= \frac{1}{2} + \frac{1}{2} \cdot \frac{V_m}{V_{dc}/2} \cdot sin(\omega t) + \frac{1}{2} \cdot \frac{\omega L I_m}{V_{dc}/2} \cdot sin(\omega t - \phi - 120^o + 90^o) \\
D_B(t)_{test} &= \frac{1}{2} + \frac{1}{2} \cdot \frac{V_m}{V_{dc}/2} \cdot sin(\omega t) + \frac{1}{2} \cdot \frac{\omega L I_m}{V_{dc}/2} \cdot sin(\omega t - \phi + 120^o + 90^o) \quad (85)
\end{aligned}
$$

From (84) and (85), it can be observed that the duty ratios are not the same for the actual system and the test configuration. The modulating references are a set of balanced sine waveforms for the actual system while they primarily contain a fundamental frequency common mode component in the test configuration. The above observation can be made from the phasor diagrams of Fig. 3.5(a) and Fig. 3.5(b) also. The modulating references in the test configuration can be made balanced as a first step towards making the duty ratios to be the same in the actual system and the test configuration. The phasor diagrams show that this can be done by setting the fundamental frequency common mode voltage to zero. With the common mode voltage set to zero, we have for the test configuration under steady state,

$$
\begin{aligned}
D_R(t)_{test} &= \frac{1}{2} + \frac{1}{2} \cdot \frac{\omega L I_m}{V_{dc}/2} \cdot sin(\omega t - \phi + 90^o) \\
D_Y(t)_{test} &= \frac{1}{2} + \frac{1}{2} \cdot \frac{\omega L I_m}{V_{dc}/2} \cdot sin(\omega t - \phi - 120^o + 90^o) \\
D_B(t)_{test} &= \frac{1}{2} + \frac{1}{2} \cdot \frac{\omega L I_m}{V_{dc}/2} \cdot sin(\omega t - \phi + 120^o + 90^o) \quad (86)
\end{aligned}
$$

The next step is to equalize the modulation indices in (84) and (86). The filter inductor drop is small compared to the grid voltages in the actual system. So, the duty ratio for the actual system under steady state can be approximated by neglecting the filter inductor drop. This is done to get an intuitive understanding of how the modulation indices can be made equal. The approximated duty ratios of the actual system are given by,

$$\begin{aligned} D_R(t)_{act} &\simeq \frac{1}{2} + \frac{1}{2} \cdot \frac{V_m}{V_{dc}/2} \cdot sin(\omega t) \\ D_Y(t)_{act} &\simeq \frac{1}{2} + \frac{1}{2} \cdot \frac{V_m}{V_{dc}/2} \cdot sin(\omega t - 120^o) \\ D_B(t)_{act} &\simeq \frac{1}{2} + \frac{1}{2} \cdot \frac{V_m}{V_{dc}/2} \cdot sin(\omega t + 120^o) \end{aligned} \tag{87}$$

From (86) and (87), the modulation indices will be equal if $\frac{\omega L I_m}{V_{dc}/2}$ equals $\frac{V_m}{V_{dc}/2}$. With the fundamental frequency, filter inductor values, rated load current and rated grid voltage being fixed, the only possible way to achieve equal modulation indices is by reducing the dc bus voltage in the test configuration. The reduced dc bus voltage to be used to test the dc bus capacitors can be found using the relationship, $\frac{\omega L I_m}{V_{dc,reduced}/2} = \frac{V_m}{V_{dc}/2}$.

For experimental validation, the dc bus is set at a lower voltage of $V_{dc,reduced} = 60V$ instead of 800 V so that the modulation index for the actual system and the test configuration are almost the same as given below using parameters listed in Table 3.3.

$$m_{act} \simeq \frac{V_g\sqrt{2}}{V_{dc}/2} = 0.707 \tag{88}$$

$$m_{test} = \frac{(2 * \pi * 50) \cdot (L_1 + L_2) \cdot I_{rated}\sqrt{2}}{V_{dc,reduced}/2} = 0.652 \tag{89}$$

By reducing the dc bus voltage, we are forcing similar currents as in the actual system to flow into the dc bus capacitors of the test configuration. It may be noted that the losses and hence the temperature rise in the dc bus capacitors is due to the ripple current through the same. The dc bus voltage affects only the leakage current in the capacitor. The power loss contribution due to the leakage current is relatively small compared to the losses due to the Equivalent Series Resistance (ESR) and is usually ignored in the thermal studies of electrolytic capacitors.

3.8.3.2 Instantaneous Output Grid-Side Inductor Currents

The instantaneous output currents $i_R(t)$, $i_Y(t)$, $i_B(t)$ are dependent on the magnitude of the three-phase balanced output currents and the phase angle between the output voltage and the output current. The output current magnitude is the same for both the actual system and the test configuration with a reduced dc bus voltage as suggested in the previous subsection. However, with a reduced dc bus voltage and the CM made zero, a balanced three-phase voltage is now applied directly to a purely inductive balanced load. This fixes the phase angle between the inverter output voltage and the current at 90^o. Hence, unlike the actual system where the phase angle can be varied from -180^o to $+180^o$, there is only one possible test operating point for the proposed method.

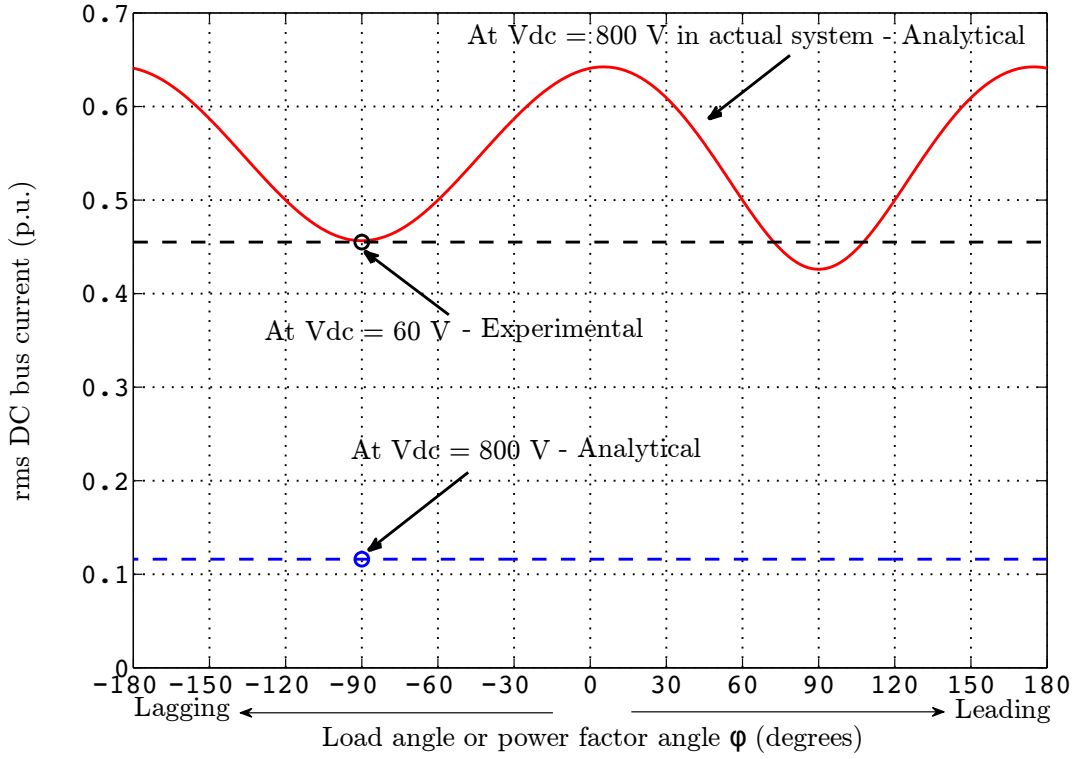


Figure 3.17: Analytical dc bus rms current of the actual system for varying grid power factor angles at a dc bus voltage of 800 V, analytical dc bus rms current of the test configuration for a lagging inverter power factor angle of 90^o at a dc bus voltage of 800 V and experimental dc bus rms current of the test configuration for a lagging inverter power factor angle of near 90^o at a reduced dc bus voltage of 60 V.

Fig. 3.17 shows the analytically computed rms current in the dc bus capacitors for varying grid power factor angles in case of the actual system. The experimental rms current for the test operating point is also shown. As the inverter uses a busbar structure for the dc bus connections, the dc bus current has been estimated from the experimental output filter currents and gating signals. The experimental value closely matches with the analytical value. Further, it can be observed that the experimental dc bus capacitor rms current is 0.455 p.u. which is about 71% of the rms current at 0^o where it is highest and measures 0.642 p.u. The analytical value of the rms current for the test configuration with a dc bus voltage of 800 V for 90^o lagging inverter power factor angle neglecting the effect of the small common mode currents at the output is also shown in the plot and measures 0.116 p.u. This is just 18% of the highest dc bus rms current in the actual system. Hence, it is required to lower the dc bus voltage so that the dc bus capacitors are tested under near equivalent loading conditions.

3.8.4 Testing of Output Filter Components

For the output filter components to be tested effectively, it must be ensured that,

1. The rms value of the fundamental frequency currents is the same in the actual system and the test configuration.
2. The rms value of the ripple current is the same in the actual system and the test configuration.
3. The individual spectral components of the ripple current is the same in the actual system and the test configuration.
4. The currents through the filter components in the legs other than the LUT do not exceed their maximum limits observed in the actual system.

In the list above, 3 is required because the temperature rise in the filter components do not depend on the rms value of the current alone. It also depends on the individual spectral components of the current. In the capacitor, the ESR which decides the power loss and hence the temperature rise is frequency dependent. The ESR reduces with frequency [107]. Similarly, in the inductors, both the core loss and copper loss are frequency dependent. While, hysteresis and eddy current loss which together constitute the core loss can be expressed

as equations that are functions of frequency of the flux [91, 108], the copper loss is also dependent on the frequency as the resistance varies due to skin and proximity effects. So, both the actual system and the test configuration should have the same spectral pattern of current. Section 3.8.4.1 and Section 3.8.4.2 compares the fundamental frequency component and ripple component of currents in the output filter components of the LUT respectively for the actual system and the test configuration.

3.8.4.1 Fundamental Frequency Currents in the Output Filter Components

For the LUT, the fundamental frequency current in each individual output filter components is identical in the actual system and the test configuration. The current control used in the test configuration ensures that the fundamental frequency component of current through the grid side output filter inductor of the LUT match exactly with that of the actual system. The fundamental frequency voltage across the output filter capacitor in the R-phase LUT is given by $\mathbf{V_S} + \mathbf{V_{L_{R2}}} = \mathbf{V_{R_g}} + \mathbf{V_{L_{R2}}}$. This being identical to the filter capacitor voltage in the R-phase leg of the actual system, the fundamental frequency current through the output filter capacitor is identical in the actual system and the test configuration. Since the inverter side filter inductor current is the sum of the currents through the grid side filter inductor and the output filter capacitor current, it also matches the fundamental frequency current in the actual system.

3.8.4.2 Ripple Currents in the Output Filter Components

The output LCL filter is designed based on the recommendations of the IEEE Standard [28, 65]. The recommendations being very stringent, the grid side inductor ripple current is negligible and has not been considered. Hence, the inverter side inductor and the filter capacitor are assumed to carry the same ripple current. All instantaneous voltages and instantaneous currents at the LUT in the test configuration, including the switching voltage waveforms at its output terminal, being exactly identical to that in the actual system, the instantaneous ripple current is the same in both the cases. This ensures the rms value and the individual spectral components of the ripple current to be identical in both the cases. It should be noted that the CM and DM components of voltages are different in the actual system and the test configuration. In spite of this, the ripple currents are identical in both

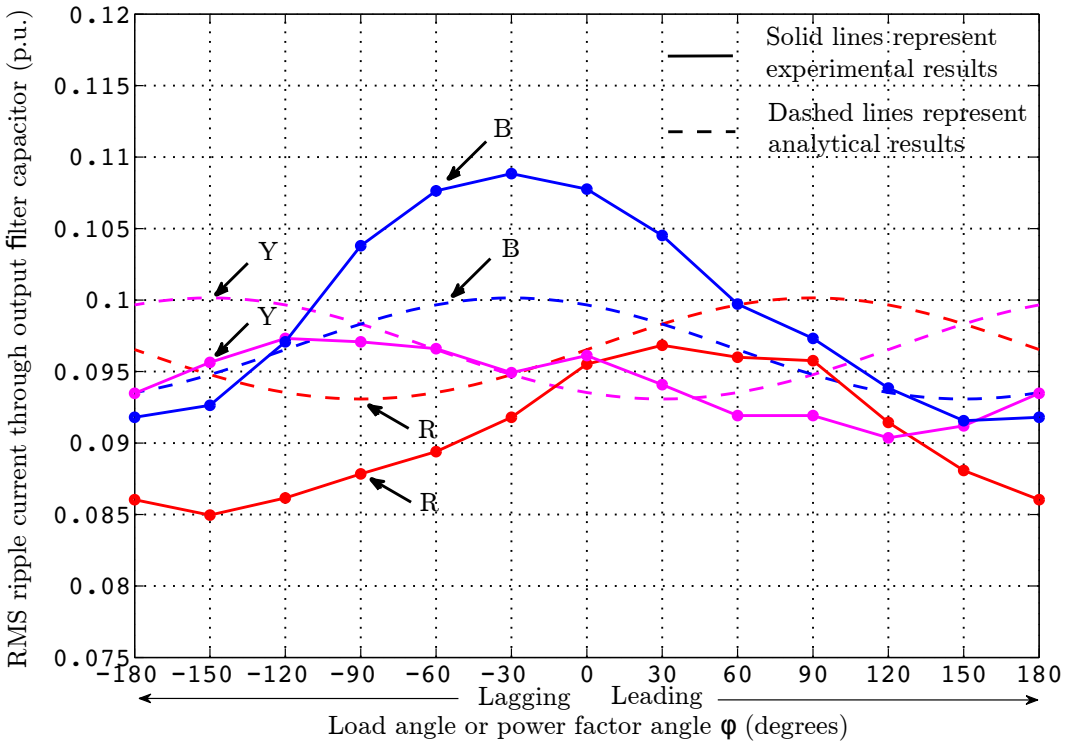


Figure 3.18: Analytical and experimental rms ripple currents in the output filter capacitors of the three legs in the test configuration at rated operating conditions. R-phase is the LUT.

the cases as the instantaneous switching voltages are the same in both the cases and the HFCM and HFDM circuits of the actual system and the HFCM and HFDM circuits of the test configuration are all identical as shown in Fig. 3.6. In other words, the CM and DM components of the ripple current are different in the actual system and the test configuration. But, the total instantaneous ripple current remains the same in both the cases.

From Fig. 3.5, it can be observed that the current controlled legs are identical to the LUT with the load angle or power factor angle shifted by -120^o and $+120^o$ respectively. So, the fundamental frequency currents and the ripple currents through the filter components connected to these legs will not exceed their normal maximum values observed in the actual system operated at the rated conditions assuming that the inverter is designed to operate at all grid power factor angles. Fig. 3.18 shows analytical and experimental rms ripple currents through the filter capacitor of the three phases for varying power factor angles. The experimental values follow a sinusoidal pattern observed in the analytical results. The

differences in the p.u. rms values were observed to be of the same order as the tolerances of the inductors used in the hardware. The variation in inductance is around 5%. This leads to about 5% variation in the ripple current also.

3.9 Analysis and Experimental Results – 3-Wire Configuration

In a 3-wire configuration, the fourth wire shown in dotted lines in Fig. 3.2 is disconnected. Disconnecting the fourth wire changes only the CM currents. In the test configuration, the fundamental frequency currents can still be maintained to be three-phase balanced and at the rated value. But, since the voltages at the output terminals of the test configuration are predominantly CM, the ripple is now very low compared to the 3-wire configuration of the actual system. As discussed earlier, the effect of output ripple current on the thermal testing of the semiconductor devices and the testing of the dc bus capacitors is negligible. Hence, the thermal testing of the semiconductor devices and the dc bus capacitor testing can be done for the 3-wire configuration as it was done for the 4-wire case. However, for the output filter components, the test configuration emulates the actual system only at the fundamental frequency. The high frequency losses in the output filter cannot be characterized for the 3-wire configuration. The tests for the 3-wire configuration are explained in the context of space vector modulation scheme. The experimental results use the conventional space vector pulse width modulation (CSVPWM) scheme at a dc bus voltage of 700 V. The dc bus voltage has been reduced so as to have similar modulation indices for the sine-triangle and CSVPWM schemes.

The modulating signal in space vector based PWM techniques can be seen as the sum of a fundamental frequency sine wave modulating signal and a common mode modulating signal. In particular, for the CSVPWM scheme, the common mode signal is half of the mid value of the three sinusoidal references at any instant as shown in Fig. 3.19. The common mode signal can be approximated using a triangular waveform of peak equal to one-fourth of the peak of the sine waveform. The triangular waveform can further be approximated using its fundamental frequency sine waveform. This approximated sine is shown in Fig. 3.19 and is useful in the thermal analysis of the semiconductor devices. The approximated sine is a third harmonic of the fundamental frequency sine wave modulating signals as can be observed from the waveforms. Fig. 3.20 shows the actual and approximated CSVPWM modulating

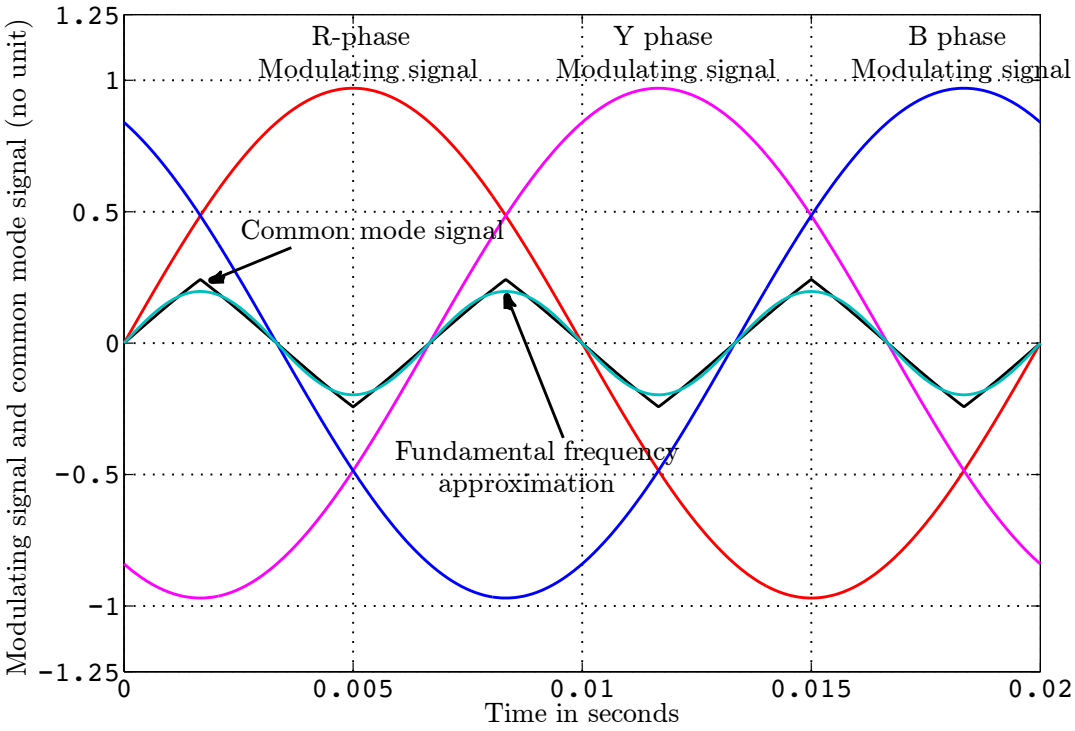


Figure 3.19: Three-phase sinusoidal modulating signals and the common mode required to generate the references in the case of CSVPWM. The common mode signal can be approximated using a triangular waveform of peak equal to one-fourth of the peak of the sine waveform. Further, the triangular waveform can itself be approximated using its fundamental frequency component as shown.

signals. The third harmonic sine approximation of the common mode modulating signal can be seen to give very close approximation.

3.9.1 Current Control

The current control remains the same as in the case of a 4-wire system except for the third harmonic common mode added to the three phase references. In case of the actual system, the third harmonic common mode is generated from the three phase references as explained in Fig. 3.19 and Fig. 3.20. In case of the test configuration, the third harmonic to be added to all the three phases should be the same as that added to the LUT, say R-phase leg,

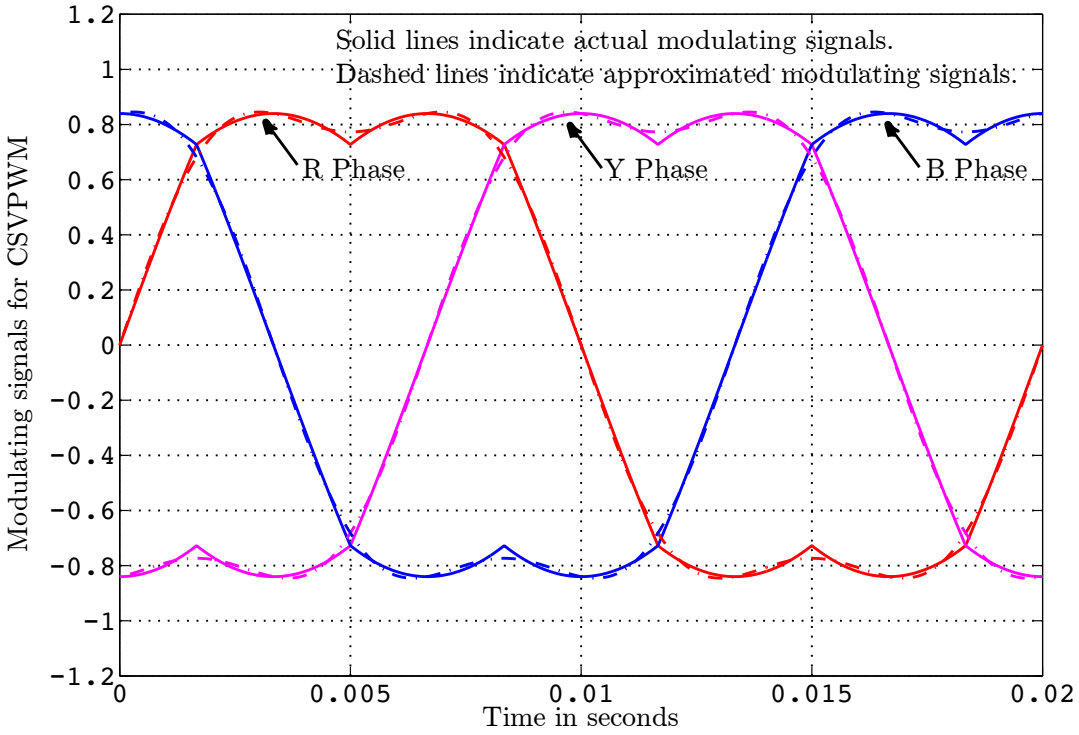


Figure 3.20: Modulating signals for CSVPWM. The actual and the approximated waveforms using the common mode approximation shown in Fig. 3.19 have been shown.

in the actual system. The generation of this reference cannot be done directly using the three phase sinusoidal references of the test configuration as only the LUT has the same reference waveform in both the actual system and the test configuration. The other two phase references are not the same in the two cases. So, in the test configuration, the third harmonic waveform is generated by using two virtual waveforms that correspond to Y and B phase of the actual system – created internally in the digital processor. The control block diagram still remains the same as in Fig. 3.9 except for an additional third harmonic component ($v_{cm,3}$) added to v_{R_iO}. Thus, we have for the three-wire configuration,

$$v_{cm} = v_{R_g} + v_{cm,3} \tag{90}$$

And,

$$v_{R_iO} = v_{R_g} + v_{cm,3} + v_{R_iO,dm} \tag{91}$$

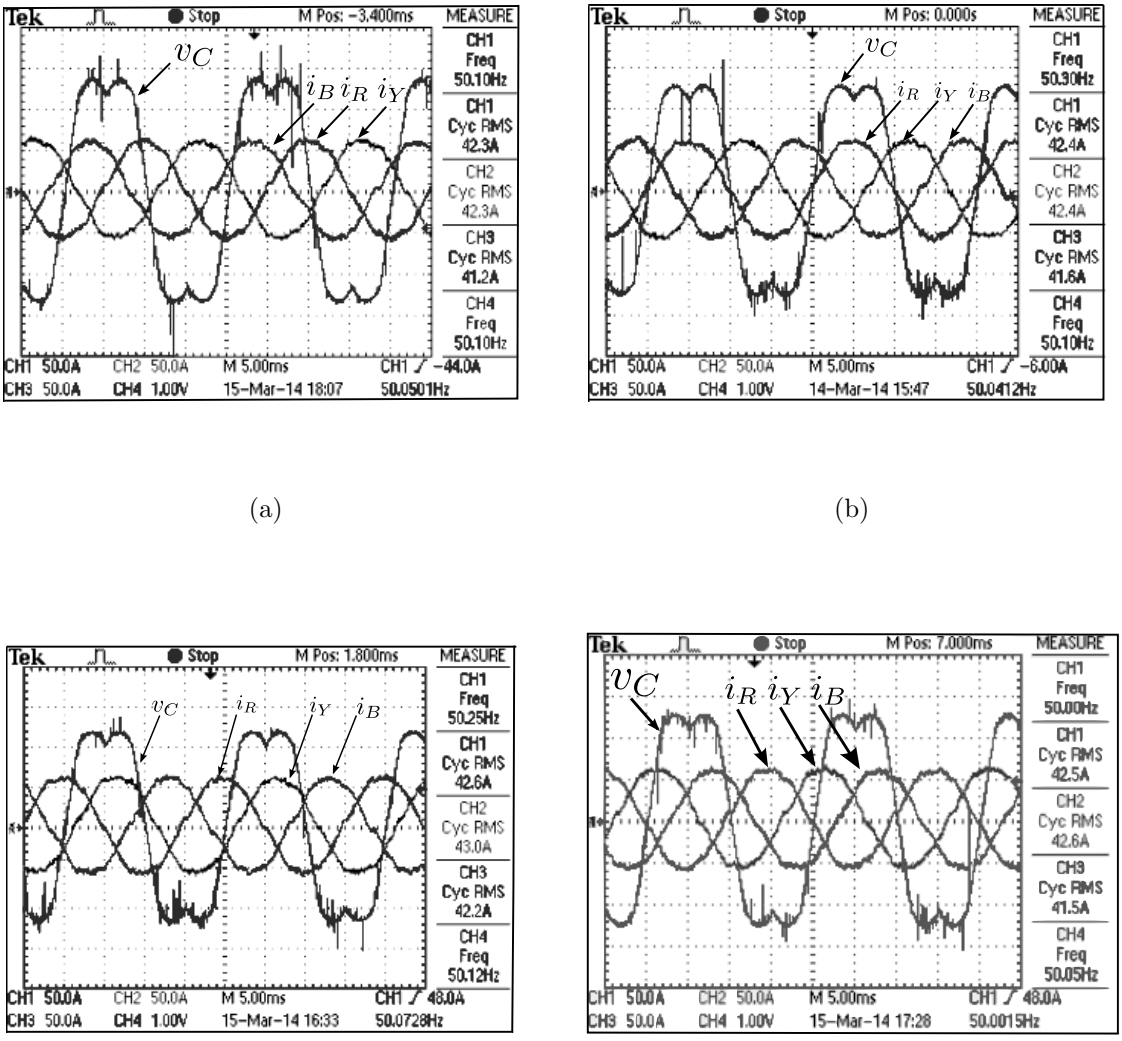


Figure 3.21: Three phase currents CH1: i_R, CH2: i_Y, CH3: i_B and R-phase LCL filter capacitor voltage CH4: v_C in the test configuration while emulating a grid-connected inverter in a 3-wire configuration that injects (a) a 90^o lagging current (b) an in-phase current (c) a 90^o leading current (d) an 180^o out-of-phase current at the point of common coupling with the grid. Experimental parameters are as shown in Table. 3.3. CH1, CH2, CH3: 50A/div; CH4: 100V/div.

Fig. 3.21 shows the three phase currents i_R, i_Y, i_B and the voltage v_C across the R-phase LCL filter capacitor while emulating a grid-connected inverter that injects a 90^o lagging current, an in-phase current, a 90^o leading current and an 180^o out-of-phase current at the point of common coupling with the grid in a 3-wire configuration that uses CSVPWM. The experimental parameters are as shown in Table. 3.3.

3.9.1.1 Effect of Third Harmonic Common Mode on Voltage References

In the test configuration, the three phase references are not balanced. So, adding the third harmonic common mode to the three phases leads to skewed voltage references as shown in the simulated result in Fig. 3.22 for an operating grid power factor of 30^o lag. The nature and extend of the skew depends on the operating grid power factor as can be observed from

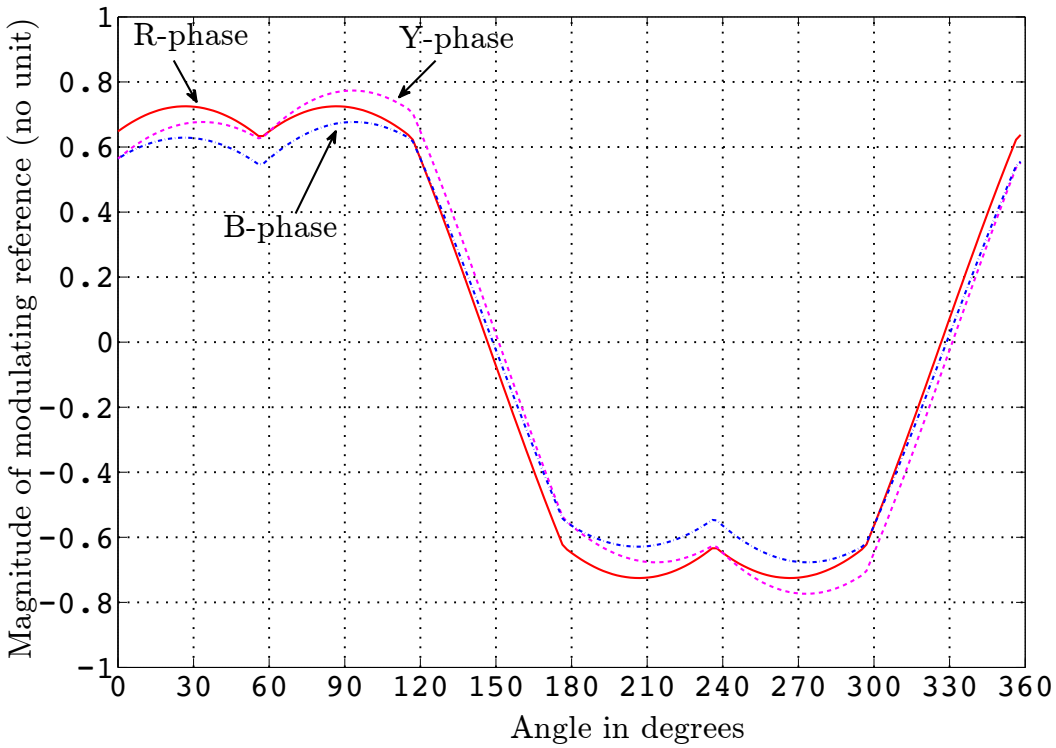
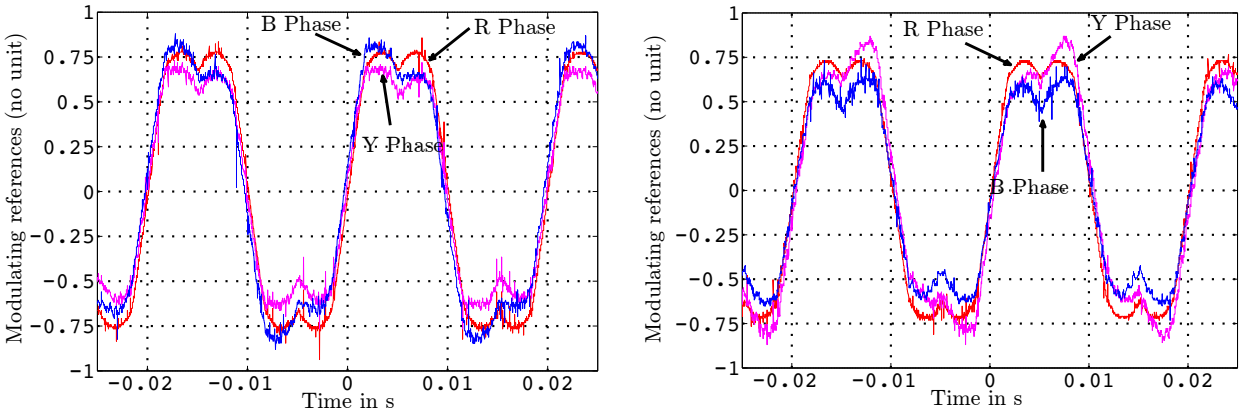
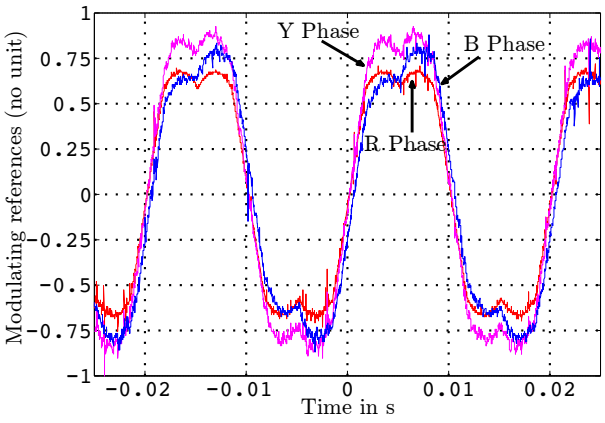


Figure 3.22: Simulated three-phase voltage references for the test configuration in a 3-wire configuration using CSVPWM modulation scheme. The references have been simulated for a grid power factor angle of 30^o lag.



(a)

(b)



(c)

Figure 3.23: Experimental three-phase skewed voltage references in the test configuration for CSVPWM at (a) 90^o lagging grid power factor (b) unity grid power factor (c) 90^o leading grid power factor. The experimental conditions are as mentioned in Table. 3.3. R-phase leg is the LUT. The modulating signals have been scaled to -1 V to +1 V, the usual range used in a triangle comparison method of gate signal generation.

the experimental waveforms shown in Fig. 3.23 for 90^o lagging current, an in-phase current and a 90^o leading current. As can be seen, the reference voltages for the legs other than the LUT might have peak magnitudes greater than the peak magnitude observed in the actual system. This means that the modulation indices might be pushed to their limits when operated under the suggested test configuration.

The left Y axis of Fig. 3.24 shows the plot of the simulated peaks of the three-phase modulating references in the actual system and the test configuration for a 3-wire configuration operated using CSVPWM at various grid power factor angles. The various parameters used for simulation appear in Table. 3.3. The right Y axis shows the plot of percentage of modula-

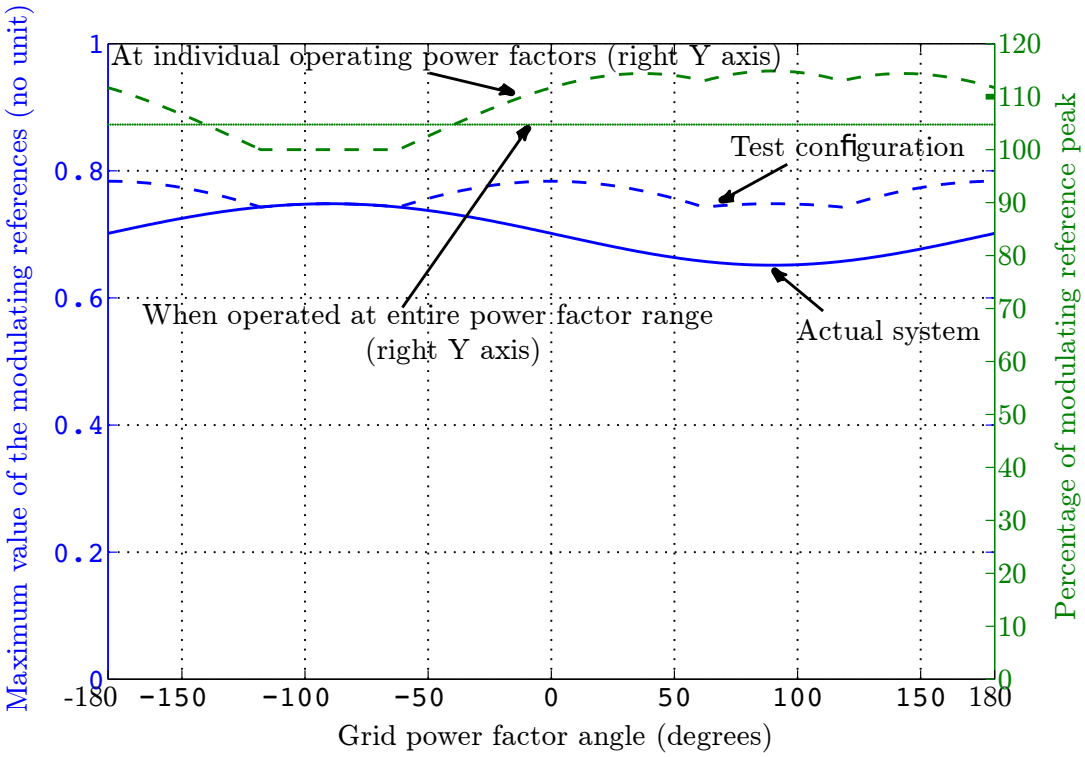


Figure 3.24: Y1 axis (left Y axis): Modulation peak at different operating grid power factors for the actual system (solid line) and the test configuration (dashed line). Y2 axis (right Y axis): Percentage of modulation peak for the test configuration as compared to that of the actual system when operated at different grid power factors (dashed line) and when designed for the entire grid power factor range (solid line). The plots are the simulated results for the parameters given in Table. 3.3.

tion peak in the test configuration in comparison with that of the actual system at different grid power factor angles. As can be observed, the percentage increase in peak modulation depends on the operating grid power factor angle and can be as high as 14.8% corresponding to a grid power factor angle of 90^o lead. From the perspective of dc bus requirement, this means that when designed for operation only at 90^o lead, the ideal minimum dc bus voltage requirement is 456V for the actual system whereas to run the proposed test, a minimum dc bus voltage of 524V i.e. an increase of 68V is required. However, if the inverter is designed for the entire range of grid power factors, the percentage increase in peak modulation is less at 4.7%. This means that the minimum dc bus requirement in the actual system and the test configuration are 524V and 549V respectively i.e. an increase of only 25V is required. In most practical cases, the dc bus voltage might be sufficient to run the test using the proposed test configuration even when the inverter is designed to operate at particular grid power factor.

3.9.2 Thermal Testing of Semiconductor Devices

The closed-form expressions for the switching loss in the IGBTs and diodes and the module terminal losses are the same for sine triangle and CSVPWM schemes. Only the conduction losses differ with the PWM scheme. Closed-form expressions for conduction loss in the IGBT and diode can be arrived at in case of CSVPWM scheme by approximating the common mode by a triangular waveform and by considering only the fundamental component of the triangular common mode. The expressions are given in Appendix E. This approximation would give very close results to that obtained using the exact common mode component as the voltage references generated by the approximation are very close to the exact references as can be observed from Fig. 3.20. Further, the total loss itself is not very different from the total loss obtained for a sine triangle PWM scheme with the same dc bus voltage as shown in Fig. 3.25. So, the variation of the loss per leg in the actual system and the test configuration with the grid power factor angle can be approximated using a sine function $P(\phi) = P_o + P_m sin(\phi - 90^o)$ as in Section 3.8.2 as the effect of third harmonic terms of power loss is negligible as can be observed from Fig. 3.25. The maximum percentage error in the total loss of the test configuration as compared to that of the actual system is 0.51%. Hence, the proposed test method is useful for thermal testing of semiconductor devices in case of 3-wire also.

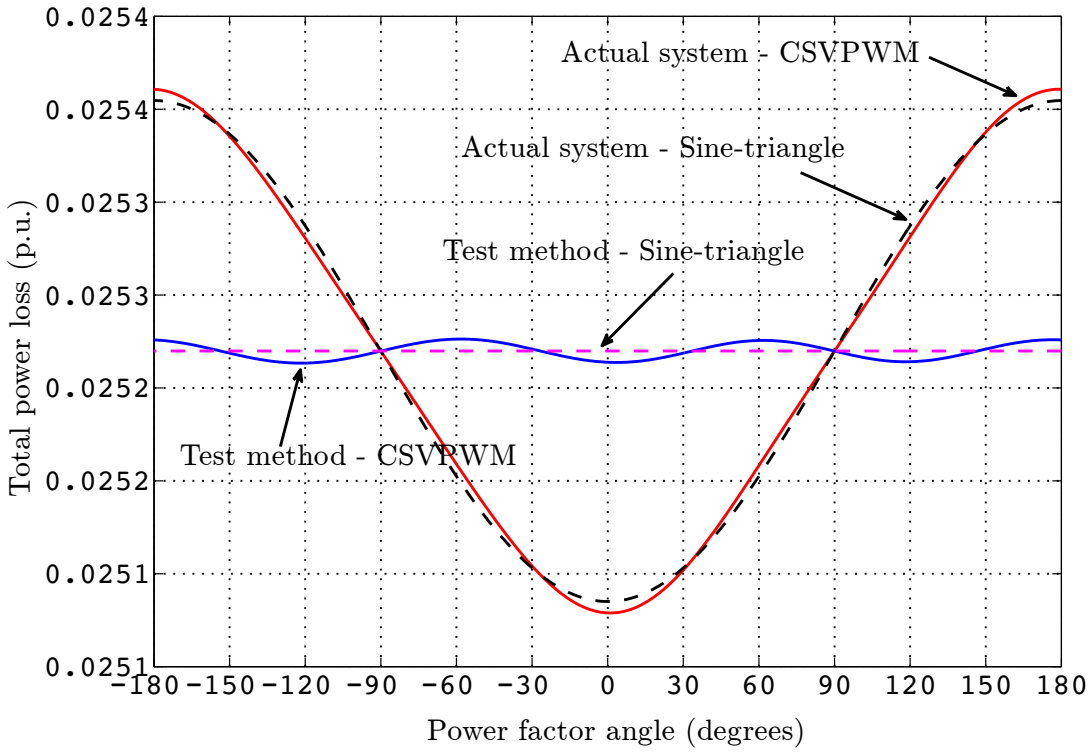


Figure 3.25: Simulated total power loss for three-legs in a three-phase 3-wire configuration that uses CSVPWM scheme for varying grid power factor angles. The total power loss has been shown for the actual system and the test configuration. Also, the total power loss for sine triangle modulation scheme for the actual system and test configuration have been shown. The total power loss can be seen to be very close in case of Sine-triangle and CSVPWM schemes. The parameters used are as in Table 3.3. The dc bus voltage is 700V for all the plots.

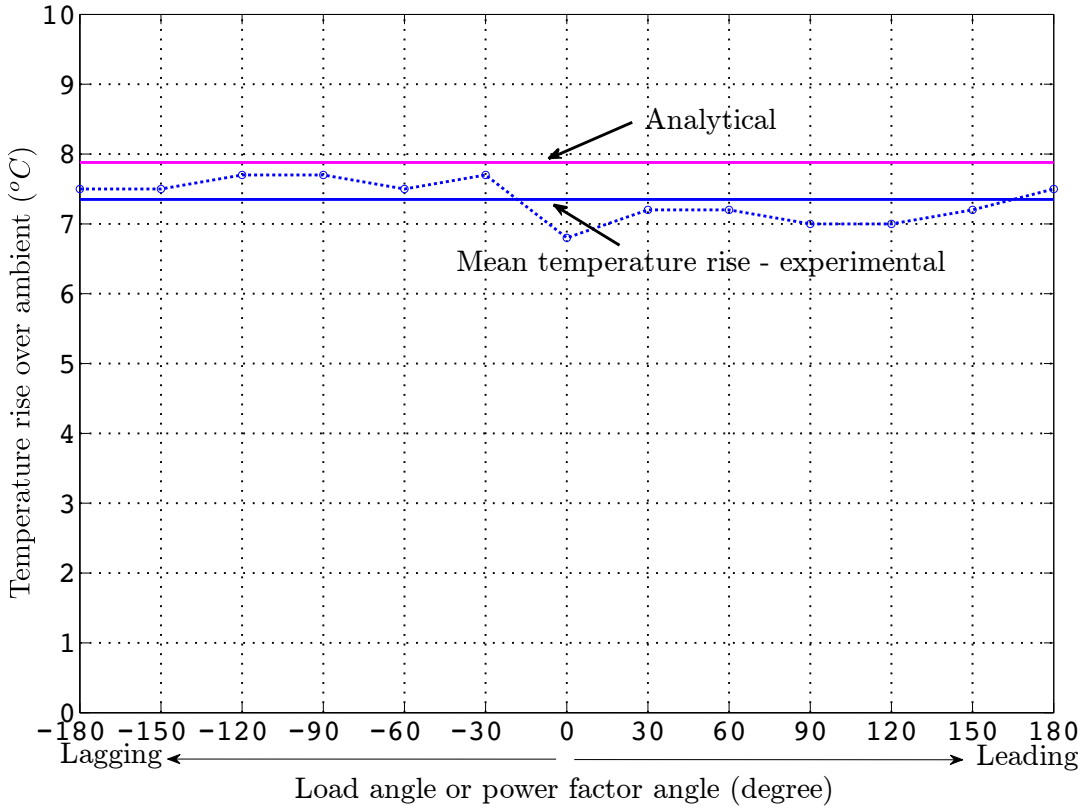


Figure 3.26: Plot of analytical and experimental heatsink temperature rise over ambient for varying ϕ with the three legs of the inverter mounted on the same heatsink and modulated using CSVPWM scheme.

Fig. 3.26 shows the theoretical and experimental temperature rise over ambient for CSVPWM scheme. The experimental result closely matches with the theoretical prediction.

3.9.3 Testing of DC Bus Capacitors

The difference between the 4-wire and 3-wire configurations lies only in the CM currents. The fundamental frequency currents can still be maintained to be three-phase balanced and at the rated value in the 3-wire configuration. But, since the voltages at the output terminals of the test configuration are predominantly CM, the ripple is very low compared to the 3-wire configuration of the actual system. As discussed earlier, the effect of output ripple current on the testing of the dc bus capacitors is negligible. The same limitations explained

in Section 3.8.3 apply for the 3-wire case also. Hence, the dc bus capacitor testing can be done for the 3-wire configuration as it was done for the 4-wire case.

3.9.4 Testing of Output Filter Components

As explained in Section 3.9.3, the ripple is very low in the test configuration as compared to the actual system in a 3-wire configuration. So, for the output filter components, the test configuration emulates the actual system only at the fundamental frequency. The high frequency losses in the output filter cannot be characterized for the 3-wire configuration.

3.10 Summary

In this Chapter a new test method to evaluate the thermal performance of the semiconductor devices of a high-power three-phase grid-connected inverter with output LCL filter is described. The proposed method does not require a high power source or load. The power taken from the grid supplies only the losses in the system under test. Compared to the other power circulation methods available in literature which use another inverter of the same rating, the power consumption is reduced by nearly 50% as the rated currents are circulated within the same inverter in the proposed method. Further, the method can be used for thermal testing of the semiconductor devices in either case of the cooling arrangement being common or independent for the individual semiconductor devices or legs of the inverter. The proposed method has been analyzed in detail for a three-phase 4-wire configuration. The control method of the test configuration has been discussed. The usefulness of the method to test the dc bus capacitors and output filter components has been studied. The procedures for the semiconductor device thermal test, dc bus capacitor testing and output filter components testing have been elaborated and the equivalence of the test methods to the actual system have been shown. The total power loss in the proposed test method is shown to differ from that of the actual system by 0.5% to 1.05% only, for a switching frequency range of 2.5 kHz to 10 kHz. The dc bus capacitor can be tested upto around 70% of its highest expected rms current. For a 3-wire case, the test configuration is seen to emulate the output filter component currents only at the fundamental frequency. The applicability of the method to space vector based PWM techniques has also been shown. Experimental results from the inverter operated at 24 kVA have been used to validate the proposed test approach. This test method has a wide practical applicability in testing of high power inverters.

Chapter 4

Control Performance Evaluation of Grid-Connected Inverters

In recent years, renewable sources integrated to the grid are on the increase. Renewable sources invariably use a grid-connected inverter as an interface to the grid. With the power levels of wind and solar generation units having reached a few MWs, a sudden disconnection of these renewable sources due to short time grid disturbances such as voltage sags and voltage swells can cause instability in the grid. To avoid this, regulations mandate high power wind and solar generation units to have Low Voltage Ride-Through (LVRT) and High Voltage Ride-Through (HVRT) capabilities. LVRT and HVRT capabilities are additional controls implemented in the grid-connected inverters to stay connected to the grid during prescribed depths and durations of voltage sags and voltage swells respectively. To test these capabilities before commissioning, it is required to re-create short time disturbances like voltage sags and voltage swells in the testing laboratory. A hardware grid simulator can be used for this. The present day hardware grid simulators are usually inverters that are controlled to emulate the disturbances usually observed in the grid.

Besides useful for LVRT and HVRT testing, a grid simulator can be used to test any electrical equipment connected to a low voltage grid for its adherence to the EMI standard IEC 61000-4-11 [68]/IEC 61000-4-34 [69]. IEC 61000-4-11/IEC 61000-4-34 gives recommended immunity tests – for equipment connected to the mains – towards voltage dips, short interruptions and voltage variations. Further, the grid simulator can also be used to test the controls of a grid-connected inverter like the current control and dc bus voltage control or the performance of any other equipment connected to the grid under several real-time grid conditions. A 50 kVA inverter has been programmed as a grid simulator to primarily test the control performance of grid-connected inverters under various disturbance conditions.

The developed grid simulator is capable of generating a wide range of disturbance conditions – voltage sags, voltage swells, frequency deviation and phase jumps. This Chapter focuses on the development of a simple yet effective algorithm to generate the different disturbance conditions. The simulator has been experimentally tested with three-phase purely resistive, diode-bridge and inverter loads.

Section 4.1 discusses the various methods available in literature to simulate the disturbances usually observed in the grid. The features of grid simulation products that have recently become commercially available is also discussed. Further, the focus of the present work is detailed. In Section 4.2, the topology of the grid simulator developed to test the control performance of grid-connected inverters is briefed. Section 4.3 outlines the controls used in the front-end converter and the output inverter. Section 4.4 explains the start-up sequence of the grid-simulator inverters and the different modes involved in the generation of a disturbance voltage. The Finite State Machine model for the control algorithm is developed in Section 4.5. Section 4.6 gives the details of the system parameters of the grid simulator and the parameters of the different loads which are used to test the grid simulator's performance. The experimental results appear in Section 4.7. The scope for future work on the grid simulator control to improve stiffness of the grid simulator output voltage is detailed in Section 4.8. Section 4.9 summarises the work done on grid simulator.

4.1 Grid Simulators - A Survey

4.1.1 Grid Simulation Methods Available in Literature

The simulation of grid disturbances in a laboratory environment has been of interest for a long time. However, till a few years back, the interest has primarily been to test for EMI compliance as per the IEC standards IEC 61000-4-11 [68]/IEC 61000-4-34 [69] for electrical equipment connected to the grid. Since the mentioned standards focus primarily on testing of grid connected equipment under voltage sags, most earlier literature have limited their focus to generation of voltage sags. All these earlier works [88, 109–111] mostly use simple passive components [88, 109, 110] to create voltage sags with the exception of [111] which uses a series-injected inverter for the same purpose. While [109] creates the sag by dropping a desired fraction of the grid voltage across an inductor, [88] uses an auto-transformer tap as a means to achieve the same. Both [109] and [88] use power electronic switches. In [109],

the load is attached to the grid through an inductor. A thyristor controlled reactor (TCR) is connected in parallel to the load. Whenever a sag is required, the TCR is switched in a controlled manner so that the current through the inductor increases and creates the sag of required depth and duration. In [88], a power electronic switch is used to switch between taps in the auto-transformer which creates a voltage sag at the output. [110] controls a synchronous generator in closed loop to create a sag. In [111], a sag is created by injecting a voltage in series with the grid using an inverter. The operating principle in [111] is similar to that of a Dynamic Voltage Restorer (DVR) discussed in Section 1.1.1.1. The main drawback of the above methods is that they are limited to creating only sags. Further, except for [111], the other methods use passive components which are bulky, costly and lead to slow dynamic excitation for creating the disturbance voltage.

With the distributed generation gaining pace and their power levels reaching a few MWs, research work on grid simulators have become more generic in recent years [83–88]. The recent literature aims at the generation of swells, unbalance, harmonic voltages and frequency deviations apart from the sags. The requirement of a generic hardware has prompted researchers to use IGBT based inverters. The hardware usually has an active front-end converter that charges the dc bus and an inverter at the output side to generate the required grid disturbances. The decoupled control of the front-end and output inverters together with the bi-directional power flow capability of this topology makes it possible to generate a wide range of grid disturbance conditions in the laboratory. The primary difference in the various methods available in literature [83–88] is the topology used for the output inverter. The front-end converter is a three-phase three-wire inverter in most cases [83–86]. For the output inverter, [83] uses a three-phase 4-wire inverter with mid point dc bus connection while [86,87] use a three-phase four-leg inverter and the rest [84, 85, 88] use a simple three-phase 3-wire inverter. Reference [84] gives extensive experimental results for the developed grid simulator hardware. The other literature discusses experimental results for only sags [83, 88] or provide results only under open circuit condition of the output inverter without connecting any loads [86, 87]. All above methods use already existing standard inverter topologies and inverter control methods for the front-end converter and the output inverter. Hence, they all are capable of producing disturbance conditions with comparable output voltage dynamics.

4.1.2 Commercially Available Grid Simulators

Several manufacturers have recently introduced commercial grid simulator products. Table 4.1 lists and compares the features of some commercially available grid simulators. The primary objective of these systems are to test equipment for compliance to grid-connection standards.

4.1.3 Focus of Work

As in recent literature, the present work also makes use of back-to-back connected inverters sharing a common dc bus to generate grid disturbances. Inverter topologies and control methods having become standard over the years, the work focuses mainly on developing a simple yet effective control algorithm for generating the grid disturbances. A Moore Model based Finite State Machine (FSM) [112] has been used to develop, analyse and implement the algorithm in a digital controller. Using the proposed algorithm, the disturbance generation can be referenced to any of the three phases at any desired phase angle. Further, by adjusting the disturbance duration, the exit phase angle can be set as desired and can be referenced to any of the three phases. The digital control makes it possible to control the point of disturbance very close to the desired phase angle. Also, the algorithm allows the user to repeat the disturbance creation any number of times without restarting the grid simulator, by using a press button switch.

The developed grid simulator is capable of generating voltage sags, voltage swells, frequency deviations and phase jumps. The focus of the work is to develop the grid simulator as a test set-up to evaluate the control performance of grid-connected inverters. So, the experimental studies are directed at testing the grid simulator's capability to produce and maintain the required voltage at its output terminals. Results have been provided to show the various features of the implemented algorithm. The grid simulator has been tested with different loads – a linear purely resistive load, a non-linear three-phase diode bridge load and an inverter load. So, though the grid simulator is primarily built to test grid-connected inverters, loads other than inverters can also be tested.

Parameter/Feature	**Manufacturer**			
	ABB [113] (ACS 6000)	Ametek [114] (MX CTS Series)	Chroma [115] (61800 Series)	Heiden [116] (TC ACS Series)
Year of Manufacture	2012	2013	2013	2012
Rating	3 MVA - 12 MVA	30 kVA - 90 kVA	45 kVA - 60 kVA	50 kVA to 700 kVA
Per Phase Output	As per customer specification	0-300 V	0-300 V	0-280 V
Programmable Faults	sags, swells, frequency variations, unbalance	sags, swells, frequency variations, unbalance, flicker, inter-harmonics	sags, swells, frequency variations, unbalance, flicker, inter-harmonics	sags, swells, frequency variations, unbalance, flicker, inter-harmonics
Supported Standards	Wind generation standards - IEC 61400-21, FERC 661, PRC-024-1 [71,117,118]	IEC 61000 3-2, 3-3, 3-11, 3-12, 4-11, 4-13, 4-14, 4-17, 4-28, 4-29 [67,68,70,119–125]	IEEE 1547, IEC 61000 3-2, 3-3, 3-15, 4-11, 4-34, IEC 62116 [28,67–69,72,119,126]	all IEC grid feed-in standards

Table 4.1: Comparison of features of commercially available grid simulators.

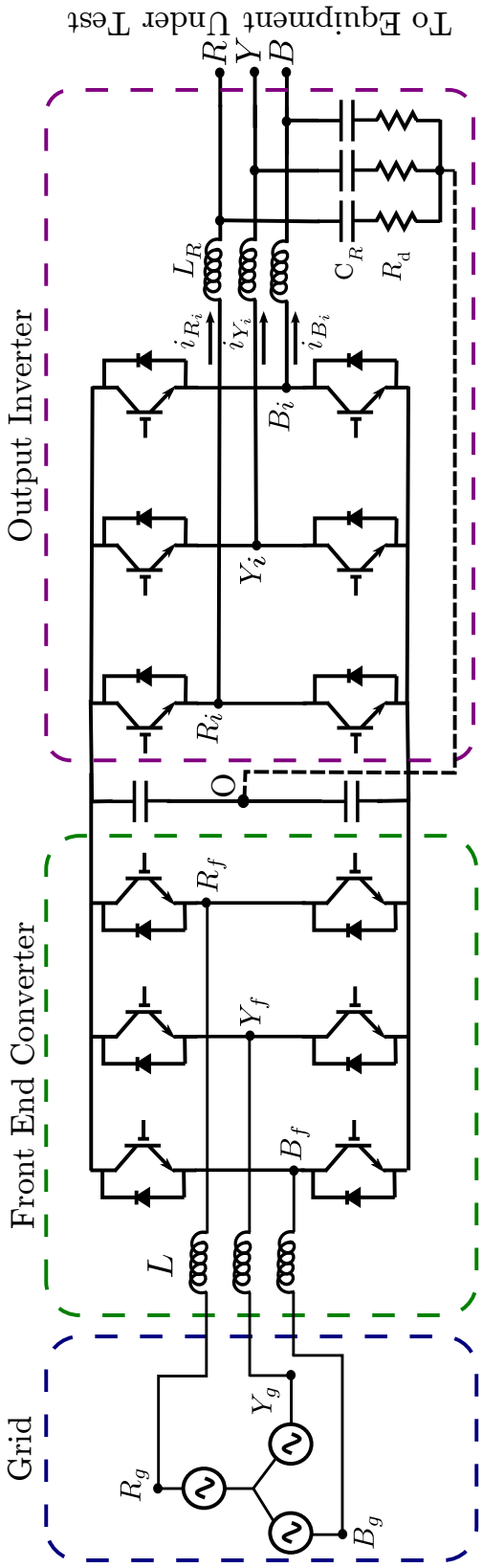


Figure 4.1: Grid Simulator Topology. The front-end converter is a three-phase inverter connected to the grid through an L filter. The output inverter is a three-phase inverter configurable as a 3-wire connection shown in solid lines or as a 4-wire with dc bus mid-point connection shown in dashed lines. A LC filter is used to filter the switching ripple component at the output. Passive resistive damping (R_d) is used to damp the resonance of the LC filter.

4.2 Grid Simulator Topology

Fig. 4.1 shows the topology used in the present work. As shown in the figure, the grid simulator uses an IGBT based back-to-back connected inverter sharing a common dc bus. The front-end uses a three-phase inverter with output L filter to connect to the grid. The front-end converter ensures a fixed voltage at the common dc bus. At the output side, a three-phase inverter with LC filter configurable in a 3-wire or 4-wire topology is used. The output inverter is programmed to generate a wide range of disturbance conditions. The LC filter resonance is damped by passive means through resistors (R_d) connected in series with the output filter capacitors. The front-end converter and the output inverter are both rated at 50 kVA. For the experiments, two legs of the front-end converter are used in a single-phase configuration and hence the input rating is limited to 16.7 kVA.

4.3 Grid Simulator Controls

As explained in Section 4.2, the developed grid simulator has a front-end converter (FEC) and an output inverter. The control of the FEC and the output inverter are decoupled. The FEC tries to maintain a fixed dc bus voltage irrespective of the dynamics of the output inverter. The output inverter uses the fixed dc bus voltage to create the required nominal and disturbance voltages at its load terminals. Section 4.3.1 and Section 4.3.2 explain the controls used for the FEC and output inverter respectively.

4.3.1 Front-End Converter Control

As explained in Section 4.2, the FEC is a single-phase grid-connected inverter with L filter. The FEC locks to the grid using a Synchronous Reference Frame based Phase-Locked Loop (SRF-PLL) [127]. The SRF-PLL requires transformation of the input grid voltage from the stationary reference frame to the synchronous rotating d-q frame. The Second Order Generalised Integrator (SOGI) [128] is used to convert the single phase input grid voltage into orthogonal components to be used for dq transformation. Fig. 4.2 shows the SRF-PLL.

Once locked to the grid, the FEC uses an inner current control loop to draw near unity power factor current from the grid. An outer dc bus voltage control loop maintains the dc bus at the required reference voltage. The current loop uses a proportional-resonant

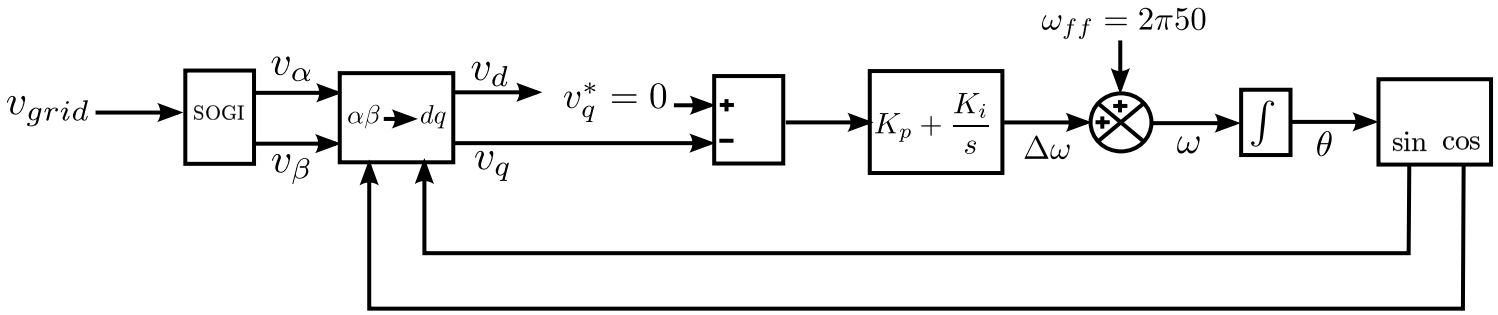
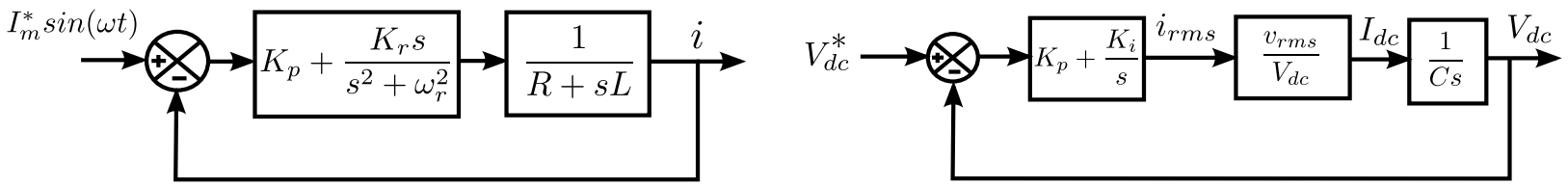


Figure 4.2: Synchronous Reference Frame Phase Locked Loop (SRF-PLL) for single-phase FEC. The Second Order Generalized Integrator (SOGI) has been used in the generation of orthogonal components. References [128] and [127] discuss the SOGI and SRF-PLL respectively.



(a) (b)

Figure 4.3: FEC Controls. The parameters used for control are listed in Table. 4.2. (a) Inner current loop structure. PR controller is used. It acts directly on the ac current reference. L, R are the filter inductance and the resistance associated with the filter. $\omega_r = 2.\pi.50$ (b) Outer voltage loop structure. PI controller is used. v_{rms} is the rms grid voltage.

PLL Control		**Current Control**		**Voltage Control**	
Parameter	**Value**	**Parameter**	**Value**	**Parameter**	**Value**
K_p	0.775 rad/V-s	K_p	125.6 V/A	K_p	0.334 A/V
K_i	1.801 rad/V-s^2	K_r	2543.7 V/A-s	K_i	0.050 A/V-s

Table 4.2: FEC Control Parameters.

(PR) controller in the stationary reference frame for its control. The voltage loop uses a proportional-integral (PI) controller. Fig. 4.3 shows the inner current control and outer voltage control loops. The FEC uses sine-triangle modulation at a switching frequency of 10kHz.

Table. 4.2 lists the various control parameters used for the SRF-PLL, current and voltage control loops.

4.3.2 Output Inverter Control

The output inverter is controlled as an open loop voltage source. The pulse-width modulation signals are generated from the three-phase nominal and disturbance voltage references using sine-triangle modulation at a switching frequency of 10kHz. The disturbance voltage references are generated using the voltage disturbance generation algorithm explained in Section 4.5.

4.4 Grid Simulator Operation

A proper start-up sequence is required to ensure that the grid simulator reaches a steady operating state smoothly. The disturbance generation at the output inverter also requires a well-defined sequence of operation. Section 4.4.1 and Section 4.4.2 explain the sequence of operation of the grid simulator and the different modes involved in the generation of voltage disturbance.

4.4.1 Start-Up Sequence of Grid Simulator

The following is the start-up sequence of operation of the grid simulator once the input power is switched on:

1. The anti-parallel diodes in the FEC act as a diode bridge rectifier and charge the dc bus capacitor towards voltage V_1. V_1 corresponds to the diode bridge output voltage. A resistor is connected in series with the filter inductor L when the dc bus starts to charge. A contactor shorts out the resistor when the dc bus voltage is close to V_1. This ensures that the there are no current spikes due to sudden charging of dc bus capacitor. The current control, dc bus voltage control and the output inverter controls are not activated during this period. The gate pulses to both the inverters are withheld through software.

2. When the anti-parallel diodes are charging the dc bus capacitor, the PLL control starts and locks the inverter to the grid frequency and phase.

3. Once the dc bus is charged to V_1, a toggle switch is used to start the current and voltage loops of the FEC. The toggle switch action can be automated. The output inverter controls still remain deactivated. The FEC controls boost the voltage from V_1 to the set reference voltage, V_{dc}^*.

4. Once the dc bus voltage stabilises at V_{dc}^*, the output inverter control is activated using a press button switch. This slowly ramps up the voltage at the ac terminals of the output inverter to the nominal value. This ensures that there are no current spikes or oscillations due to sudden charging of the output LC filter.

4.4.2 Modes during Disturbance Generation

Fig. 4.4 shows the different modes involved in the disturbance voltage generation at the ac terminals of the output inverter including the start-up voltage ramp-up. The voltage magnitude versus time plot has been drawn assuming the disturbance is a voltage sag. However, the different modes shown are equally applicable to the other types of disturbances also. The different modes are as follows:

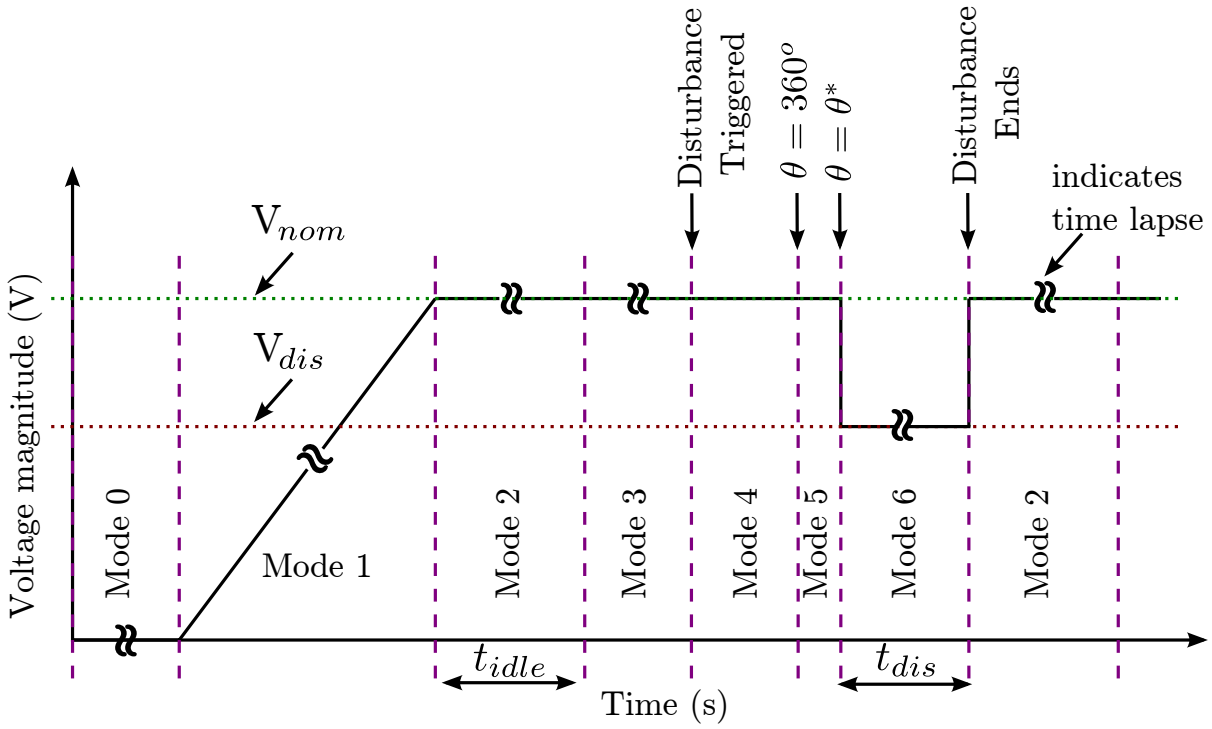


Figure 4.4: Grid Simulator modes during voltage disturbance generation. t_{idle} is the duration of idle state between successive disturbances, t_{dis} is the time duration of the voltage disturbance. V_{nom}, V_{dis} indicate the nominal and disturbance voltage magnitudes.

Mode 0: No output voltage

During this mode, the input power to the grid simulator has been switched on and the grid simulator is going through its start-up sequence to boost the dc bus voltage to the set reference, V_{dc}^*. The grid simulator output voltage is withheld during this mode as explained in Section 4.4.1.

Mode 1: Voltage ramp-up

This mode is entered by activating a press button switch after ensuring that the dc bus voltage has stabilised at V_{dc}^*. On pressing the switch, the output voltage of the grid simulator ramps up slowly to the nominal value. The ramp up time is programmable.

Mode 2: Wait state between disturbances

This mode is entered once the output voltage is ramped up to the nominal value. The

grid simulator enters into a wait state for a set interval of time. During the wait state, the disturbance event cannot be triggered. The grid simulator has been programmed to re-create a disturbance any number of times to allow the user to repeat the test to study different control behaviour of the equipment under test without having to restart the grid simulator. Since the same press button switch is used to create the disturbance several times, a wait time is provided between successive disturbances so as to avoid false triggers.

Mode 3: Ready state

This mode is entered once the wait time between successive faults elapse. The output voltage remains at the nominal value. The grid simulator is ready to service any disturbance trigger input. The ready state is exited on triggering a disturbance using the press button switch.

Mode 4: Wait state for end of current cycle of reference phase

This mode is entered on receiving the trigger to start the disturbance. The algorithm waits for the end of the current cycle of the reference phase so that the disturbance can be started at the required phase angle in the new cycle. The output ac voltage is at its nominal value during this mode.

Mode 5: Wait state for desired phase angle in new cycle

This mode is entered on the completion of the current cycle of the reference phase after the disturbance is triggered using the press button switch. The algorithm monitors the phase angle of the reference phase during this mode. The mode ends when the desired phase angle, θ^* is reached. The output ac voltage is at its nominal value during this mode.

Mode 6: Disturbance state

This mode is entered on the phase angle of the reference phase reaching the desired value. The disturbance voltage appears at the output ac terminals during this mode. The three phase disturbance voltage magnitude, frequency and starting phase are programmable. Magnitude setting helps create a sag, swell or unbalance, frequency deviations are created by adjusting the frequency setting, starting phase can be used to create phase jumps. A combination of different settings can help create a wide range of disturbance conditions. The duration of this mode is programmable. By adjusting the duration of the disturbance, the

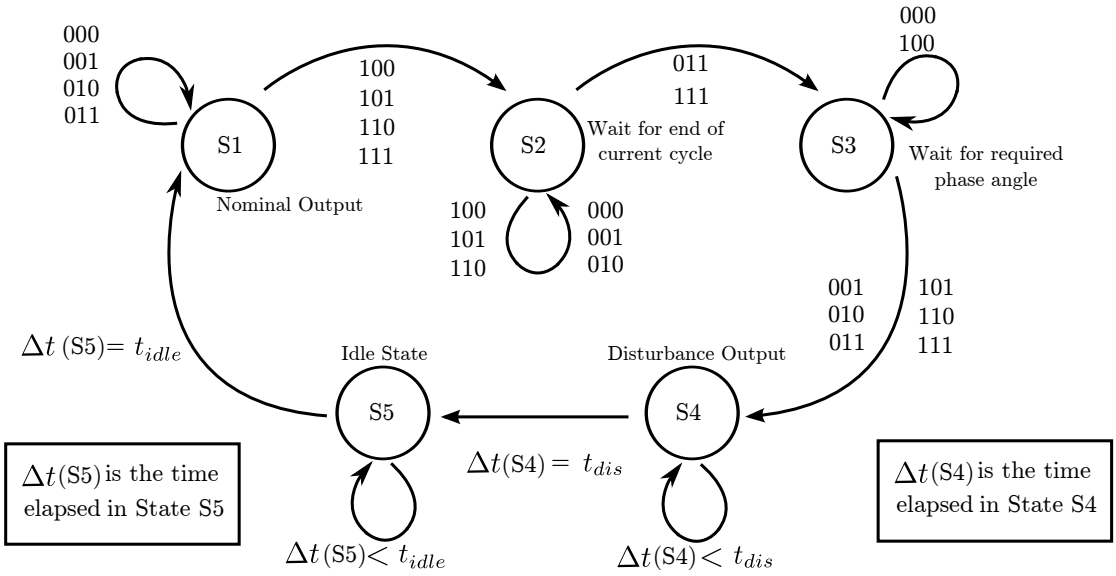


Figure 4.5: Moore model based finite state machine for the voltage disturbance generation algorithm. The FSM assumes that the voltage disturbance has already been referenced to a chosen phase. The FSM is the same for any referenced phase. Only the combination 'BC' in Table. 4.4 varies with the referenced phase. In the figure, combinations 000 to 111 indicate the value of 'ABC'.

user can choose to reference the disturbance exit to the required phase angle of any desired phase. At the end of this mode, the ac output voltage returns to the nominal value. The initial phase angle after exit of the disturbance is programmable. This helps set any end point of fault conditions.

4.5 Voltage Disturbance Generation Algorithm

Fig. 4.5 shows the Moore Model based Finite State Machine (FSM) [112] of the voltage disturbance generation algorithm for a chosen reference phase. In a FSM, 'states' describe 'events'. Different 'inputs' act as 'triggers' and cause control to be transferred from one state to another. The control transfer is called a 'transition'. The different states involved in the disturbance generation algorithm are listed in Table 4.3 and the various input triggers are listed in Table. 4.4. The FSM conveys the same idea as Fig. 4.4 but brings better clarity into implementation of the algorithm. The use of input triggers ensures that the algorithm

State	Description	Corresponding Mode
State 1 (S1)	Grid simulator output voltage is at its nominal value and awaits a disturbance trigger input.	Mode 3
State 2 (S2)	Grid simulator waits for the current cycle of the reference phase to end ($\theta = 360^o$).	Mode 4
State 3 (S3)	Grid simulator waits for the desired phase angle ($\theta = \theta^*$) to be reached for the reference phase.	Mode 5
State 4 (S4)	Disturbance voltage is created at the output.	Mode 6
State 5 (S5)	Grid simulator is idle. No disturbance can be triggered.	Mode 2

Table 4.3: Description of States of the FSM

Press Button Switch Status	
Combination (A)	**Status**
0	The press button switch has not been pressed
1	The press button switch has been pressed
Phase angle of reference phase	
Combination (BC)	**Status**
00	$0^o < \theta < \theta^*$
01	$\theta = \theta^*$
10	$\theta^* < \theta < 360^o$
11	$\theta \geq 360^o$
Time duration of disturbance	
t_{dis}	Indicates the duration of disturbance.
Time duration of idle state	
t_{idle}	Indicates the duration of idle state between successive disturbances.

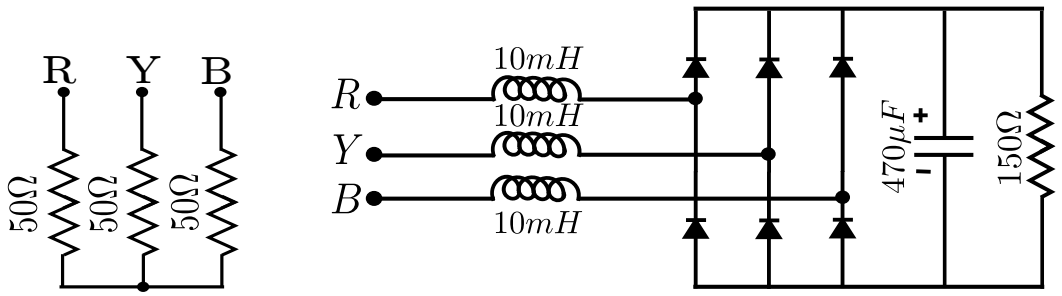
Table 4.4: Trigger Inputs

is tested for all possible combination of triggers, thus avoiding any mal-operation due to unexpected input conditions. The FSM can be understood by comparing the different states with Modes 2 to 6 discussed in Section 4.4. The modes corresponding to the different states are listed in Table 4.3. The FSM has been drawn assuming a reference phase to have been chosen already. For different selections of reference phase, only the phase angle used for generating trigger combinations 'BC' will change.

4.6 Grid Simulator Parameters and Test Loads

The grid simulator hardware is rated at 50kVA. Though the grid simulator is rated at 50kVA, it is expected to be used to test loads upto 10kVA only. The high margin is given to ensure that the grid simulator works effectively even under unexpected fault conditions of the connected load during testing. Further, the experiments have been conducted at a lower power level. For the experiments, the dc bus voltage is set to 500 V. The switching frequency is 10 kHz for both the FEC and the output inverter. The nominal output voltage per phase is 120V rms and the fundamental frequency is 50Hz. The filter inductor value for the FEC is 20mH. The output inverter LC filter values are 5mH and 3μF. A 2Ω resistance is connected in series with the LC filter capacitors to damp the LC resonance.

Fig. 4.6 and Fig. 4.7 show the linear purely resistive load, non-linear diode bridge load and current-controlled inverter load used as test loads in the experimental studies. The values of the various components used in the loads have been indicated in the figures. In the diode bridge load, the inductors are used to smoothen the input currents and the output capacitor is used to maintain a steady dc bus voltage. The inverter load is controlled as a grid-connected STATCOM using current control implemented in the synchronous reference (dq) frame [2]. The STATCOM uses a Synchronous Reference Frame Phase Locked Loop (SRF-PLL) [127] to lock to the grid simulator's output frequency and phase. The convention used for the STATCOM considers d-axis to be aligned along the voltage vector and q-axis to be lagging the d-axis by 90^o i.e. a current along d-axis would indicate real current and a current along q-axis would indicate a reactive current. The SRF-PLL generates a cos unit vector along the d-axis and a sin unit vector along the q-axis for use in the current control. As per the conventions used for the STATCOM, cos unit vector is in-phase with the R-phase grid voltage and sin unit vector lags R-phase grid voltage by 90^o.



(a) (b)

Figure 4.6: Three-phase 3-wire loads used for experimental testing of the grid simulator. (a) A linear purely resistive load. (b) A non-linear diode-bridge load.

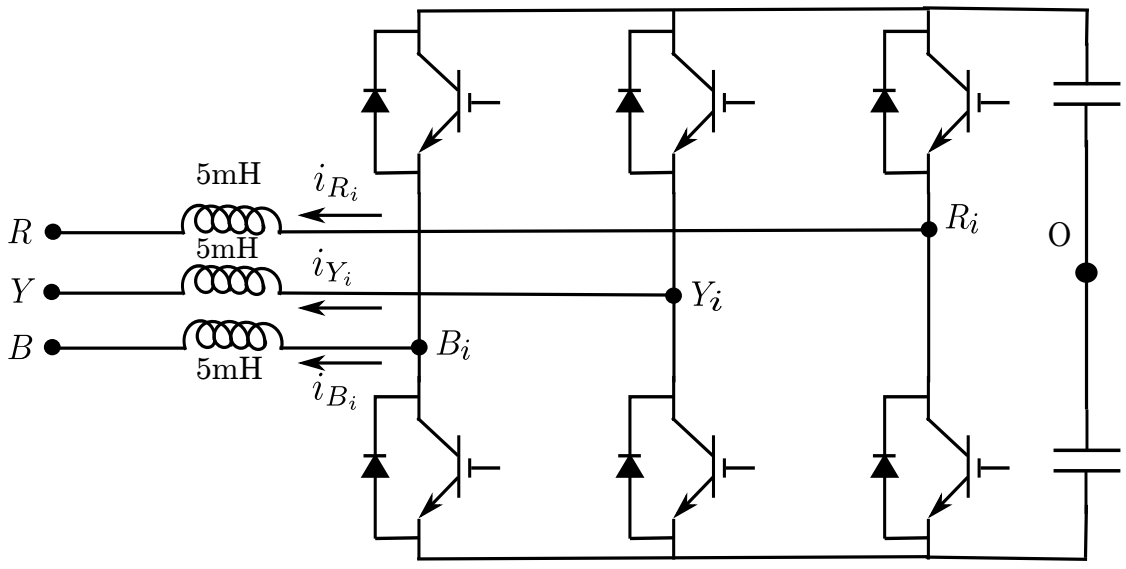


Figure 4.7: A three-phase 3-wire inverter load used for experimental testing of the grid simulator. The inverter is programmed as a current controlled STATCOM. The inverter is rated for 10kVA and switches at 10kHz.

4.7 Experimental Results

4.7.1 Modes of Operation of Grid Simulator

Fig. 4.8 and Fig. 4.9 show the different modes in the voltage disturbance generation as discussed in Section 4.4.2. Fig. 4.8 shows mode 0 and mode 1. There is no output voltage from the grid simulator in mode 0. The voltage ramps up in mode 1. The slow ramping up of voltage helps avoid capacitor current spikes at the output LC filter. Fig. 4.9(a) and Fig. 4.9(b) show modes 2 to 6 for a 50% voltage sag of 5 cycles. The sag is referenced to R-phase at an angle of 30^o. In all the figures in this Section, the trigger status indicates the point at which the disturbance is triggered and serviced. The trigger status goes from LOW to HIGH when the disturbance is triggered using a press button switch. The trigger status goes from HIGH to LOW when the disturbance is serviced i.e. when disturbance period starts at the desired phase angle of the referenced phase.

4.7.2 Sag, Swell and Frequency Deviation

Fig. 4.10 shows DSP references for different types of faults. Voltage sag, voltage swell and frequency deviation have been shown. An example of a phase jump is shown in Section 4.7.3.3.

4.7.3 Load Testing

The grid simulator has been tested with linear, non-linear and inverter loads. The experimental results from the various tests are discussed in this Section.

4.7.3.1 Linear Purely Resistive Load

Fig. 4.11 shows the response of a linear purely resistive load to a 50% voltage sag created by the grid simulator. The load current can be observed to immediately fall by 50% as expected during the sag.

4.7.3.2 Non-Linear Diode-Bridge Load

Fig. 4.12 shows the response of a non-linear diode bridge load to a 50% voltage sag created by the grid simulator. The load current can be observed to become zero on entering the disturbance condition. Since the input voltage dips, for a few cycles the input current

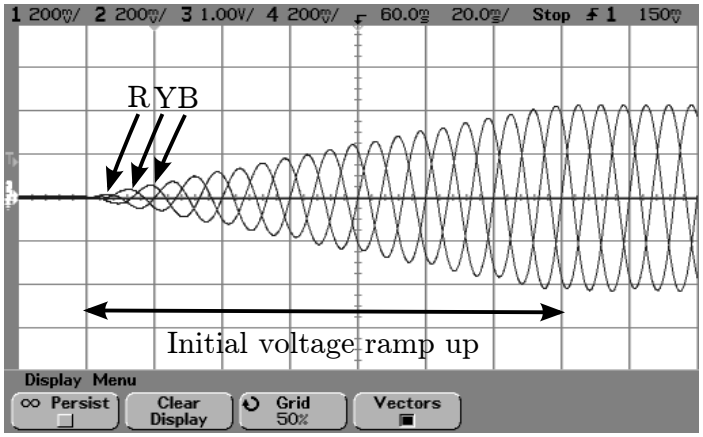
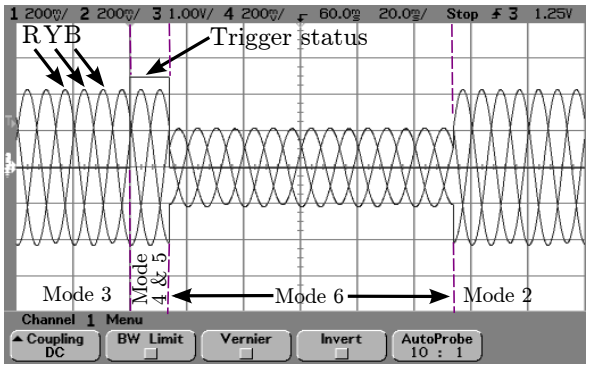
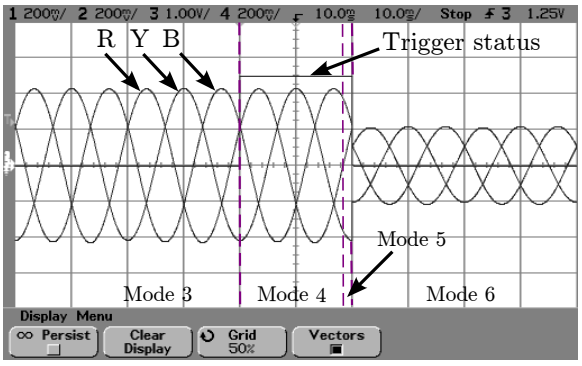


Figure 4.8: Three-phase voltage references from the DSP during initial voltage ramp-up. The ramp up time is programmed to 0.14s. The experimental ramp up time matches closely with the programmed time. Ch1, Ch2, Ch4: R,Y,B phase voltage references. Magnitude scale for Ch1, Ch2, Ch4: 80V/div, Time scale: 20ms/div.



(a)



(b)

Figure 4.9: Three-phase voltage references from the DSP for a 50% voltage sag for 5 cycles. The voltage sag is referenced to R-phase at an angle of 30^o. Ch1, Ch2, Ch4: R,Y,B phase voltage references, scaling is 80V/div. Ch3 indicates the trigger status. (a) A complete sag disturbance cycle. Time scale: 20ms/div. (b) Enlarged view of a sag occurring at 30^o of R-phase. Time scale: 10ms/div.

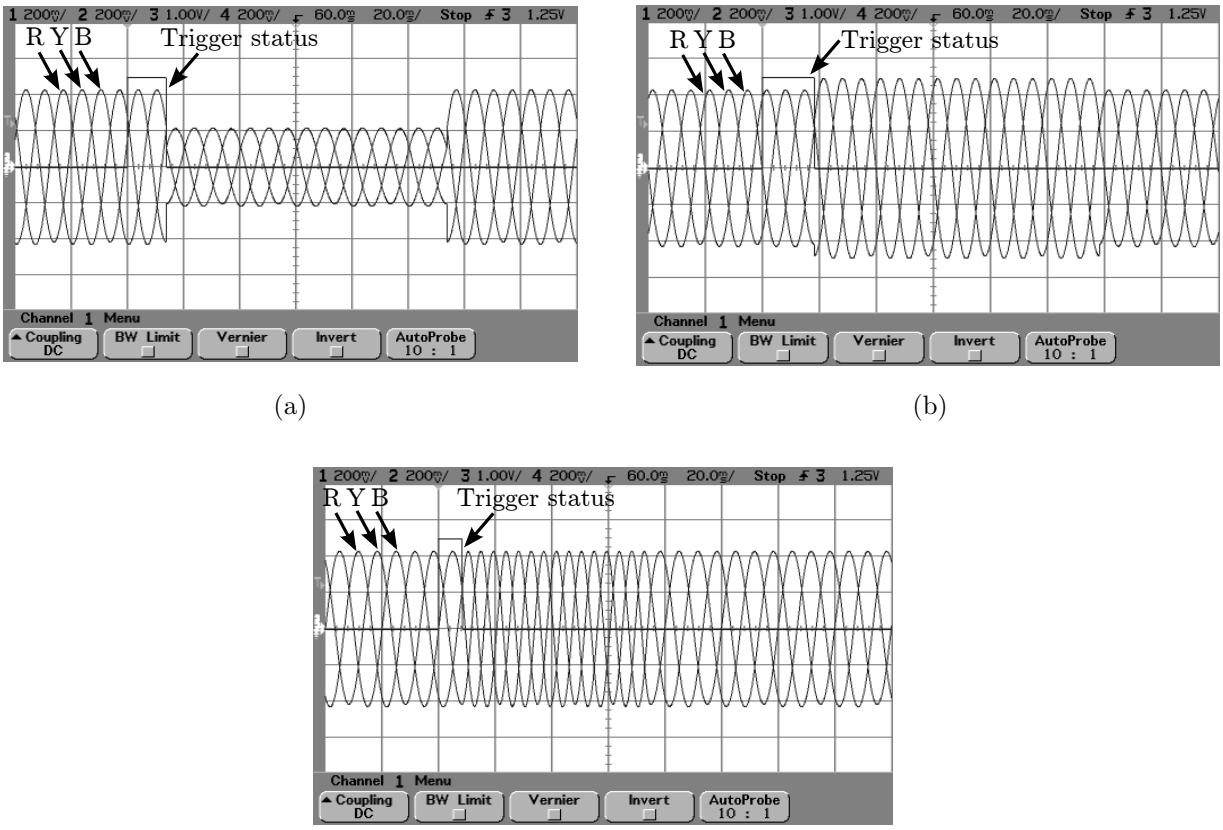
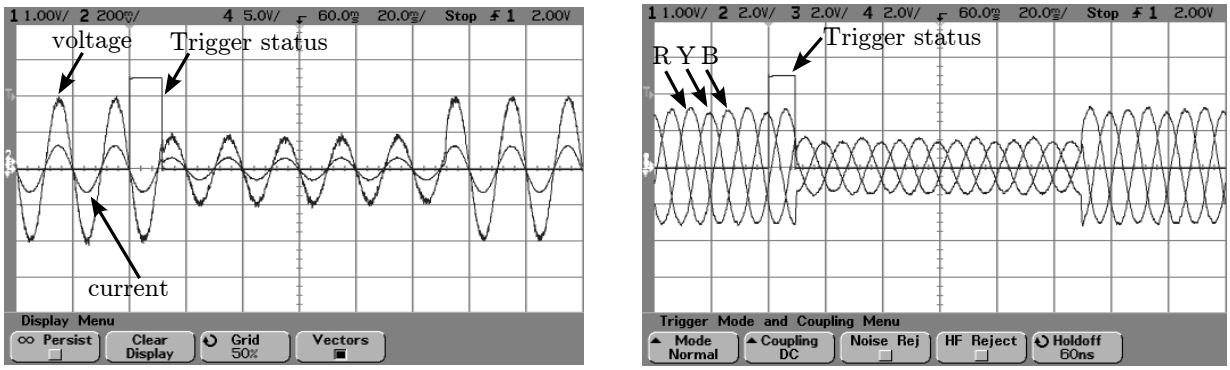
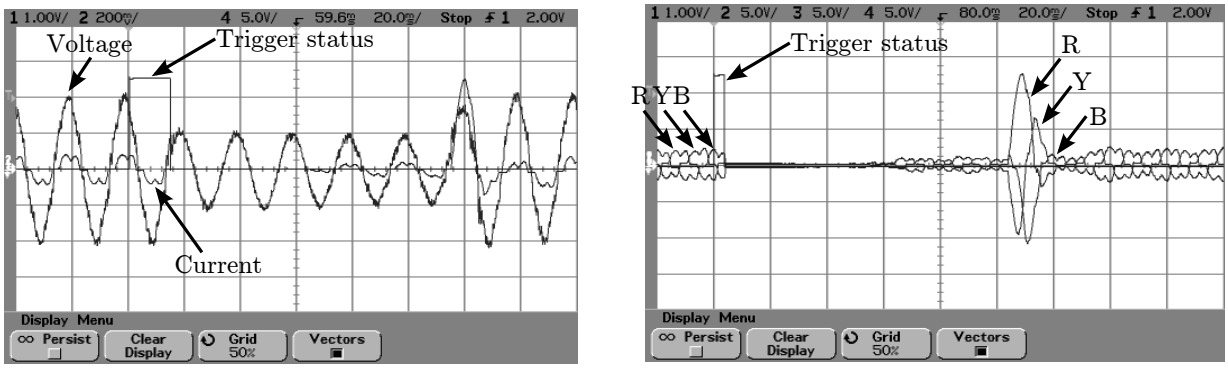


Figure 4.10: Three-phase voltage references from the DSP for different types of disturbance voltages. The disturbances are referenced to R-phase at an angle of 30^o. Ch1, Ch2, Ch4: R,Y,B phase voltage references, scaling is 80V/div. Time scale: 20ms/div. Ch3 indicates the trigger status. (a) A 50% voltage sag for 5 fundamental cycles (b) A 15% voltage swell for 5 fundamental cycles (c) Frequency deviation from 50 Hz to 75 Hz for 5 disturbance frequency cycles. The frequency deviation has been set to a higher value for visibility. It can be set to values closely around 50 Hz also.



(a) (b)

Figure 4.11: Response of a linear purely resistive load shown in Fig. 4.6(a) to a 50% voltage sag for 5 fundamental cycles. The sag has been referenced to 30^o of R-phase. (a) R-phase voltage and current. Ch1: Trigger status, Ch2: R phase voltage 80V/div, Ch4: R phase current 5A/div, Time scale: 20ms/div. (b) Three phase currents. Ch1: Trigger status, Ch2, Ch3, Ch4: R, Y and B phase currents 2A/div. Time scale: 20ms/div.



(a) (b)

Figure 4.12: Response of a non-linear diode-bridge load shown in Fig. 4.6(b) to a 50% voltage sag for 5 fundamental cycles. The sag has been referenced to 30^o of R-phase. (a) R-phase voltage and current. Ch1: Trigger status, Ch2: R phase voltage 80V/div, Ch4: R phase current 5A/div, Time scale: 20ms/div. (b) Three phase currents from the grid simulator. Ch1: Trigger status, Ch2, Ch3, Ch4: R, Y and B phase currents 5A/div. Time scale: 20ms/div.

becomes zero. The output electrolytic capacitor supplies the load current during this period. Similarly, at the exit of the disturbance, the phase currents have a surge due to sudden increase in the input voltage. The output electrolytic capacitor draws a peaky current during this period due to sudden increase in the input voltage.

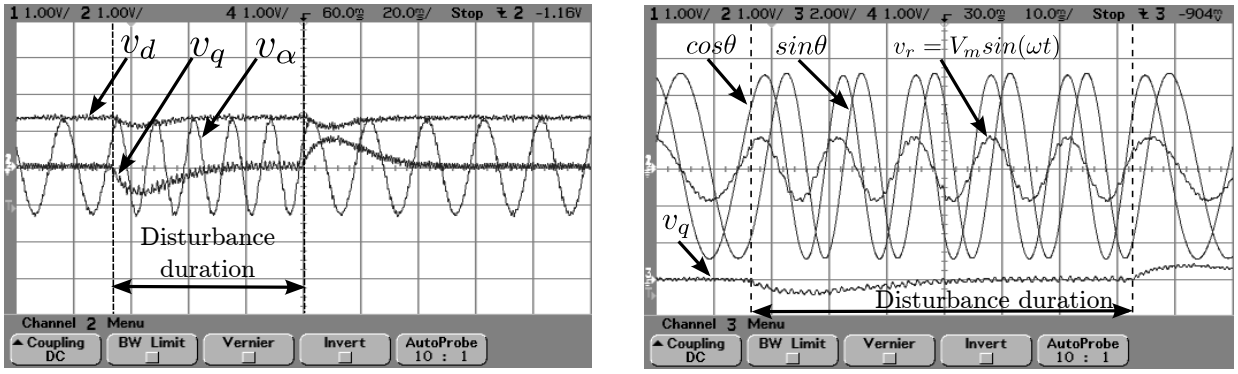
4.7.3.3 Current Controlled Inverter Load

In this Section experimental results of the response of the various controls of a inverter programmed as a STATCOM is discussed. The topology of the STATCOM is shown in Fig. 4.7. The experimental results demonstrate the usefulness of the grid simulator to test grid-connected inverters for their control performance under grid-disturbance conditions.

Control Performance of PLL Fig. 4.13 shows the response of PLL control of a inverter load controlled as a STATCOM as described in Section 4.6 to a change in frequency from 50Hz to 75Hz for 5 cycles of the disturbance frequency. The disturbance is referenced to R-phase at a phase angle of 30^o. The frequency change has been set to a higher value to clearly observe the dynamics of the PLL control. As observed from Fig. 4.13(a), the PLL control ensures that v_d follows the peak of v_α and v_q follows zero. The control response time is around the expected design value of 0.055s. Fig. 4.13(b) shows the cos unit vector, which goes out of synchronism at the occurrence of the fault, locking back to the R-phase grid voltage due to PLL control action.

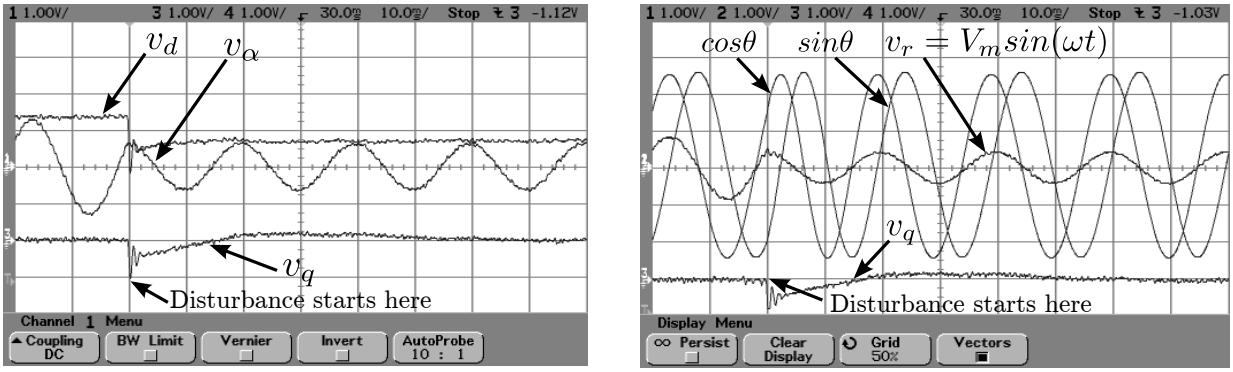
Fig. 4.14 shows the response of the PLL control to a voltage sag with phase jump. The sag disturbance is referenced to R-phase at an angle of 30^o. At the beginning of the disturbance, the phase jumps from 30^o to 90^o. Fig. 4.14(a), the PLL control ensures that v_d follows the peak of v_α and v_q follows zero and Fig. 4.14(b) shows the cos unit vector locking to the R-phase grid voltage due to PLL control action.

Control Performance of Current Control Fig. 4.15 shows the response of the q-axis or reactive current controller to a step change in current reference. The step change in current reference is from zero to 8.5 A. This corresponds to a per phase current step from zero to 4A. i_q can be observed to track i_q^* within half a fundamental cycle. The q-axis current controller output has also been shown. It can be observed that the controller output is saturated initially. This shows that the current controller's bandwidth is limited by the



(a) (b)

Figure 4.13: (a) The PLL control ensures that v_d tracks the peak of v_α and v_q tracks zero. Ch1, Ch2, Ch4: v_d, v_q, v_α. Ch1, Ch2, Ch4: 200 V/div, Time scale: 20ms/div. (b) The cos unit vector can be observed to get locked to the R-phase grid voltage due to the action of the PLL control. Ch1, Ch2, Ch3, Ch4: sin unit vector, cos unit vector, v_q and v_r. Ch3: 400 V/div, Ch4: 200 V/div, Time scale: 20ms/div.



(a) (b)

Figure 4.14: (a) The PLL control ensures that v_d tracks the peak of v_α and v_q tracks zero. Ch1, Ch3, Ch4: v_d, v_q, v_α. Ch1, Ch3, Ch4: 200 V/div, Time scale: 10ms/div. (b) The cos unit vector can be observed to get locked to the R-phase grid voltage due to the action of the PLL control. Ch1, Ch2, Ch3, Ch4: sin unit vector, cos unit vector, v_q and v_r. Ch3, Ch4: 200 V/div, Time scale: 10ms/div.

voltage available for control. The dc bus voltage sets an upper limit on the voltage available for control.

Control Performance of DC Bus Voltage Control Fig. 4.16 shows the response of the dc bus voltage controller to a step change in dc bus voltage reference. The waveform captures the voltage boost action of the STATCOM. An initial dc bus voltage exists due to three-phase diode bridge rectification of the three-phase ac input. The voltage is boosted to the set reference of 500V through boost action of the STATCOM. The d-axis current is also shown in the figure. Initially the d-axis current is high and saturated. This indicates that the STATCOM is absorbing real power to boost the dc bus voltage to 500V. Once the dc bus voltage reaches 500V, the d-axis current becomes small as only the losses in the system needs to be absorbed from the grid.

STATCOM Response to Sag, Swell and Phase Jump Fig. 4.17 shows the R-phase reference voltage and the R-phase reactive current from the STATCOM under a voltage sag of 20%, 40% and 70%. The STATCOM control can be observed to be effective under the mentioned sag conditions.

Fig. 4.18 shows the operation of the STATCOM under a voltage swell of 15%.

Fig. 4.19 shows the operation of the STATCOM under a 20% voltage sag with a phase jump from 30^o to 90^o on entering the disturbance and from 90^o to 30^o on exiting the disturbance. The reactive current can be observed to deviate from its set reference when the phase jump occurs but it starts tracking again within 2 cycles.

The experimental results have been provided for balanced disturbances only, as the intention is to highlight the capabilities of the developed algorithm. However, the experimental set-up can be used to test unbalanced disturbance conditions also, with changes to the front-end converter control. Unbalanced output voltages result in unbalanced output currents, which lead to imbalance in the top and bottom dc bus voltages. Further, second harmonic voltages would be observed in the dc bus. A three-phase four-wire front-end with appropriate controls can handle this. The mid-point of the dc bus is available in the hardware and hence, it is possible to convert into such a topology. Only control changes are required to generate and test unbalance disturbance voltage conditions. However, the algorithm developed for disturbance voltage generation still remains the same.

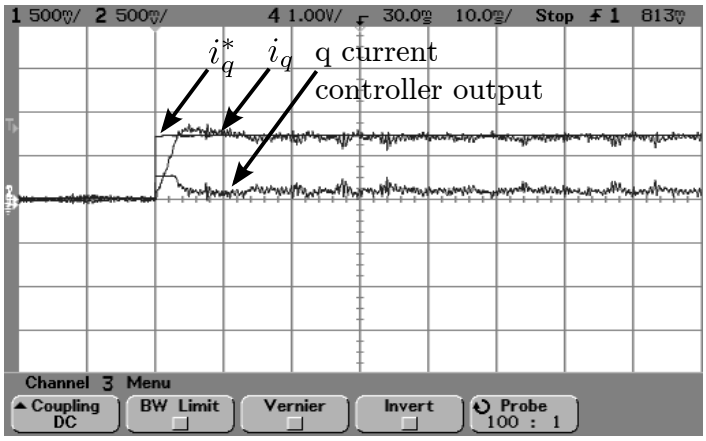


Figure 4.15: Step response of q-axis current controller. The controller output has also been shown. Ch1, Ch2, Ch4: i_q^*, i_q and q-axis current controller output. Magnitude scale for Ch1, Ch2: 6A/div, Ch4: 200V/div, Time scale: 10ms/div.

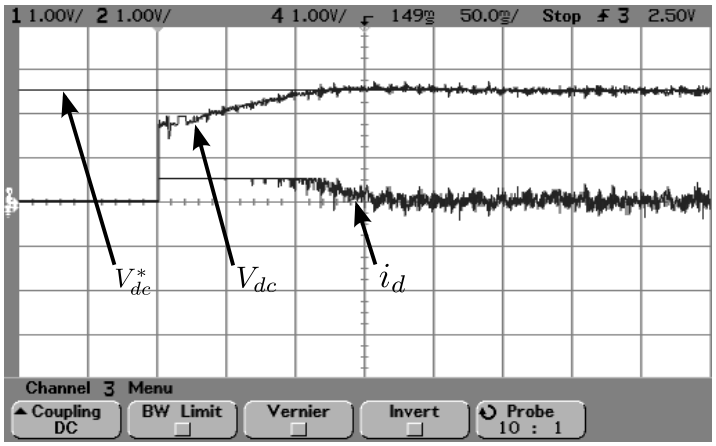
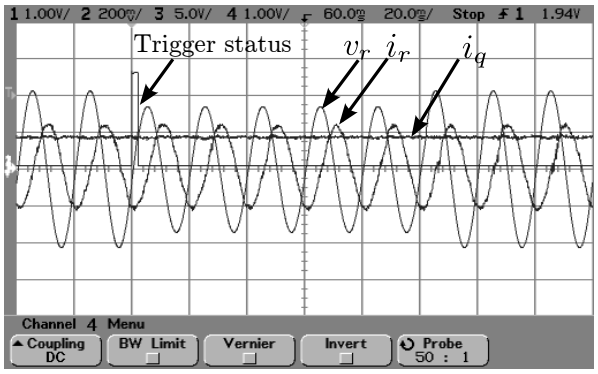
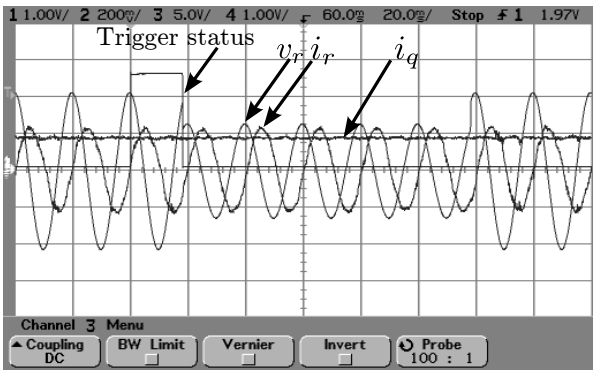


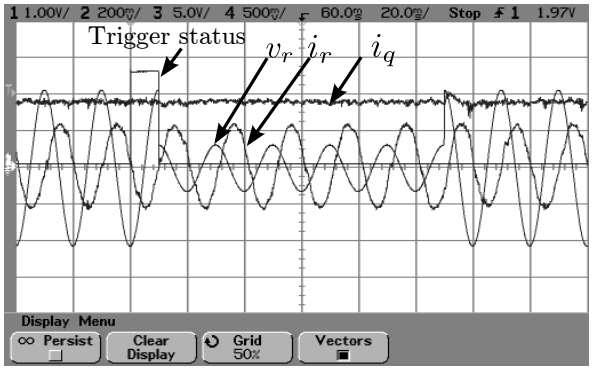
Figure 4.16: Step response of dc bus voltage controller. The d-axis current has also been shown. The d-axis current is high when the dc bus voltage is being boosted. Once the set reference voltage is reached, the d-axis current falls down to a small value as only the losses in the system needs to be supplied thereafter. The reactive current reference during the same time is set to 4A/phase. Ch1, Ch2, Ch4: V_{dc}^*, V_{dc} and i_d. Magnitude scale for Ch1, Ch2: 200 V/div, Ch4: 12A/div, Time scale: 50ms/div.



(a)



(b)



(c)

Figure 4.17: STATCOM operation under voltage sag. The reactive current reference has been set to 4A/phase or $i_q^* = 8.5A$. Ch1, Ch2, Ch3, Ch4: Trigger status, R-phase reference voltage, R-phase current from the STATCOM to the grid simulator, i_q of STATCOM. The STATCOM control can be seen to be effective under voltage sag. Time scale: 20ms/div. (a) A 20% sag for 5 cycles referenced to 30^o of R-phase. Magnitude scale for Ch2: 80V/div, Ch3: 5A/div, Ch4: 12A/div. (b) A 40% sag for 5 cycles referenced to 60^o of R-phase. Magnitude scale for Ch2: 80V/div, Ch3: 5A/div, Ch4: 12A/div. (c) A 70% sag for 5 cycles referenced to 90^o of R-phase.Magnitude scale for Ch2: 80V/div, Ch3: 5A/div, Ch4: 6A/div.

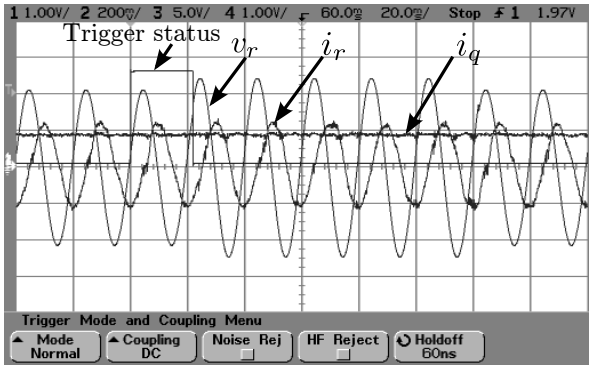


Figure 4.18: STATCOM operation under a voltage swell of 15% for 5 cycles referenced to 45^o of R-phase. The reactive current reference has been set to 4A/phase or $i_q^* = 8.5A$. Ch1, Ch2, Ch3, Ch4: Trigger status, R-phase reference voltage, R-phase current from the STATCOM to the grid simulator, i_q of STATCOM. Ch2: 80V/div, Ch3: 5A/div, Ch4: 12A/div. Time scale: 20ms/div. The STATCOM control can be seen to be effective under voltage swell.

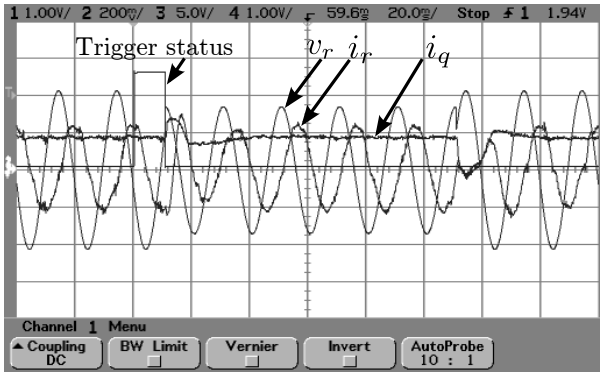


Figure 4.19: STATCOM operation under a 20% voltage sag with phase jump. The sag is for 5 cycles and referenced to 30^o of R-phase. The phase jumps from 30^o to 90^o on entering the disturbance and from 90^o to 30^o on exiting the disturbance. The reactive current reference has been set to 4A/phase or $i_q^* = 8.5A$. Ch1, Ch2, Ch3, Ch4: Trigger status, R-phase reference voltage, R-phase current from the STATCOM to the grid simulator, i_q of STATCOM. Ch2: 80V/div, Ch3: 5A/div, Ch4: 12A/div. Time scale: 20ms/div. The STATCOM control can be seen to be effective under the phase jump.

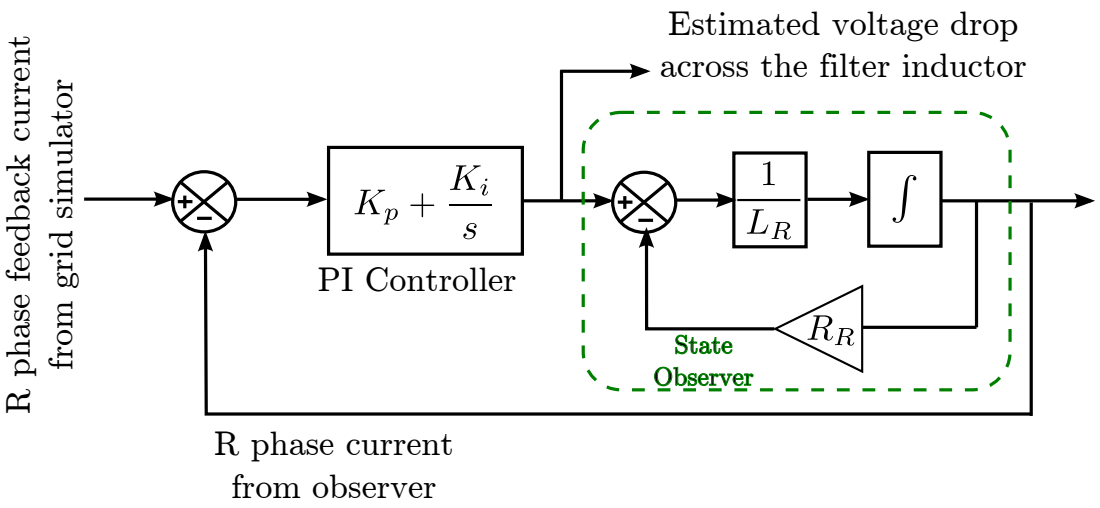


Figure 4.20: Fundamental frequency current control based on state observer to improve the output voltage of the grid simulator. The controller has been shown for the R phase. The control is similar for the other phases. L_R and R_R are the output filter inductance and associated resistance for the R phase output of the grid simulator. The estimated voltage drop across the filter inductor is to be added to the open loop voltage reference.

4.8 Future Scope of Work

The focus of the present work has mainly been on the development, analysis and implementation of the voltage disturbance generation algorithm. The output inverter is controlled as a open loop voltage source. The open loop control ensures the desired output ac voltage to be produced at the inverter output terminals. However, depending on the nature and magnitude of the output three-phase currents, the ac voltage seen by the load at the output LC filter capacitor will have deviations from the set reference. The voltage drop in the output filter inductor leads to magnitude variations, phase angle variations and distortions in the output capacitor voltage.

To create a stiff output ac voltage across the LC filter capacitor, a feedback control using the output filter inductor current can be implemented. A possible state observer based current feedback scheme using Proportional-Integral (PI) controller is shown in Fig. 4.20. The control compensates for the inductor drop at fundamental frequency by re-creating

the expected drop in the filter inductor using a state observer implemented in the digital controller.

Alternatively, the current control shown in Fig. 4.20 can also compensate specific harmonic voltage drops in the filter inductor by using a multi-resonant PR controller. Then the controller transfer function would be,

$$\text{Controller transfer function} = K_p + \sum_{n=1,5,7,\ldots} \frac{K_{rn}s}{s^2 + (2.\pi.50.n)^2} \tag{92}$$

For further improving the stiffness of the grid simulator output voltage, an outer voltage loop can be used in addition to the current loop. The outer voltage loop will act directly on the error in the filter capacitor voltage. The accuracy of the inner current loop depends on the exactness of the inductance and associated resistance values used in the observer. The outer loop corrects any errors due to deviation of the filter component values from their measured values.

4.9 Summary

A 50kVA back-to-back connected inverter is programmed as a grid simulator. A novel voltage disturbance generation algorithm has been proposed for the grid simulator. The proposed algorithm has been developed, analysed and implemented in digital control using a Moore model based finite state machine. The developed grid simulator can reference the start of the disturbance to any phase at any desired phase angle. By adjusting the duration of the disturbance, the exit phase angle can be set with reference to any desired phase. The magnitude, phase angle and frequency of the grid simulator output voltage during the nominal and disturbance durations are programmable. The magnitude setting helps create voltage sags and swells, the frequency setting helps create frequency deviations and phase jumps can be created by setting the desired phase angle at the entry and exit of the disturbance condition. A combination of the different settings help create a wide range of disturbance conditions. The proposed algorithm has been validated using experimental studies on different loads – a linear purely resistive load, a non-linear diode bridge load and a current controlled inverter load. The developed grid simulator is useful in evaluating the control performance of grid-connected inverters and any other equipment connected to the grid.

Chapter 5

Conclusion

Grid-connected inverters have found wide application as power quality converters and as interface between renewable sources and the grid. As more of these converters are put to use and as their power levels increase, research on grid-connected inverters has gained importance. The focus of researchers has been to improve the performance of these converters and to make them more reliable. Also, the increasing connection of switching converters to the grid has led to newer issues related to stability and voltage quality in the grid. Several standards such as the IEEE Standard 519-1992 [65], IEEE Standard 1547-2003 [28] and the various IEC standards for grid-connection like [67–69, 119] have been introduced to ensure that the stability and voltage quality in the grid are not compromised. The need for compliance to these grid standards have opened up more avenues for research in this field. This thesis has proposed design methods and performance evaluation methods that are useful for compliance with emerging grid performance requirements. A 50 kVA back-to-back connected inverter has been built to experimentally validate the theoretical predictions. The following Sections highlight the various contributions of the thesis.

5.1 LCL Filter Damping Design

Stringent regulations on harmonic currents that can be injected into the grid require the use of third order LCL filters in grid-connected inverters. The use of LCL filters lead to resonance. Resonance can be damped through active or passive means. Passive damping is simple and more reliable. Various passive damping topologies have been suggested in literature. But, the choice of passive damping components of the topologies have not been done systematically. In the present work, a comparative analysis of the losses in a few

passive topologies available in literature has been done. Based on the comparison, the SC-RL method is chosen as a suitable passive damping topology for high power grid-connected inverters and a component selection method for the same has been developed. The proposed method aims at reducing the losses in the damping resistor while keeping the system well damped. A component by component optimization and trade-off procedure is used to achieve this. With the proposed method, the power loss in the damping resistor is in the range of 0.05% to 0.1% while the quality factor is in the range of 2.0 to 2.5. The proposed method also ensures that the additional poles introduced by the passive damping network too are well damped. Further, the method has been shown to be applicable for a wide range of practical switching frequencies. The power loss and quality factor have been verified experimentally to be within the expected range.

5.2 Thermal Testing

For better reliability, burn-in tests are performed on grid-connected inverters. Burn-in tests are run continuously for long durations of time to allow the temperatures to stabilise. So, at high power levels, burn-in tests consume lot of power. To ensure energy savings, regenerative methods are usually adopted at high power levels. Also, it is not practical to have sources and loads of high power in the testing laboratory. In this thesis, a novel method that draws only the losses in the test configuration has been proposed and the controls required for the same have been developed. The proposed method overcomes the shortcomings in the existing methods. Existing methods in literature either use two inverters or require the individual legs of the inverter to have independent cooling arrangement. The proposed method does not have these limitations. Also, since the method circulates high currents within the test inverter itself, it consumes less power than existing methods. A complete analysis of the proposed method has been presented for both cases of a three-phase 3-wire configuration and a three-phase 4-wire configuration. Further, the usefulness of the proposed method to test the other passive components associated with the inverter like the dc bus capacitors and output filter components has been studied. Experimental tests show a close match with theoretical predictions.

5.3 Grid Simulator

High power grid-connected inverters are required to have controls that ensure their operation even under short time grid disturbances like voltage sag, voltage swells, frequency deviations and phase jumps. A grid simulator is a hardware that can create a wide variety of grid disturbances in a controlled manner in a laboratory environment to test the grid-connected inverters for their control performance under these disturbance conditions. There are several literature on grid simulators all of which focus mainly on the converter topology. In this thesis, a back-to-back connected inverter is programmed as a grid simulator. The focus of the work has been on the development of a novel disturbance voltage generation algorithm with simple yet powerful features, for the grid simulator. The algorithm has been developed, analysed and implemented in a digital controller using finite state machine model. The algorithm has the flexibility to reference start of the disturbance generation to any phase at any desired phase angle. Further, by adjusting the duration of the disturbance, the end of the disturbance generation can be set to the desired phase angle of any phase. The control of the start and end disturbance conditions help in studies of grid transient events with precise details and to observe the response of the various control loops of a grid-connected inverter to such events. The proposed algorithm also allows the precise conditions of the test to be repeated. Further, it is possible to set the magnitude, phase and frequency of the three phases at the start and end of the disturbance cycle. By adjusting the magnitude, voltage sags and voltage swells can be created, by adjusting the phase angle phase jumps can be simulated and deviations in grid frequency can be generated using the frequency parameter. Also, a wide range of grid disturbances can be simulated through different combinations of the mentioned parameters. The grid simulator has been experimentally tested with a linear purely resistive load, a non-linear diode-bridge load and a current controlled STATCOM load.

5.4 Scope for Further Work

In the proposed thermal test method, a more detailed analysis and experimental validation can be made for the testing of dc bus capacitors and output filter components. In the grid simulator, the front-end converter control can be modified to handle top and bottom dc bus voltage imbalance and to mitigate second harmonic voltages in the dc bus. This

would help use the system to create and test unbalanced grid disturbance voltage conditions and unbalanced loads. Further, a closed loop control for the output inverter would ensure that the grid simulator acts as a stiff voltage source that generates the required disturbance voltage irrespective of the load current.

5.5 Summary

Design and performance evaluation of sub-systems of grid-connected inverters has been researched in this thesis. LCL filter passive damping design, a test method for thermal performance evaluation and a test system for control performance evaluation are the chosen aspects of study. Detailed study of available literature in each of the mentioned areas has been done and significant incremental contributions has been made in each of the chosen aspects. Firstly, a method of component selection procedure that reduces the losses in the damping resistor while keeping the system well damped has been proposed. Then, a new method for thermal testing of grid-connected inverters has been proposed. Finally, a test system to study the control performance of grid-connected inverters has been developed. The proposed methods have been verified experimentally on a back-to-back connected custom-built inverter. The contributions have direct industrial application to improve the efficiency and reliability of grid-connected inverters.

Appendix A

Details of Experimental Set-Up

A three-phase 50kVA back-to-back inverter sharing a common dc bus has been fabricated in-house for experimental validation of the work. One of the inverters connect to the grid and act as a Front-End-Converter (FEC) to charge the dc bus to the required voltage. The other converter is used as an output inverter.

A.1 Hardware Specifications

Table A.1 shows the specifications of the developed hardware.

Parameter	**FEC**	**Output Inverter**
Rated three-phase power	50kVA	50kVA
Rated voltage/phase	240V	240V
Rated current	70A	70A
Fundamental Frequency	50Hz	50Hz
DC bus voltage	800V	800V
Device used	SKM150GB12T4G	SKM150GB12T4G
Switching frequency	10kHz	10kHz
Cooling	Forced-air	Forced-air

Table A.1: Hardware Specifications.

For all the experiments, the front-end is operated as a single-phase using two legs of the inverter. So, the input power is limited to 16.7kW. For experiments discussed in Chapter 2, the dc bus is set to 400V and the tests are performed at an output voltage of 100V/phase and a current of 40A/phase i.e. at a three phase output power of 12kVA. For experiments in Chapter 3, the dc bus is set to 800V and the output voltage, current and three-phase power are 200V/phase, 40A/phase and 24kVA respectively. The experiments in Chapter 2 and Chapter 3 are run in current circulation method discussed in Chapter 3 and hence do not require high power to be drawn from the front-end connected to the grid. For experiments in Chapter 4, the dc bus is set to 500V and the output voltage is set to 120V/phase. The output current varies with the load.

A.2 Details of Digital Controller

Following are the details of the digital controller used. A common digital controller board is used to control the two inverters.

Processor: Texas Instrument's TMS320F2812
Clock Frequency: 150MHz
Coding: Assembly language
Analog to digital converter (ADC) Used: Internal ADC of TMS320F2812
ADC Sampling Frequency: 20kHz
Computation Frequency: 20kHz

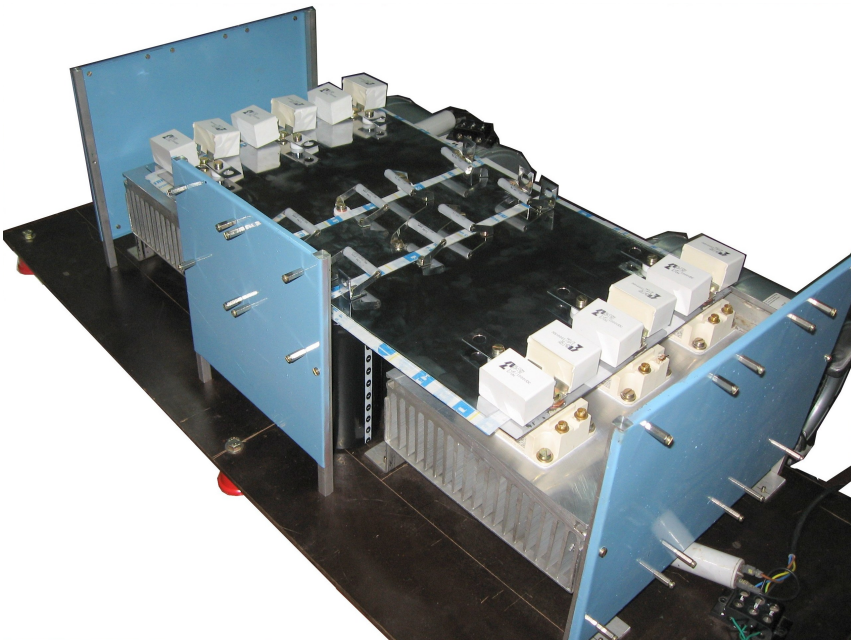
A.3 Experimental Set-Up

Fig. A.1 shows the back-to-back inverter during assembly. Fig. A.1(a) shows the heatsink and dc bus capacitor arrangement. Fig. A.1(b) shows the set-up after the busbars, snubber capacitors and balancing resistors have been assembled.

Fig. A.2(a) shows the set-up along with the filter. The filter is shown in close-up view in Fig. A.2(b). The SC-RL damping components can be viewed in the close-up view. The output filter capacitance is made out of two parallel capacitors and to one of the capacitors a parallel combination of a damping resistor and a damping inductor is connected in series.

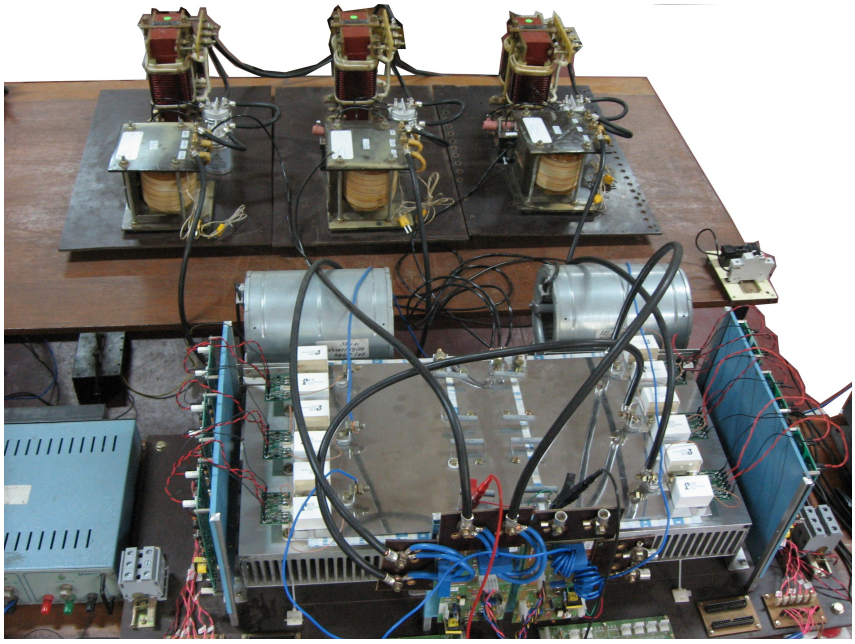
A cabinet has been built to house the back-to-back inverter and the output filter. Fig. A.3(a) shows the outer structure of the cabinet. Fig. A.3(b) shows the inverter set-up mounted vertically inside the cabinet. Fig. A.4 shows the digital signal processing board used for control.

(a)

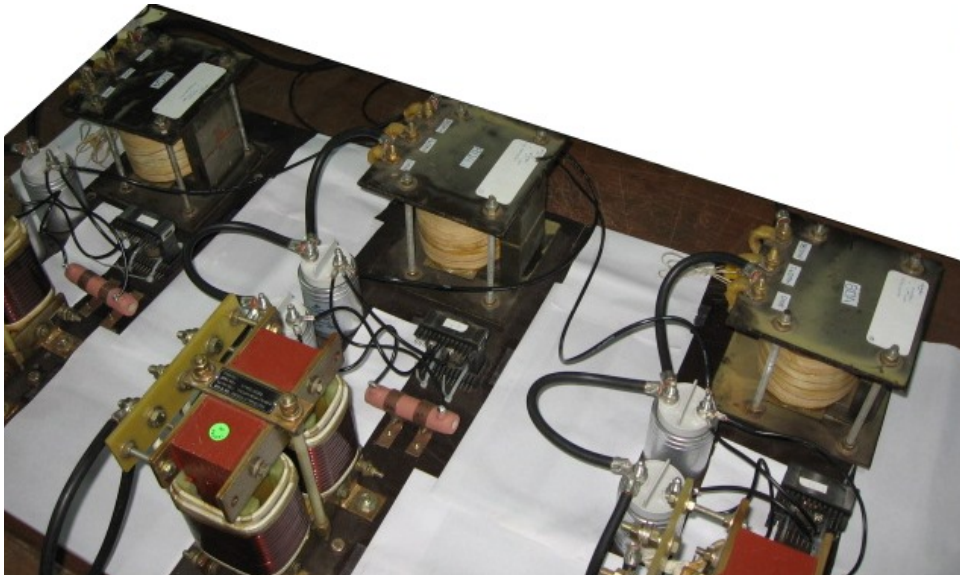


(b)

Figure A.1: 50 kVA back-to-back connected inverter during assembly. (a) Heatsink and dc bus capacitor arrangement (b) Assembled inverter with busbars, snubbers and balancing resistors.



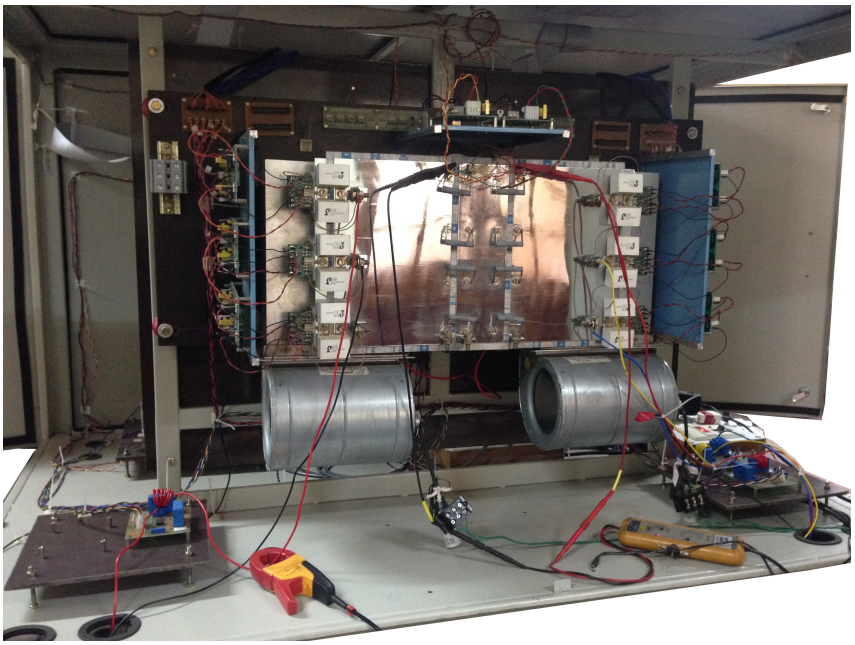
(a)



(b)

Figure A.2: 50 kVA back-to-back connected inverter with output LCL filter. (a) Completely assembled back-to-back inverter with gate drive boards, sensing boards and output LCL filter. (b) Close up view of output LCL filter showing split-capacitor resistive-inductive (SC-RL) passive damping components.

(a)



(b)

Figure A.3: Cabinet that houses the 50 kVA back-to-back inverter and the output filters. (a) Cabinet outer structure. (b) Back-to-back inverter mounted vertically inside the cabinet.

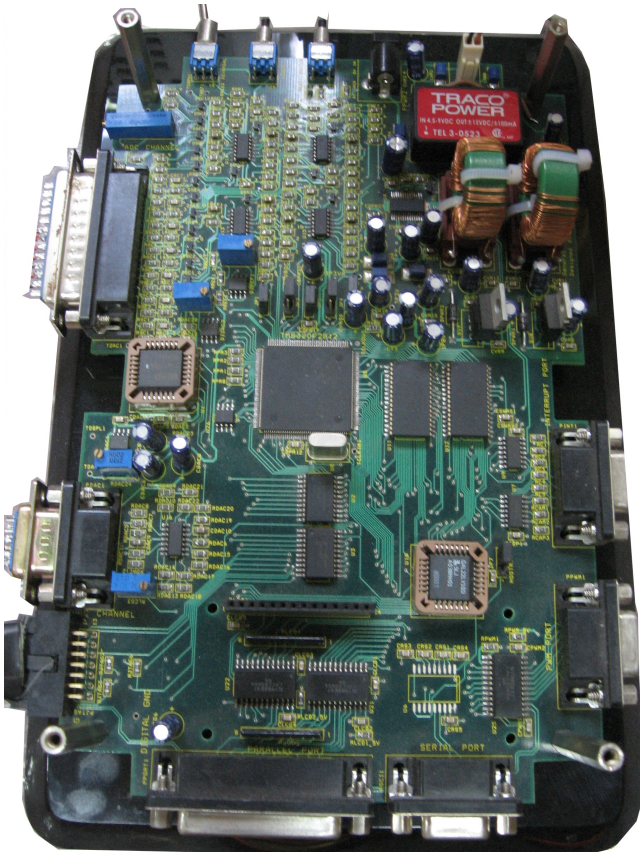


Figure A.4: TMS320F2812 digital signal processor board used to control the back-to-back connected inverters.

Appendix B

Harmonic Limits: Terminology, Definitions and Test Method

To use the current harmonic limits recommended by IEEE Standard 519–1992 [65] and IEEE Standard 1547–2003 [28], a clear understanding of the various terminology and definitions used by these standards is essential. In this Appendix, some terminology, definitions and test method related to the use of the current harmonic limits recommended by the mentioned IEEE standards is elaborated.

B.1 Point of Common Coupling (PCC)

IEEE standards define the harmonic limits at the PCC. Hence, a clear definition of PCC is essential. Fig. B.1 shows the PCC. PCC is the point at which the local electric power system is connected to the area electric power system [28]. In other words, it is the closest point on the utility side of the consumer's service where another utility consumer can potentially be supplied [129]. To get a better idea, "Consumer 3" in Fig. B.1 can be thought of as say, an educational institute which has some loads and a distributed source like solar energy generation system both of which are connected to the PCC through a common transformer. The electrical network within the educational institute can be considered as a local electric power system. The area electric power system is the common feeder that supplies power from the grid to a region in the city. The area electric power system would be supplying power to different consumers in that region (Consumer 1 to Consumer 4 in this case). As shown for "Consumer 3", PCC need not be the point at which a distributed source is connected to the power system through a grid-connected inverter. However, the harmonic limits are defined to be met by the grid-connected inverter at the PCC rather than at the point of interconnection

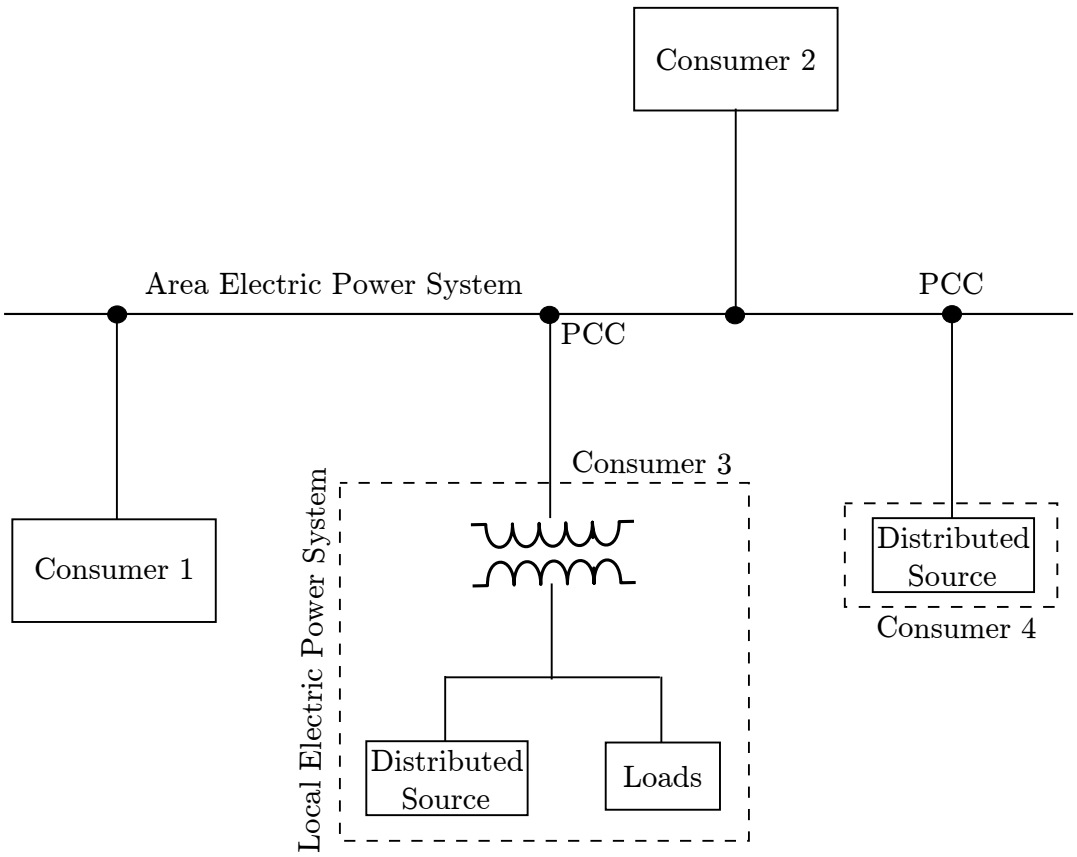


Figure B.1: Point of Common Coupling.

in the system as PCC is the point of common connectivity with other consumers. In the figure, "Consumer 4" can be thought of as a wind farm in the neighbourhood of the institute that is connected directly to the area electric power system. In this case the PCC happens to be the point at which the distributed source is connected to the power system through a grid-connected inverter.

B.2 Harmonic Measures

Harmonic content can be measured using different parameters. Each parameter has a specific use. As can be seen in Table 2.1, the IEEE standards use the TDD to define harmonic current limits. This Section gives the definition and use of different parameters.

B.2.1 Total Harmonic Distortion (THD)

The total harmonic distortion is the ratio of the total rms value due to all the voltage/current harmonic components to the rms value of the fundamental component of voltage/current. For example, the voltage THD is given by,

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_{fu}} \tag{93}$$

Where,
V_h = rms value of h^{th} harmonic component of voltage (V)
V_{fu} = rms value of fundamental component of voltage (V)

THD is generally not used to define the harmonic current limits at the PCC because under lightly loaded conditions, the THD will be high even though the actual harmonics injected is very less. This is due to the fact that the fundamental component of current will be less under lightly loaded condition. So, if THD is used to specify the harmonic limits, a consumer might be penalised wrongly. However, THD serves as a useful specification for voltage harmonics at the PCC as the nominal fundamental voltage does not vary with loading.

B.2.2 Total Demand Distortion (TDD)

The total demand distortion is the ratio of the total rms value due to all the current harmonic components to the rms value of highest fundamental demand current (15 or 30 minute demand). The fundamental demand current is the fundamental rms current averaged over an interval of 15 or 30 minutes. The current TDD is given by,

$$TDD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_D} \tag{94}$$

Where,

I_h = rms value of h^{th} harmonic component of current (A)
I_D = rms value of highest fundamental demand current (15 or 30 minute demand) (A)

The highest fundamental demand current is arrived at by monitoring the fundamental demand current for a considerable duration of time under peak load conditions. Thus, the TDD will be low under lightly loaded condition. Using TDD as a measure of harmonic content will make sure that the consumer is not penalised wrongly under any load condition. This makes TDD a suitable choice for harmonic current monitoring at the PCC.

B.2.3 Total Rated current Distortion (TRD)

The total rated current distortion is the ratio of the total rms value due to all the current harmonic components to the rms value of the fundamental rated current of the equipment or unit under study. The TRD is given by,

$$TRD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_R} \tag{95}$$

Where,
I_h = rms value of h^{th} harmonic component of current (A)
I_R = rms value of fundamental rated current of the equipment or unit under study (A)

The equipment or unit under study is tested for adherence to harmonic standards before putting it to use in the local electric power system. The test would typically be done by the manufacturer at his place. TDD cannot be used as it is applicable only at the PCC. So, assuming that every load or source connected to the local electric power system is allowed to inject harmonics equally in terms of p.u values, the equipment or unit can be tested for conformance to standards by using its rated fundamental current in the place of highest fundamental demand current. In other words, TRD can be used in the place of TDD. The TRD measurement will either be equal to or be conservative as compared to TDD.

B.3 Design Test for Conformance to Harmonic Standards

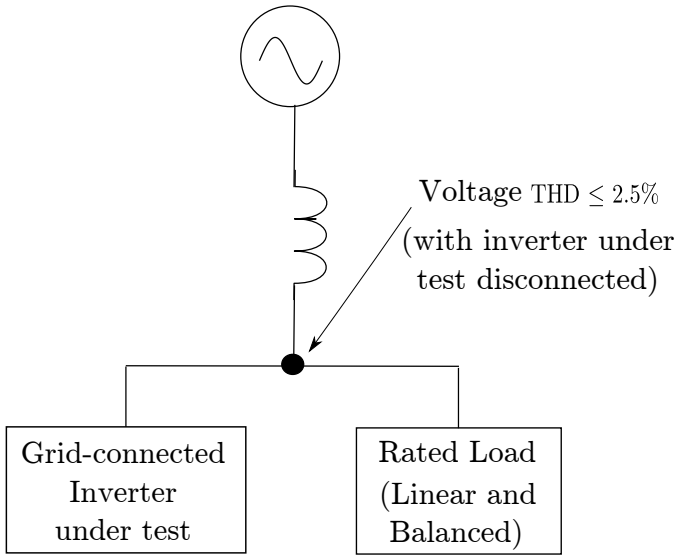


Figure B.2: Design test set-up.

It might not always be possible to do the harmonic conformance test at the site. IEEE Standard 1547–2003 [28] suggests a design test method to check for adherence to harmonic limits at the PCC. The test method uses TRD measurements instead of TDD and can be performed at the laboratory or manufacturing site. As TDD is always less than or equal to TRD, the method is conservative.

The test is performed by operating the grid-connected inverter under test in parallel to a predominantly inductive voltage source with voltage THD not exceeding 2.5% when the grid-connected inverter is disconnected (Fig. B.2). A linear, balanced load is used and the inverter is operated at power levels as close as possible to the rated current. This set-up emulates the connection of a distributed source directly to the PCC and feeding linear balanced loads. The measured TRD is expected to be within the limits specified in Table 2.1.

Appendix C

Quality factor in the context of LCL filter design

Quality Factor (QF) is a terminology used in resonant circuits to quantify resonance behaviour. Though the basic idea of resonance and the definition of QF remains the same for grid-connected inverters with output LCL filter, the context is different from that of resonant converters. In resonant converters, the power circuit operates around the resonance frequency whereas in grid-connected inverters, the resonance occurs due to non-idealities in the power circuit and is not desired. This Appendix tries to clarify the use of quality factor in the context of LCL filter design.

By general definition [91],

$$QF = 2\pi \frac{\text{Total energy stored in the reactive components}}{\text{Energy dissipated per cycle}} \tag{96}$$

The QF is usually computed at the resonance frequency.

C.1 Quality factor in second-order series RLC circuits

Let us consider the series RLC circuit shown in Fig. C.1.

Let,

$$v_c(t) = V_m sin(\omega t) \tag{97}$$

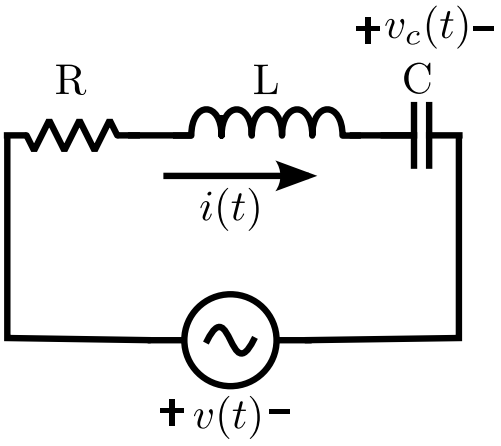


Figure C.1: Series RLC circuit.

Then, we have

$$i(t) = C\frac{dv_c}{dt} = \omega C V_m cos(\omega t) \tag{98}$$

Now,

$$\begin{aligned} \text{Total energy stored in the reactive components} &= \frac{1}{2}Li^2 + \frac{1}{2}Cv^2 \\ &= \frac{1}{2}\omega^2 LC^2 V_m^2 cos^2(\omega t) + \frac{1}{2}CV_m^2 sin^2(\omega t) \end{aligned} \tag{99}$$

At $\omega = \omega_r = \frac{1}{\sqrt{LC}}$, the natural resonance frequency of the RLC circuit, the total energy stored in the reactive components simplifies to $\frac{1}{2}CV_m^2$. The energy dissipated in the resistor per cycle at the natural resonance frequency is $\frac{1}{2}\omega_r^2 C^2 V_m^2 R \cdot \frac{2\pi}{\omega_r}$. So, the QF can be computed to be $\frac{1}{R}\sqrt{\frac{L}{C}}$ using (96).

Considering one of the transfer functions of the series RLC circuit, say, $\frac{I(s)}{V(s)}$, we have,

$$\frac{I(s)}{V(s)} = \frac{sC}{1 + \frac{s}{1/RC} + \frac{s^2}{1/LC}} \tag{100}$$

Comparing the denominator with the standard form [91] $1 + \frac{s}{(QF)\omega_r} + \frac{s^2}{\omega_r^2}$, we can see that the value of QF is the same as that derived using (96).

C.1.1 Important observations on QF

1. (96) is the general definition of QF.

2. In second order systems, the QF can be directly found by comparing the denominator of the transfer function with the standard form $1 + \frac{s}{(QF)\omega_r} + \frac{s^2}{\omega_r^2}$.

3. Considering the general second order transfer function $\frac{1}{1 + \frac{s}{(QF)\omega_r} + \frac{s^2}{\omega_r^2}}$, QF is the magnitude of the asymptotic bode plot at the resonance frequency [91]. The actual peak of the bode plot appears slightly away from the resonance frequency. However, without loss of much accuracy, the magnitude at the resonance frequency is always considered as it can readily be obtained from the transfer function.

4. In second order systems, considering the other standard form $\frac{\omega_r^2}{\omega_r^2 + 2\zeta\omega_r s + s^2}$, the damping factor ζ can be observed to be $\frac{1}{2(QF)}$. Thus, a low QF translates into better damping.

5. From the expression $QF = \frac{1}{R}\sqrt{\frac{L}{C}}$, for a given L and C, a low QF or equivalently a better damping indicates more losses as the resistance has to be increased to achieve better damping.

C.2 Quality factor in higher order systems

The quality factor in higher order systems is complicated by the presence of more than one resonance. The multiple resonance frequencies might be well seperated or might appear close by. Due to this, the magnitude of the bode plot at the natural resonance frequencies are not a good approximation for the QF. The magnitude of the peak of the bode plot would be a good indicator to characterize the resonance in this case. The peak of the bode plot appears at ω_d, the damped resonance frequency. So, the QF can be computed as,

$$QF = \frac{\left|\frac{V_C(j\omega)}{V_i(j\omega)}\right|_{\text{at } \omega = \omega_d}}{\left|\frac{V_C(j\omega)}{V_i(j\omega)}\right|_{\omega \to 0}} \tag{101}$$

The above equation is valid for second order systems also. It would be more accurate than the QF expression $\frac{1}{R}\sqrt{\frac{L}{C}}$.

C.2.1 Application in LCL filter design

In this thesis, (101) has been used for LCL filter damping design as the circuit is of higher order. A low QF is desirable as the design aims at damping the resonance. This is in contrast to resonant converters where a high QF is desirable as the circuit is intended to be operated around resonance and a low QF will lead to higher losses. In LCL filters, resonance phenomenon is due to non-idealities present in the inverter and associated circuitry while the converter itself is intended to be operated at the fundamental frequency which is not same as the resonance frequency. Through damping, the resonance component of current is kept low. A higher damping does require use of a higher value of resistance. However, the low QF ensures that the resonance component of current to be very low and thus the losses due to that component also is low and can usually be neglected as compared to the losses in the damping resistor due to the fundamental frequency and switching ripple components of current.

Appendix D

Quality Factor and Power Loss Expressions

Quality factor (QF) and damping resistor power loss are two parameters that can be used to assess a passive damping scheme. While the QF is a measure of level of damping, the power loss in the damping resistor indicates the trade-off in efficiency due to the addition of the passive damping network. This Appendix lists the state space models and expressions for quality factor and power loss in case of R and SC-R passive damping schemes shown in Fig. D.1.

D.1 State Space Model

The state space models for R and SC-R damped LCL filters can be developed using the state variables (i_i, i_g, v_{cap}) and (i_i, i_g, v_c, v_d) respectively. Fig. D.1 shows the mentioned state variables. i_{R_d} is the output variable for both the cases as the power loss in the damping resistor is the quantity of interest in either case. The state space equations appear below:

D.1.1 R Passive Damping

The state space equations are,

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \end{aligned} \tag{102}$$

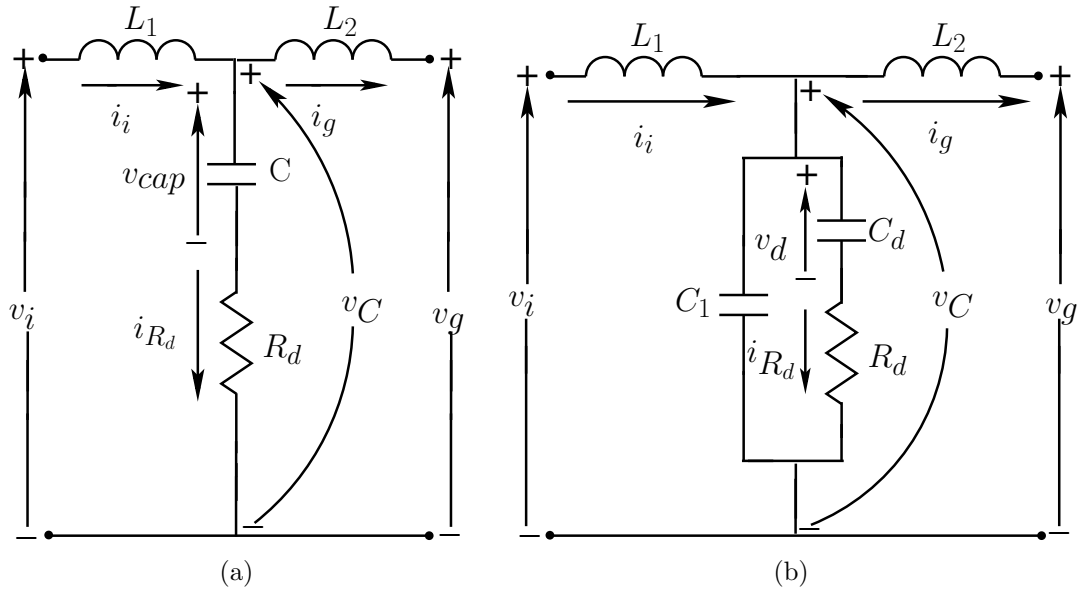


Figure D.1: Passive damping schemes. (a) Purely Resistive (R) damping scheme. (b) Split-Capacitor Resistive (SC-R) damping scheme.

Where,

$$\mathbf{A}=\begin{bmatrix} -\frac{R_d}{L_1} & \frac{R_d}{L_1} & -\frac{1}{L_1} \\ \frac{R_d}{L_2} & -\frac{R_d}{L_2} & \frac{1}{L_2} \\ \frac{1}{C} & -\frac{1}{C} & 0 \end{bmatrix};\ \mathbf{B}=\begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & -\frac{1}{L_2} \\ 0 & 0 \end{bmatrix};\ \mathbf{x}=\begin{bmatrix} i_i \\ i_g \\ v_{cap} \end{bmatrix};$$

$$\mathbf{u}=\begin{bmatrix} v_i \\ v_g \end{bmatrix};\quad \mathbf{C}=[1 \quad -1 \quad 0];\quad \mathbf{D}=[0 \quad 0];\quad \mathbf{y}=i_{R_d};$$

D.1.2 SC-R Passive Damping

The state space equations are,

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \\ \mathbf{y}(t) &= \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \end{aligned} \tag{103}$$

Where,

$$\mathbf{A}= \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ \frac{1}{C_1} & -\frac{1}{C_1} & -\frac{1}{C_1 R_d} & \frac{1}{C_1 R_d} \\ 0 & 0 & \frac{1}{C_d R_d} & -\frac{1}{C_d R_d} \end{bmatrix}; \mathbf{B}= \begin{bmatrix} \frac{1}{L_1} & 0 \\ 0 & -\frac{1}{L_2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}; \mathbf{x}= \begin{bmatrix} i_i \\ i_g \\ v_C \\ v_d \end{bmatrix};$$

$$\mathbf{u}= \begin{bmatrix} v_i \\ v_g \end{bmatrix}; \quad \mathbf{C}= \begin{bmatrix} 0 & 0 & \frac{1}{R_d} & -\frac{1}{R_d} \end{bmatrix}; \quad \mathbf{D}= [0 \;\; 0]; \quad \mathbf{y}= i_{R_d};$$

D.2 Quality Factor

Using Fig. D.1 and the steps listed in Section 2.4.2.2, the transfer function $\frac{V_C(s)}{V_i(s)}$ and the simplified approximate QF expressions for R and SC-R passive damping schemes can be derived and is given below:

D.2.1 R Passive Damping

Using simple circuit principles,

$$\frac{V_C(s)}{V_i(s)} = \frac{L_2\ s + R_d\ C\ L_2\ s^2}{(L_1 + L_2)s + R_d C(L_1 + L_2)s^2 + C L_1 L_2 s^3} \tag{104}$$

With $L_1 = L_2 = L/2$, the QF can be derived to be,

$$QF = \sqrt{1 + \frac{L}{4R_d^2 C}} \tag{105}$$

D.2.2 SC-R Passive Damping

Using simple circuit principles,

$$\frac{V_C(s)}{V_i(s)} = \frac{L_2\ s + R_d\ C_d\ L_2\ s^2}{(L_1 + L_2)s + R_d C_d (L_1 + L_2)s^2 + L_1 L_2 (C_1 + C_d)s^3 + R_d L_1 L_2 C_1 C_d s^4} \tag{106}$$

With $L_1 = L_2 = L/2$ and $C_1 = C_d = C/2$, the QF can be derived to be,

$$QF = 2 \times \sqrt{1 + \frac{L}{CR_d^2}} \tag{107}$$

D.3 Power Loss

The power loss in the passive damping network primarily consists of two components - the fundamental frequency component, P_{fu}, and the switching ripple component, P_{ri}. The fundamental frequency loss component can be computed using simple circuit principles assuming $v_C = 1p.u.$ in Fig. D.1 as explained in Section 2.4.2.3 while the power loss due to the switching ripple component can be computed using state space analysis outlined in the same Section. The closed form expressions for the fundamental frequency loss component in R and SC-R passive damping schemes are given below. The switching ripple loss component is computed numerically using the state space models in Section D.1 and hence does not have closed form expressions.

D.3.1 R Passive Damping

Using simple circuit principles and taking v_C to be 1 p.u.,

$$P_{fu}(p.u.) = \frac{C^2 R_d}{1 + C^2 R_d^2} \tag{108}$$

D.3.2 SC-R Passive Damping

Using simple circuit principles, with $C_1 = C_d = C/2$ and taking v_C to be 1 p.u.,

$$P_{fu}(p.u.) = \frac{C_d^2 R_d}{1 + C_d^2 R_d^2} \tag{109}$$

Appendix E

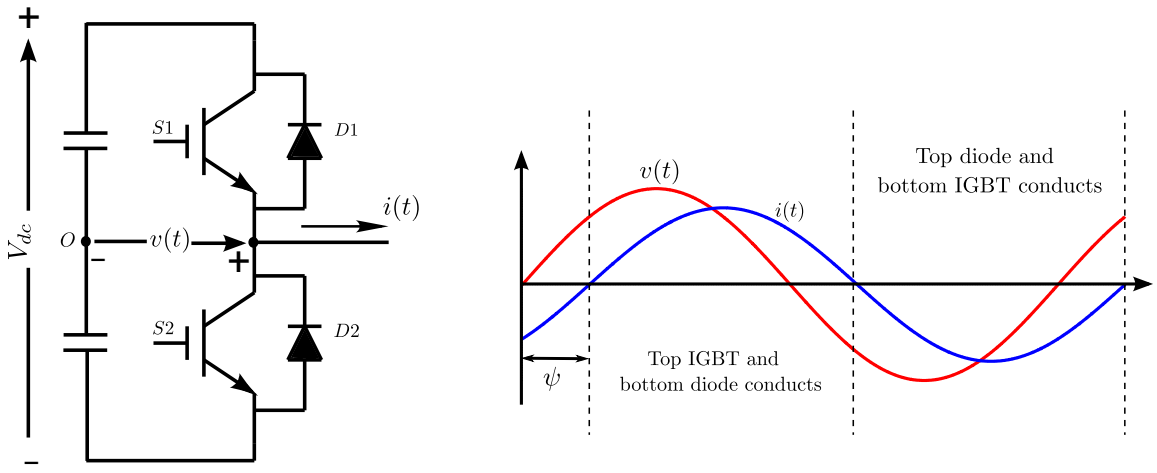
Computation of Semiconductor Power Losses in Inverter

The power loss in the semiconductor devices of an inverter has the following components:

1. Conduction Loss
    a. IGBT conduction loss
    b. Diode conduction loss
2. Switching Loss
    a. IGBT turn-on loss
    b. IGBT turn-off loss
    c. Diode reverse recovery loss
3. Module Terminal Loss

The equations used in this thesis to compute the various power loss components are based on [101]. This Appendix gives the list of formulas used along with some pointers to derive the same.

Conventions Used: Fig. E.1(a) describes the voltage polarity and current direction conventions used in the power loss equations described in this Appendix. Fig. E.1(b) describes the power factor angle ψ at the output terminal of the inverter leg. It also shows the conduction periods of the IGBTs and diodes shown in Fig. E.1(a).



(a) (b)

Figure E.1: Conventions used for power loss computations. (a) One leg of the inverter showing conventions used in power loss computations. (b) Current and voltage waveform at the output of the inverter describing angle ψ and conduction periods of top and bottom IGBTs and diodes.

E.1 Conduction Loss

E.1.1 IGBT Conduction Loss

The average conduction loss (P_{S_cond}) in top IGBT of one leg of the inverter can be computed as,

$$P_{S\_cond} = \frac{1}{2\pi} \int_0^{2\pi} p_S(t)\, d(\omega t) \tag{110}$$

where, $p_S(t)$ represents the instantaneous conduction loss in the top IGBT and is given by,

$$p_S(t) = \begin{cases} [V_{CE0} + r_{CE} \cdot i(t)] \cdot i(t) \cdot D(t), & i(t) \geq 0 \\ 0, & i(t) < 0 \end{cases} \tag{111}$$

where, V_{CE0}, r_{CE} are datasheet parameters of the IGBT, i(t) is the instantaneous current at the output terminal as shown in Fig. E.1(a) and D(t) is the instantaneous duty ratio of the top IGBT.

Assuming sinusoidal voltages and currents at the output of the inverter terminal as shown in Fig. E.1 with a peak current of I_m, modulation index of 'm' under sine-triangle modulation scheme and power factor angle ψ, the closed form expression for average conduction loss in top IGBT, P_{S_cond} can be derived to be,

$$P_{S\_cond} = \frac{1}{2}\left[\frac{V_{CE0}}{\pi} I_m + \frac{r_{CE}}{4} I_m^2\right] + m \cdot \cos\psi \left[\frac{V_{CE0}}{8} I_m + \frac{r_{CE}}{3\pi} I_m^2\right] \tag{112}$$

The conduction loss expression for the bottom IGBT can be derived in a similar manner. The only difference is the conduction period. The bottom IGBT conducts only for $i(t) \leq 0$. The final expression given by (112) is the same for the bottom IGBT also.

E.1.2 Diode Conduction Loss

The average conduction loss (P_{D_cond}) in bottom diode of one leg of the inverter can be computed as,

$$P_{D\_cond} = \frac{1}{2\pi} \int_0^{2\pi} p_D(t)\, d(\omega t) \tag{113}$$

where, $p_D(t)$ represents the instantaneous conduction loss in the bottom diode and is given by,

$$p_D(t) = \begin{cases} [V_{F0} + r_F \cdot i(t)] \cdot i(t) \cdot D'(t), & i(t) \geq 0 \\ 0, & i(t) < 0 \end{cases} \tag{114}$$

where, V_{F0}, r_F are datasheet parameters of the diode, i(t) is the instantaneous current at the output terminal as shown in Fig. E.1(a) and $D'(t)$ is the instantaneous duty ratio of the bottom diode.

Assuming sinusoidal voltages and currents at the output of the inverter terminal as shown in Fig. E.1 with a peak current of I_m, modulation index of 'm' under sine-triangle modulation scheme and power factor angle ψ, the closed form expression for average conduction loss in bottom diode, P_{S_cond} can be derived to be,

$$P_{D\_cond} = \frac{1}{2}\left[\frac{V_{F0}}{\pi} I_m + \frac{r_F}{4} I_m^2\right] - m \cdot \cos\psi \left[\frac{V_{F0}}{8} I_m + \frac{r_F}{3\pi} I_m^2\right] \tag{115}$$

The conduction loss expression for the top diode can be derived in a similar manner. The only difference is the conduction period. The top diode conducts only for $i(t) \leq 0$. The final expression given by (115) is the same for the top diode also.

E.1.3 IGBT and Diode Conduction Losses in CSVPWM

The IGBT and Diode conduction losses can still be computed using (110), (111), (113) and (114). However, the instantaneous duty ratios $D(t)$ and $D'(t)$ are different from that of the sine PWM scheme. The instantaneous duty ratio in any PWM scheme is directly related to the modulating reference waveform. Hence, the difference in the instantaneous duty ratios of the two schemes arise due to the common mode. To get simplified closed form expressions, the common mode can be approximated by a triangular waveform and the triangular waveform's fundamental frequency component alone can be used in the computation of the instantaneous duty ratio without significant loss of accuracy [104]. This adds the following additional terms to (112) and (115) [104],

For IGBT Conduction Loss: $-\frac{2}{15\pi^3} \cdot I_m^2 \cdot r_{CE} \cdot m \cdot \cos(3\psi)$

For Diode Conduction Loss: $+\frac{2}{15\pi^3} \cdot I_m^2 \cdot r_F \cdot m \cdot \cos(3\psi)$

E.2 Switching Loss

E.2.1 IGBT Turn-on and Turn-off Losses

The average switching loss (P_{S_sw}) in any IGBT of the inverter can be computed as,

$$P_{S\_sw} = \frac{1}{2\pi} \int_0^{2\pi} p_{S,sw}(t)\, d(\omega t) \tag{116}$$

where, $p_{S,sw}(t)$ represents the instantaneous switching loss in the IGBT.

Assuming linear variation of E_{on} and E_{off} w.r.t current, the average switching loss in one IGBT can be approximated to be,

$$P_{S\_sw} = f_{sw} \cdot [E_{on} + E_{off}] \cdot \frac{\sqrt{2}}{\pi} \cdot \frac{i_{rated}}{i_{test}} \cdot \left(\frac{V_{dc}}{V_{dc,test}}\right)^{K_{V,IGBT}} \cdot (1 + TC_{Esw}(T_{j,IGBT} - T_{ref})) \tag{117}$$

where,

f_{sw} : operating switching frequency
i_{rated} : rated current
i_{test} : current at which the datasheet parameters have been taken
$K_{V,IGBT}$: exponent for voltage dependency of switching loss $\sim 1.3 \ldots 1.4$
TC_{Esw} : temperature co-efficient of the switching loss ~ 0.003 per ^oC
$T_{j,IGBT}$: operating junction temperature of the IGBT
T_{ref} : reference junction temperature at which the datasheet parameters have been taken

The other parameters are datasheet parameters as mentioned in Table 3.5.

E.2.2 Diode Reverse Recovery Loss

The average reverse recovery loss (P_{D_rr}) in any diode of the inverter can be computed as,

$$P_{D\_rr} = \frac{1}{2\pi} \int_0^{2\pi} p_{D,rr}(t)\, d(\omega t) \tag{118}$$

where, $p_{D,rr}(t)$ represents the instantaneous reverse recovery loss in the diode.

The average reverse recovery loss in one diode can be approximated to be,

$$P_{D\_rr} = f_{sw} \cdot E_{rr} \cdot \left(\frac{\sqrt{2}}{\pi} \cdot \frac{i_{rated}}{i_{test}} \right)^{K_{I,diode}} \cdot \left(\frac{V_{dc}}{V_{dc,test}} \right)^{K_{V,diode}} \cdot (1 + TC_{Err}(T_{j,diode} - T_{ref})) \tag{119}$$

where,

f_{sw} : operating switching frequency
i_{rated} : rated current
i_{test} : current at which the datasheet parameters have been taken
$K_{I,diode}$: exponent for current dependency of reverse recovery loss ~ 0.6
$K_{V,diode}$: exponent for voltage dependency of reverse recovery loss ~ 0.6
TC_{Err} : temperature co-efficient of the reverse recovery loss ~ 0.006 per ^oC
$T_{j,diode}$: operating junction temperature of the diode
T_{ref} : reference junction temperature at which the datasheet parameters have been taken

The other parameters are datasheet parameters as mentioned in Table 3.5.

E.3 Module Terminal Loss

The datasheet parameter $R_{CC'+EE'}$ specifies the lead resistance of the terminals on a per module basis. One module has one leg of the inverter. The power loss per leg or module due to the terminal lead resistance is given by,

$$P_{Mod\_term} = I_{rms}^2 \cdot R_{CC'+EE'} \tag{120}$$

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