SYNCHRONOUS REFERENCE FRAME STRATEGY BASED STATCOM FOR REACTIVE AND HARMONIC CURRENT COMPENSATION

A THESIS

Submitted By

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In partial fulfillment for the award of the Degree of

MASTER OF TECHNOLOGY
IN
ELECTRICAL ENGINEERING

[POWER ELECTRONICS]

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JUNE 2007

ACKNOLEDGEMENTS

I thank my internal guide Dr.Saly George and external guide Mr.A.K.Unnikrishnan for accepting me as a project student. Also, I extend my thanks to Dr. K.M.Moideenkutty for permitting me to do the project outside the institute. And, I thank Ms.Fathima [Director – PEG, C-DAC(T)] for allowing me to do the project with the Power Electronics Group of C-DAC(T) and for the encouragement given throughout the project.

I thank the entire project team under Mr.Unnikrishnan at Power Electronics Group of C-DAC(T) for the help extended during various stages of the project. In particular, I thank, Scientist Mr.Aby Joseph for his guidance right from choosing a good topic till the completion of the project, Scientists Mr.Haneesh, Mr.Subhash Joshi and Mr.Saravana Kumar for clarifying several of the implementation related doubts, Ms.Manju for helping to start with the digital controller and Code Composer Studio, Mr.Afzil for helping to understand the inverter hardware circuit design, Mr.Ramesh for helping me with his SMPS circuits and Mr.Natesh Mayavel for introducing me to Q-formats.

Further, I thank the several research associates at Power Electronics Group of C-DAC(T) who helped me in the construction and testing of the test set-up. In particular, I wish to thank Mr.Sreelal, Mr.Pradeep, Mr.Anoop, Ms.Sreeranjini, Mr.Sajith, Mr.Ranjith and Mr.Shafeer. Also, I acknowledge the encouragement given by scientists [at Power Electronics Group, C-DAC(T)] Mr.Chandrasekar, Mr.Ganesan, Mr.Jinu and Mr.Sekar during the course of the project.

Finally, I would like to mention that without the help and suggestions of my friend Venugopal and the support of my parents, I might never have done a satisfactory project as this.

CONTENTS

ABSTRACT

The issue of power factor improvement and harmonic compensation is well known in electrical engineering. A major area of research in electrical engineering is to make a system wherein the current absorbed from the electrical utility is almost purely sinusoidal and is in phase with the voltage. The need for this is the losses incurred at the transmission otherwise and also the unnecessary expense incurred to have systems (generators, transformers and transmission lines) that can support higher currents. Though it had been a practice to use capacitors, switched capacitor banks, synchronous condensers and several other means to achieve power factor improvement till some time back, problems surfaced with more and more electronic and power electronic equipments being put to use – since now harmonics also had to be tackled. Besides the fact that some of the earlier equipments could not compensate for harmonics, some (like capacitors) others caused issues like resonance. Also, even without the problem of harmonics, the research was to develop systems that can dynamically compensate for reactive current under varying load conditions. The present work is aimed at the study of a STATCOM or Static Synchronous Compensator - as it is otherwise called - as a solution to these (dynamic compensation of reactive and harmonic currents) power quality issues.

In the present study, the synchronous reference frame strategy is used to generate current reference for compensation and conventional PI controllers are used for control. The synchronous reference frame strategy utilizes co-ordinate transformations to separate the reactive and harmonic content in the load current. The design of the closed loop controllers is kept simple by modeling them as first order systems.

The simulation studies showed good results with the reactive current compensation giving almost ideal result of near unity power factor and harmonic currents getting compensated to a larger extent. As expected, harmonic currents could not be completely compensated due to the fact that the inverter produces the output voltage only on a time-averaged sense. However, the Total Harmonic Distortion [THD] readings showed considerable reduction in harmonics.

A test set-up was developed for the purpose of hardware studies. The test set-up was constructed using an Intelligent Power Module (IPM) manufactured by Mitsubishi. The digital controller platform consisted of a fixed-point DSP, the TMS320F2812

processor of Texas Instruments with external ADC's and DAC's interfaced to it. The hardware studies were aimed at understanding different aspects of practical implementation. Studies were made on the generation of unit vectors from the grid voltage, operation of inverter based on Space Vector Modulation, current reference generation, pre-charging of the DC bus capacitor and the like. The studies gave good insight into various implementation challenges and revealed the importance of protection mechanisms in systems that are to be synchronized with the grid. Further, it was understood that systematic testing procedures have to be designed to avoid failure of the system under faults in any hardware and/or software implementations.

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LIST OF ABBREVIATIONS

APF	Active Power Filter
KVL	Kirchhoff's Voltage Law
PCC	Point of Common Coupling
PLL	Phase Locked Loop
SPWM	Sinusoidal Pulse Width Modulation
SRF strategy	Synchronous Reference Frame strategy
SSR	Solid State Relay
STATCOM	Static Synchronous Compensator
SVPWM	Space Vector Pulse Width Modulation
VSI	Voltage Source Inverter

CHAPTER 1

INTRODUCTION

1.1. POWER QUALITY – THE ISSUE

Ideally, the goal of power industry is to supply a purely sinusoidal voltage at fixed amplitude and fixed frequency. Whereas it is the duty of the supplier to provide an almost sinusoidal voltage with less variation in amplitude and frequency, the user also has a part to play in creating such a scenario. The interface point at which the utility company's responsibility ends and the user's responsibility starts is often termed as the point of common coupling (PCC). At the PCC, both the utility company and the user have some factors to comply with. While the utility company has to provide reliable power, the user has to ensure that the load connected does not lead to higher losses in the generation, transmission and distribution systems.

Considering some arbitrary load, the total current consumed can be split into three components – active, reactive and harmonic. Whereas the active current flow leads to real power consumption and is subsequently responsible for the energy absorbed by the system to do work, the reactive and harmonic currents do not lead to any net energy transfer. While the reactive current is required to establish the magnetic medium and is responsible for the energy conversion in electrical systems, the harmonic currents are the result of the switching devices used in electronic and power electronic systems. So, it is evident that one cannot do away with the reactive and harmonic currents. However, since the net energy transfer due to them (during any given fundamental period) is zero, it is not required that these currents have to be taken from the grid. It must be noted that, the 'zero energy transfer' we are talking about is at the PCC. That is, losses at the

generation, transmission and distribution systems do exist when loads draw reactive and harmonic currents. In order to bring down these losses, the utility companies require the user to absorb a nearly purely active current. This is where the user's responsibility lies.

1.2. POWER QUALITY ISSUE – THE HISTORY

The issue of power quality and the concept of power quality compensation has been there from the time the power industry got established. Earlier, the only concern was that of reactive power compensation. Majority of the industrial loads being highly inductive, power was unnecessarily wasted at the generation, transmission and distribution systems. However, with the advent of electronic and power electronic loads, harmonics also added up to the existing problem. While reactive power leads only to losses, the problem due to harmonics is worse. By absorbing harmonic currents, loads distort the supply voltage and make them deviate from there sinusoidal nature. Further, they play havoc with existing reactive current compensation systems like capacitor banks. These issues have lead to the search for better systems that can compensate for both reactive and harmonic currents. The following section traces the various solutions that have evolved over the years on this (power quality compensation) front.

1.3. POWER QUALITY IMPROVEMENT SOLUTIONS – A REVIEW

Following are some of the power quality improvement solutions that have evolved over the years ever since the power industry got established:

1. Fixed capacitors
2. Switched capacitor banks
3. Synchronous condensers
4. Static VAR compensators
5. Active Power Filters

Let us look at the principle behind each of the above solution strategies.

1.3.1. Fixed capacitors

The use of the fixed capacitors is the first attempt towards reactive current compensation. Fig.1.1 shows a system employing fixed capacitor. When a capacitor is placed in shunt as shown, the voltage at the PCC forces a fixed leading current to flow. This compensates for the lagging current drawn by the load. Obviously, the disadvantage is that the leading current drawn is fixed by the PCC voltage and when the load is varying, there will always be improper compensation.

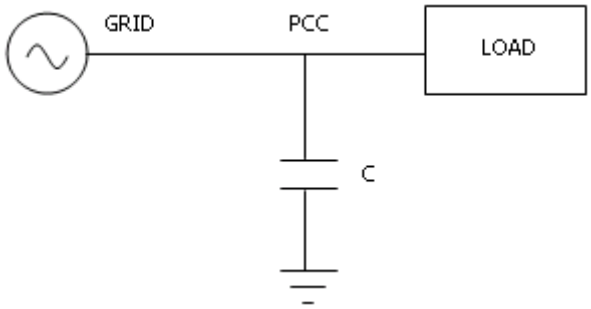

Fig.1.1. Reactive current compensation using fixed capacitor

1.3.2. Switched capacitor banks

The switched capacitor banks came up as a solution to the problem of improper compensation under varying load conditions. Capacitor banks were used with manual switches as shown in Fig.1.2. Capacitors will be switched in and out of the system manually, according to the load. However, the compensation was still not exact.

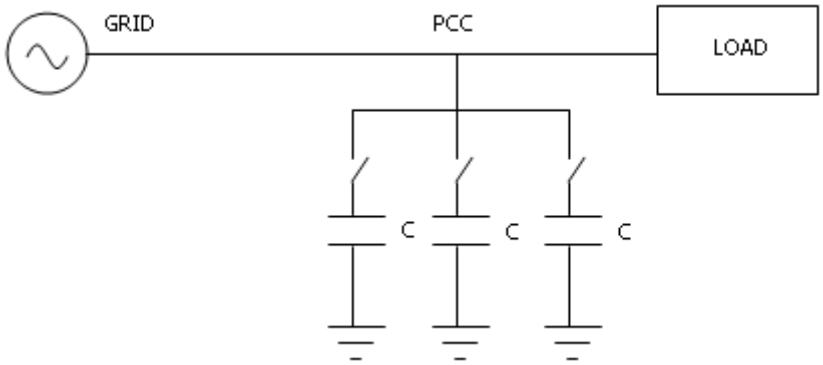

Fig.1.2. Reactive current compensation using switched capacitor banks

1.3.3. Synchronous condensers

Synchronous machines, when connected to the grid, can be used to absorb or deliver reactive current. Actually, it acts as a variable voltage source behind a reactance as shown in Fig.1.3.

The advantages of synchronous condensers over fixed and switched capacitors are:

1. They can be controlled to follow the reactive current demand of the system
2. The reactive current compensation is not fixed entirely by the PCC voltage (though PCC voltage also influences it)
3. They can provide both lagging and leading reactive currents

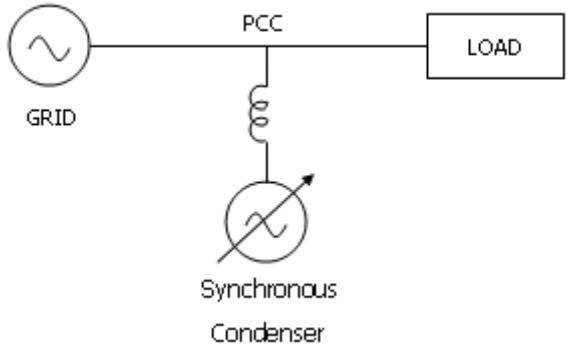

Fig.1.3. Reactive current compensation using synchronous condensers

Though synchronous condensers were a step forward in the area of reactive current compensation as they are dynamic unlike the capacitor based compensation, they still had the following disadvantages:

1. They cannot respond quickly to varying load conditions. The response is sluggish owing to the inertia of the mechanical parts involved
2. They cannot be used to compensate for harmonic currents absorbed by the load

1.3.4. Static Var Compensator (SVCs)

SVCs are one of the first attempts in using power electronics for power quality compensation. Fig.1.4 shows an SVC. As shown, the compensating system can be controlled to follow the load's reactive power requirement by controlling the thyristors. The major disadvantage is that the compensating system itself will inject harmonics into the system due to switching action.

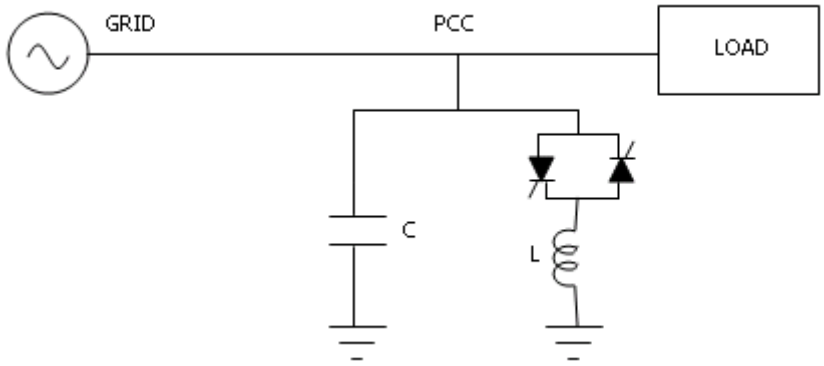

Fig.1.4. Static Var Compensator (SVC)

1.3.5. Active Power Filters (APFs)

The various compensation methods discussed so far were in use when there was no problem of harmonics. With the advent of harmonic loads, the capacitor based compensation techniques had a set-back as the capacitors got heated up due to large harmonic current flows and sometimes there was failure due to resonance phenomenon too. The synchronous condensers and SVCs also could not compensate for the harmonic currents and hence there was a need for developing newer methods of power quality compensation. Active power filters were the result of research in this direction and they aid in dynamic compensation of reactive and harmonic currents demanded by the load.

As shown in Fig.3.5, active power filters are basically voltage source inverters behind a reactance. They can be controlled to continuously track and compensate for the reactive current demanded by the load.

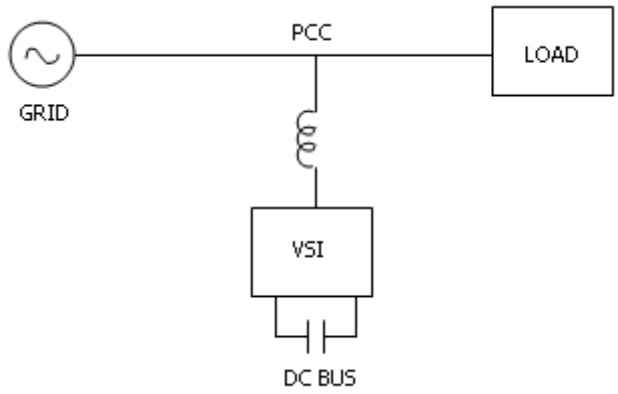

Fig.1.5. Active Power Filter (APF)

1.4. MOTIVATION, SCOPE AND OBJECTIVE OF THE THESIS

The present study on STATCOM is based on the importance of active power filters as a solution for power quality compensation. The study is aimed at understanding the basic idea behind the implementation of active power filters and to study STATCOM as a means for dynamically compensating reactive and harmonic currents demanded by the load. The present work is aimed at the design (of controller) and simulation of a synchronous reference frame strategy based STATCOM and to study various aspects of the practical implementation of the same using a digital controller. In the implementation front, the aim is to generate unit vectors from the grid voltage, operate a voltage source inverter using space vector modulation, generate current reference and understand the need and implementation details of pre-charging and the like.

1.5. OUTLINE OF THE THESIS

In this chapter, the issue of power quality was discussed in detail and the various compensation methods that have evolved over the years have been outlined. Then, the motivation for the present work on STATCOM and its scope and objectives were provided.

Chapter 2 gives an overview of STATCOM and explains how three major sections can be identified in the development of a STATCOM. Chapter 3 to

Chapter 5 details those three major sections namely the current reference generation, controller and the inverter hardware. In Chapter 6, several implementation details are given followed by a discussion of results in Chapter 7. Finally, Chapter 8 concludes the thesis and provides inputs for further study in the area of STATCOM.

CHAPTER 2

STATCOM

2.1. STATCOM – A SIMPLIFIED PICTURE

STATCOM is a Voltage Source Inverter (VSI) connected in shunt to the system at the point of common coupling (PCC) as shown in Fig.2.1. The load current can be thought of as having three components – active, reactive and harmonic. The idea is to control the voltage source inverter in such a way as to make it deliver the reactive and harmonic currents demanded by the load so that the grid has to supply only the active current. This means that the grid current will be purely sinusoidal and will be in-phase with the grid voltage on connecting the STATCOM. Ideally, it is possible to supply the reactive and harmonic current requirement of the load with a VSI having a DC bus capacitor and no external power source as the net power supplied by the STATCOM during any given fundamental period is zero. However, a small amount of real power will be absorbed from the grid practically – to compensate for the energy losses in the system.

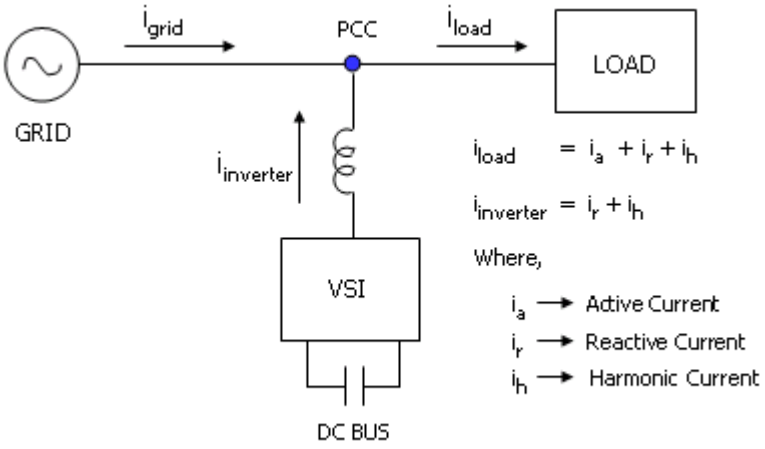

Fig.2.1.Voltage source inverter as a grid connected STATCOM

From the brief description given above, it is clear that the design of a STATCOM has three broad sections:

1. Current reference generation (It involves computing the reactive and harmonic current absorbed by the load).
2. Design of closed loop controller (It is the controller that makes the STATCOM current follow the reference).
3. Design of the VSI hardware (includes choosing DC bus capacitor and choke)

2.2. CURRENT REFERENCE GENERATOR, CONTROLLER & PLANT

The first part of the design is to generate the current reference. There are several methods to generate the current reference. The present study is based on the application of co-ordinate transformations to separate out the reactive and harmonic content of the load current. The strategy used is the *synchronous reference frame (SRF) strategy*. Chapter 3 gives a detailed description of the SRF strategy.

Once the current reference has been generated, the next work is to design the controller. For this, one needs to analyze the system and identify the job of the controller. Remembering that the STATCOM is basically a voltage source inverter and that we have the current reference that is to be tracked, it is clear that the only job that is left is to make the output current of the voltage source inverter follow the current reference. This can be done in two ways. One is by *current control of VSI* and the other is through *voltage control of VSI*. The present study utilizes the *space vector modulation technique* to control the VSI i.e. it follows a voltage-based control of VSI. This requires the current reference to be converted into an equivalent voltage reference. This is where the controller is to be employed. Thus, the job of the controller in the present case is to convert the current reference into an equivalent voltage reference to facilitate a voltage based control of the VSI. A detailed explanation of the controller and its design is given in Chapter 4.

Combining the above facts, the complete system can be visualized as given in Fig.2.2. Here, the VSI is represented as a variable voltage source as the output voltage of the VSI varies in response to the control signal (so that the output current tracks the reference i^*).

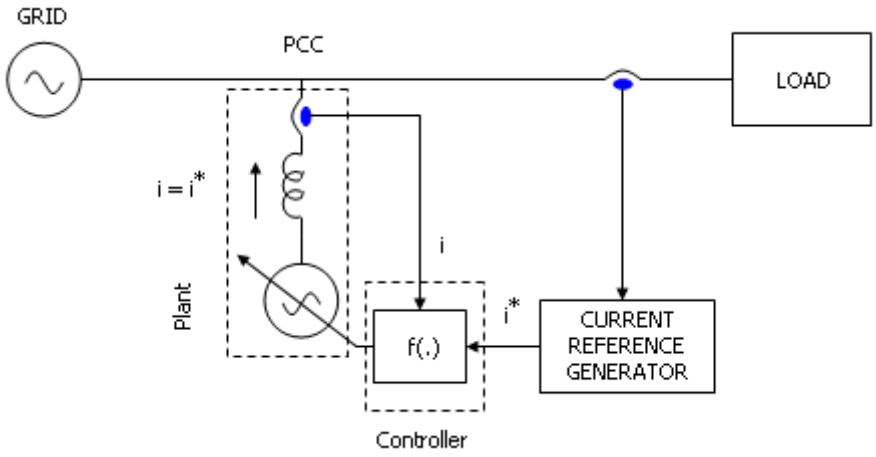

Fig.2.2.Conceptual representation of the complete system (STATCOM)

The final part is the hardware design of the VSI. It involves various aspects like choosing the devices of correct ratings, choosing the proper value for capacitor and choke, providing various protections, etc. A detailed explanation of the hardware design is given in Chapter 5.

In this chapter an outline of STATCOM was given. The design of the STATCOM was classified under three major sections and a brief idea about each of the sections was provided. The following chapters elaborate on these sections.

CHAPTER 3

SYNCHRONOUS REFERENCE FRAME STRATEGY

Synchronous reference frame strategy is a popular method used in the generation of the current reference. This chapter explains the synchronous reference frame strategy in detail.

3.1. INTRODUCTION

The synchronous reference frame strategy uses co-ordinate transformations to generate the current reference. It employs the well known *Clarke's Transformation* and *Park's Transformation* for this purpose. Though, the transformations remind us of the 'primitive machine model' concept, it may be noted that here there is no need to satisfy the condition of 'Power Invariance' as the transformations are employed just to reduce the computations involved in generating the current reference and not to develop any equivalent system. As will be seen in Chapter 4, once the controller output is obtained, reverse transformations are employed to transform the quantities back to the actual three-phase system. Thus, 'Power Invariance' never gets into the picture.

3.2. THE CLARKE'S TRANSFORMATION

Consider a three-phase *balanced* system given by eqns. (3.1), (3.2) and (3.3),

$$v_a = V_m \sin(\omega t - \phi) \quad \text{----------} \quad (3.1)$$

$$v_b = V_m \sin(\omega t - \phi - 120°) \quad \text{----------} \quad (3.2)$$

$$v_c = V_m \sin(\omega t - \phi + 120°) \quad \text{----------} \quad (3.3)$$

The system being balanced, just two parameters can define it completely rather than three parameters (v_a, v_b, v_c) as given above. Knowing any two of (v_a, v_b, v_c), we can always write down the third one since $v_a + v_b + v_c = 0$ (Though a sinusoidal system is considered here for simplicity, any non-sinusoidal balanced three phase system can be represented by just two parameters). This fact that two parameters are enough to describe a balanced three phase system should be convincing enough to accept the transformation of a three phase balanced system (a, b, c) to a two axis system (α-β) as shown in Fig.3.1. The α-β plane is often called a stationary frame of reference to distinguish it from the other two-axis plane to be defined later in this chapter.

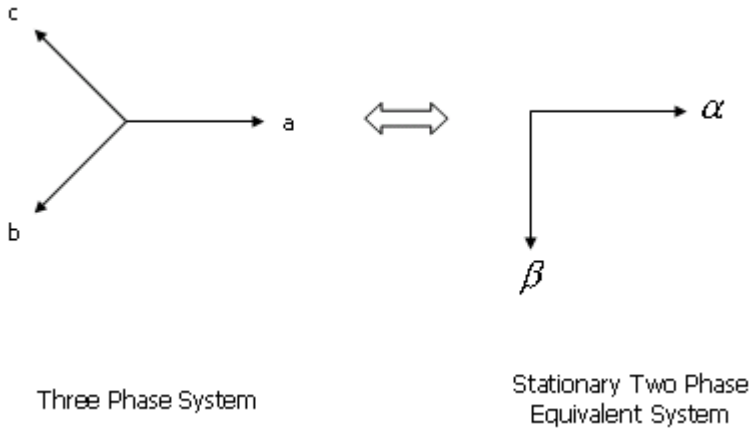

Fig.3.1. α-β plane – defined

To write the equations of transformation, the vectors 'b' and 'c' need to undergo an orthogonal decomposition along 'α' and 'β' axis. Fig.3.2 shows the decomposition of one of the axes ('b' axis) along 'α' and 'β' axis.

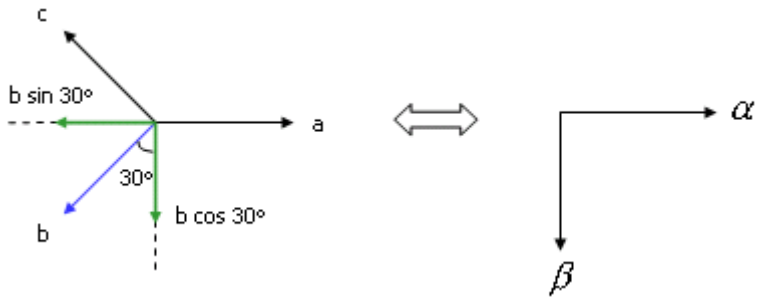

Fig.3.2. Clarke's Transformation

From Fig.3.2,

$$\alpha = a - \frac{1}{2}b - \frac{1}{2}c \qquad \text{----------} \quad (3.4)$$

$$\beta = \frac{\sqrt{3}}{2}b - \frac{\sqrt{3}}{2}c \qquad \text{----------} \quad (3.5)$$

In compact matrix form, the above *forward transformation* equations appear as,

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \qquad \text{----------} \quad (3.6)$$

From eqn. (3.6) and utilizing the fact that $a + b + c = 0$, the *reverse transformation* can easily be derived to be,

$$\begin{bmatrix} a \\ b \\ c \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \qquad \text{----------} \quad (3.7)$$

The system of transformation equations (3.6) and (3.7) constitute the *Clarke's Transformation*. This transformation lets us deal with just two equations in the place of three equations. Thus, it saves a lot of computational effort. As will be seen from the following discussions, it provides a simpler means to generate the current reference.

3.3. THREE PHASE QUANTITIES IN THE α – β PLANE

Let us have a detailed look at how the three phase quantities appear in the stationary α-β plane. This will aid in the understanding of the basics of co-ordinate transformation approach to current reference generation.

Let the three phase balanced system of grid voltages be,

$$v_a = V_m \sin(\omega t) \qquad \text{----------} \quad (3.8)$$

$$v_b = V_m \sin(\omega t - 120°) \qquad \text{----------} \quad (3.9)$$

$$v_c = V_m \sin(\omega t + 120°) \qquad \text{----------} \quad (3.10)$$

Transforming the above equations to α-β plane using eqn. (3.6), we have,

$$v_\alpha = \frac{3}{2} V_m \sin(\omega t) \qquad \text{----------} \quad (3.11)$$

$$v_\beta = -\frac{3}{2} V_m \cos(\omega t) \qquad \text{----------} \quad (3.12)$$

Now, we define $\overline{V} = v_\alpha + jv_\beta$ where 'j' is the imaginary operator. '$\overline{V}$' is called the *space vector*. The concept is similar to and has many advantages like "phasor" representation of sinusoidal quantities.

Applying the definition of space vector to eqns. (3.11) and (3.12) we have,

$$\overline{V} = v_\alpha + jv_\beta$$

$$\overline{V} = \frac{3}{2} V_m \sin(\omega t) - j\frac{3}{2} V_m \cos(\omega t)$$

$$\overline{V} = -j\left(\frac{3}{2} Vm \cos(\omega t) + j\frac{3}{2} Vm \sin(\omega t)\right)$$

$$\overline{V} = -j\frac{3}{2} V_m \cdot e^{j(\omega t)}$$

$$\boxed{\overline{V} = \frac{3}{2} Vm \cdot e^{j(\omega t - 90°)}} \qquad \text{----------} \quad (3.13)$$

The usefulness of '$\overline{V}$' is that it gives a good insight about how the three phase quantities appear in the α-β plane.

The following facts can be concluded from eqn. (3.13),

1. The magnitude of the space vector is a constant and equal to $\frac{3}{2}$ times the amplitude (V_m) of the three phase sinusoid.
2. When plotted with the (α-β) axes as (x-y) axes, the space vector starts at $-90°$ and rotates in the anti-clockwise direction.
3. The space vector completes 'f' revolutions per second where 'f' is the frequency of the three phase system in 'Hz'.
4. At time 't' from the reference time (t = 0), the space vector would have moved away from $-90°$ by 'ωt' radians in the anti-clockwise direction.

Fig.3.3 depicts the above facts pictorially.

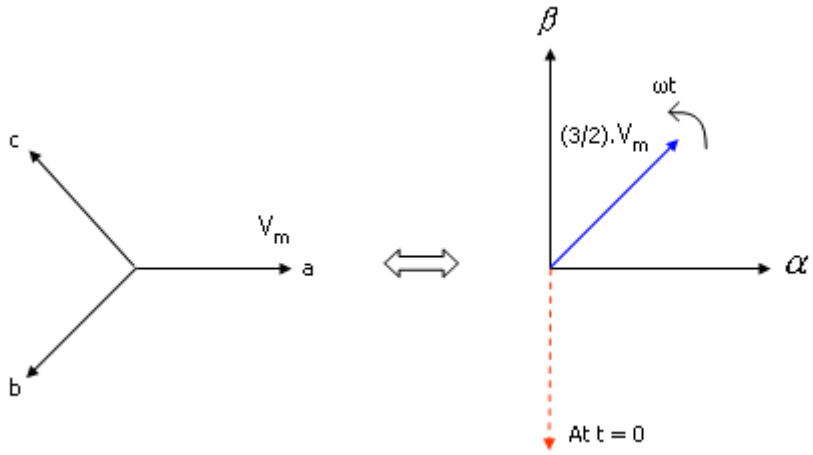

Fig.3.3. Three phase balanced voltages as space vector in α-β plane

3.4. REACTIVE CURRENT REFERENCE GENERATION

Continuing with the discussion in the last section, let us assume that the set of balanced three phase line currents that flow from the grid to be,

$$i_a = I_m \sin(\omega t - \phi) \quad \text{----------} \quad (3.14)$$

$$i_b = I_m \sin(\omega t - \phi - 120°) \quad \text{----------} \quad (3.15)$$

$$i_c = I_m \sin(\omega t - \phi + 120°) \quad \text{----------} \quad (3.16)$$

Then, the grid voltage and line current space vectors will appear in the α-β axis as shown in Fig.3.4.

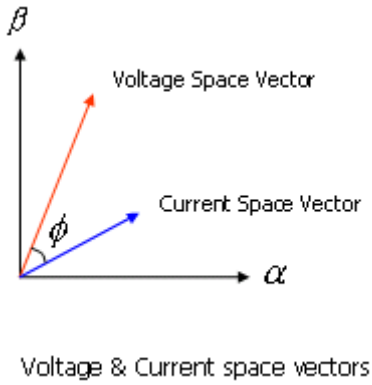

Fig.3.4. Grid voltage and line current space vectors

Now, as shown in Fig.3.5, the current space vector can be split into two component vectors – one in phase with the (grid) voltage space vector and another lagging the voltage space vector by 90^{o}.

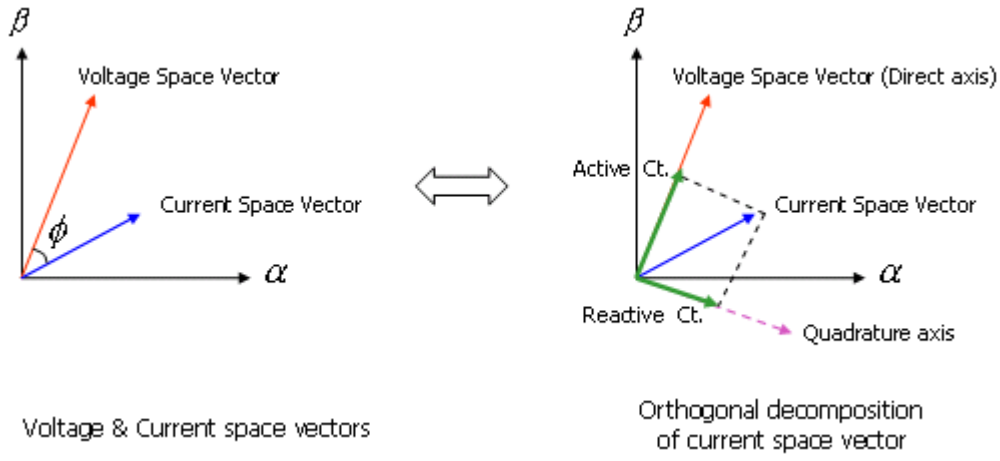

Fig.3.5. Decomposition of current space vector into its component vectors

From the earlier discussion in section 3.3, the following facts can be deduced:

1. The in-phase component corresponds to a three phase system of currents that are in-phase with the three phase grid voltages and represents the active component of the load current

2. The lagging component corresponds to a three phase system of currents that lag the three phase grid voltages by 90^o and represents the reactive component of the load current

Further, we can say from the sign of the lagging component whether the load is inductive or capacitive. A positive sign indicates an inductive load whereas a negative sign represents a capacitive load.

Thus, the current reference for reactive current compensation can be obtained in the α-β plane by the following two simple steps:

1. Track the angle between the voltage and current space vectors continuously. Let the angle be 'ϕ'. i.e. $\phi = \angle\overline{V} - \angle\overline{I}$.
2. Then,
    a. Instantaneous active current = $|\overline{I}|\cos\phi$ and
    b. Instantaneous reactive current = $|\overline{I}|\sin\phi$

3.5. HARMONIC CURRENT REFERENCE GENERATION AND NEED FOR PARK'S TRANSFORMATION

In view of the difference in the frequencies of the fundamental and harmonic currents, one might attempt the generation of the harmonic current reference through a simple filter. However, it is not as easy as it seems to be. To understand the difficulty involved, let us proceed trying to compensate for both harmonic and reactive currents. Then, Fig.3.6 would be a probable scheme. Here, the high pass filtering is being done before conversion to α-β plane. As shown in the figure, a compensator is required to account for the phase and magnitude deviations in the low pass filtered signal. The problem arises even if the filtering is done in the α-β plane eventhough a little simplification would be achieved since the number of filters required would be one less than that required in the a-b-c plane. Park's Transformation provides a solution to this problem and eliminates the need for a compensator.

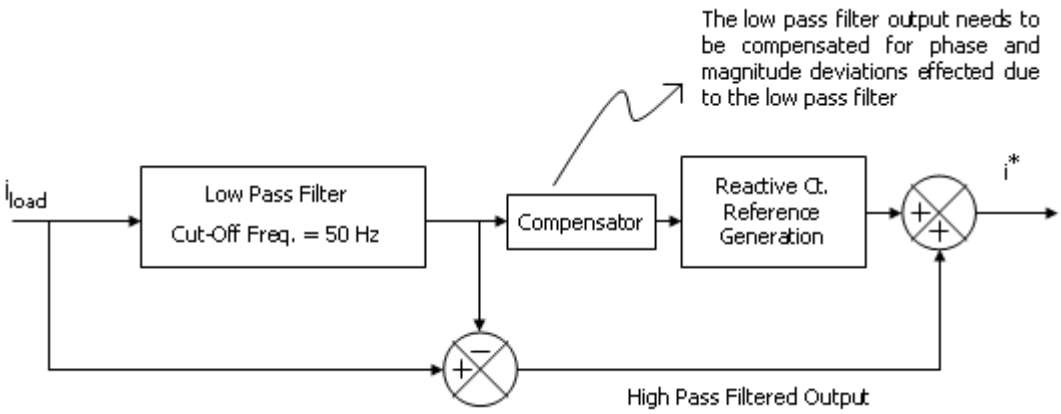

Fig.3.6. Complexity in compensation without the use of Park's Transformation

3.6. THE PARK'S TRANSFORMATION

Park's transformation is nothing more than finding the components of the load current along the direction of the voltage space vector and at quadrature to it as shown earlier in Fig.3.5 [So, it has to be used even if the load is purely linear and only reactive current needs to be compensated]. Fig.3.7 shows how the d-q plane (direct-quadrature plane, the name having its origin from the machines concepts) has been defined in the present study. The voltage space vector has been taken as the d-axis and an axis leading the d-axis by 90^o is taken as the q-axis. It must be noted that the α-β plane shown in Fig.3.7 is in accordance with the earlier definition of the α-β plane (Fig.3.1) and is different from that in Fig.3.3. The differences that arise (in the way the space vectors appear in the α-β plane) due to this can easily be understood by applying the approach followed in section 3.3.

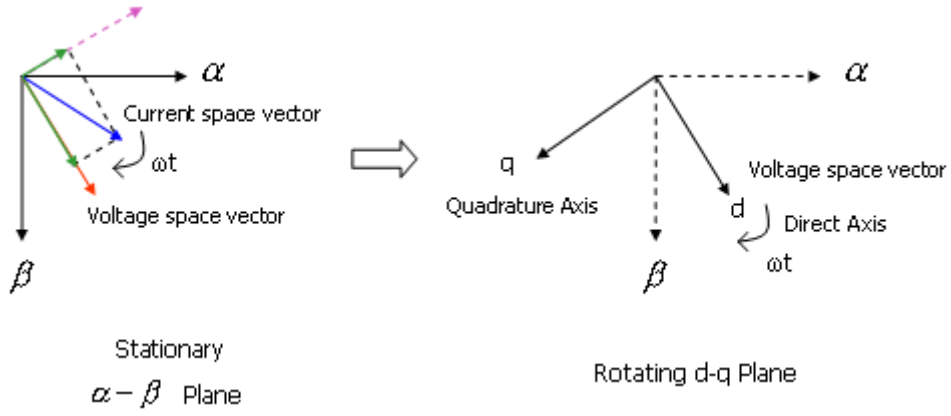

Fig.3.7. d-q plane defined

The advantage of taking the voltage space vector as one of the axis in the d-q plane is that now the d-component and q-component of fundamental current would directly give the active and reactive components respectively (However, the q-component will be negative for an inductive load and positive for a capacitive load as can be observed from Fig.3.7). Since the d-axis is always aligned along the voltage space vector and the voltage space vector is rotating 'f' times every second in the clockwise direction, the transformation actually effects a conversion to a rotating frame of reference.

The equations of transformation can be arrived at easily by decomposition of α and β components along the d and q axis. Fig.3.8 shows the decomposition of one of the components (α-component) along the d and q axis.

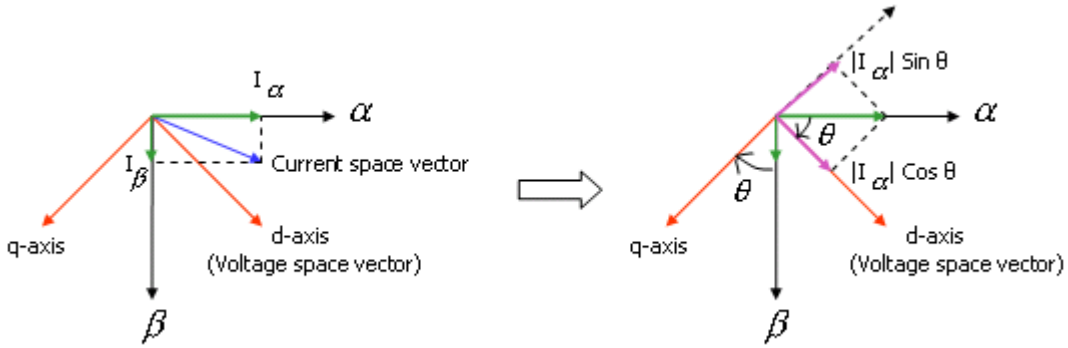

Fig.3.8. Park's Transformation

From Fig.3.8, we have,

$$d = \alpha\cos\theta + \beta\sin\theta \qquad \text{----------} \quad (3.17)$$

$$q = -\alpha\sin\theta + \beta\cos\theta \qquad \text{----------} \quad (3.18)$$

In compact matrix form, the above *forward transformation* equations appear as,

$$\begin{bmatrix} d \\ q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \qquad \text{----------} \quad (3.19)$$

The *reverse transformation* can easily be found by inversion (since the 2x2 matrix is not singular) and is given by,

$$\begin{bmatrix} \alpha \\ \beta \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} d \\ q \end{bmatrix} \quad \text{---------- (3.20)}$$

The system of transformation equations (3.19) and (3.20) constitute the *Park's Transformation*.

Unlike the earlier transformation, here the transformation matrix contains variables rather than constants. This is because we are shifting to a plane which is rotating continuously. In order to do the transformation, we require cos θ and sin θ which are generally referred to as cos and sin unit vectors respectively. They are called the unit vectors as they help us get the projection of vectors along particular directions and in that sense act like unit vectors in that particular direction. Fig.3.9 will help us find cos and sin unit vectors [Note that the definition of 'θ' in the figure is important].

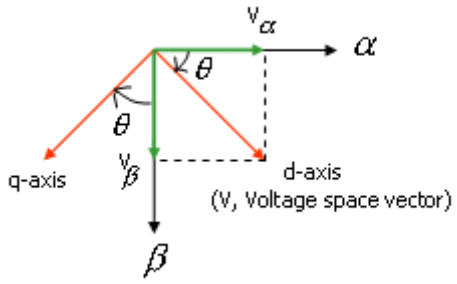

Fig.3.9. Unit vectors

From Fig.3.9, we have,

$$\cos\theta = \frac{|V_\alpha|}{|V|} = \frac{\frac{3}{2}V_m \sin(\omega t)}{\frac{3}{2}V_m} = \sin(\omega t) \quad \text{---------- (3.21)}$$

$$\sin\theta = \frac{|V_\beta|}{|V|} = \frac{-\frac{3}{2}V_m \cos(\omega t)}{\frac{3}{2}V_m} = -\cos(\omega t) \quad \text{---------- (3.22)}$$

From the above derivation, it is evident that the unit vectors can be generated by transforming the grid voltage to α-β plane and then dividing the α-component and β-component by the magnitude of the space vector $\left[\sqrt{|V_\alpha|^2+|V_\beta|^2}\right]$. Thus the unit vector generation block will be as shown in Fig.3.10.

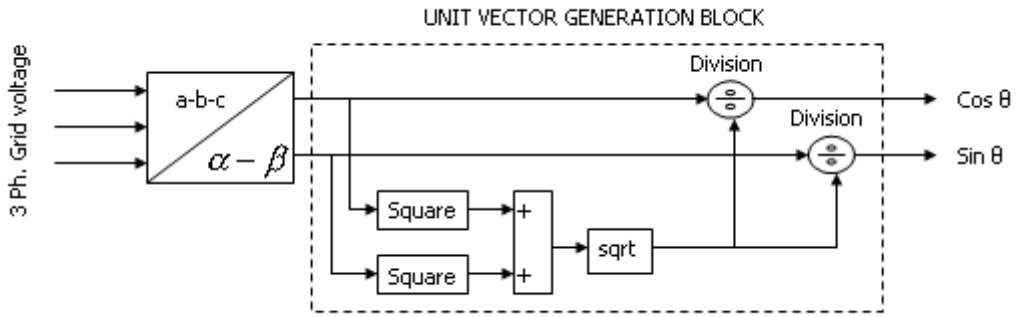

Fig.3.10. Unit vector generation from grid voltage

3.7. REFERENCE CURRENT GENERATION IN THE D-Q PLANE

In a balanced three phase system of loads that absorb active, reactive and harmonic currents, the total current can be represented as a sum of sinusoids of fundamental and harmonic frequencies. To generate the reference current for compensation, we need to know how these different components appear in the d-q plane. To understand this, let us consider a balanced three phase system with a grid frequency of ω_V (represents the fundamental frequency) and a load current component of arbitrary frequency ω_i (The component might be the fundamental or any of the harmonic frequencies) as shown below:

Grid voltage:

$$v_a = V_m \sin(\omega_v t)$$
$$v_b = V_m \sin(\omega_v t - 120°)$$
$$v_c = V_m \sin(\omega_v t + 120°)$$

Load current:

$$i_a = I_m \sin(\omega_i t - \varphi)$$
$$i_b = I_m \sin(\omega_i t - 120° - \varphi)$$
$$i_c = I_m \sin(\omega_i t + 120° - \varphi)$$

From the earlier discussion of unit vector generation, we can write,

$$\cos\theta = \sin\left(\omega_v t\right)$$
$$\sin\theta = -\cos\left(\omega_v t\right)$$

Now, the transformation of the currents to the d-q axis will be as follows,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \sin\omega_v t & -\cos\omega_v t \\ \cos\omega_v t & \sin\omega_v t \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \sin\omega_v t & -\cos\omega_v t \\ \cos\omega_v t & \sin\omega_v t \end{bmatrix} \begin{bmatrix} \frac{3}{2} I_m \sin\left(\omega_i t - \varphi\right) \\ -\frac{3}{2} I_m \cos\left(\omega_i t - \varphi\right) \end{bmatrix}$$

$$\Rightarrow \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{3}{2} I_m \cos\left[\left(\omega_i - \omega_v\right)\cdot t - \varphi\right] \\ \frac{3}{2} I_m \sin\left[\left(\omega_i - \omega_v\right)\cdot t - \varphi\right] \end{bmatrix} \quad \text{---------- (3.23)}$$

From eqn. (3.23), we can conclude the following,

1. When $\omega_i = \omega_v$, i.e. for fundamental component of current,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \frac{3}{2} I_m \cos\left(-\varphi\right) \\ \frac{3}{2} I_m \sin\left(-\varphi\right) \end{bmatrix}$$

From the expression it is evident that the fundamental component appears as DC in the d-q plane. Further, when $\varphi = 0^o$, only i_d is non-zero as expected since $\varphi = 0^o$ represents a purely active fundamental current and it should be aligned with the voltage space vector or equivalently the d-axis. Similarly, for $\varphi = \pm 90^o$, only i_q is non-zero representing that reactive fundamental current appears only along the q-axis.

2. When $\omega_i \neq \omega_v$, i.e. for harmonic load currents, both d and q axis currents are non-zero, of equal amplitude and both are sinusoidally varying. This implies that the harmonics appear as ripples in the d and q axis. (A more detailed analysis will show that the frequency of the harmonic components increase or decrease by one fundamental frequency depending upon whether the sequence of the particular harmonic is negative or positive respectively).

From the above observations, we can have the following rules for reference current generation in the d-q plane,

1. Reactive current compensation: The dc component in the q-axis will serve as the reference for reactive current compensation.

2. Harmonic current compensation: The ac component in the d and q axis will serve as the reference for the harmonic current compensation.

Thus for a composite compensation, high pass filtered d-axis component (blocking only the dc component) and the entire q-axis component will be taken as the reference current. The high pass filter for the d-axis will be implemented through a low pass filter.

The block diagram for a composite compensation of both reactive and harmonic currents is shown in Fig.3.11.

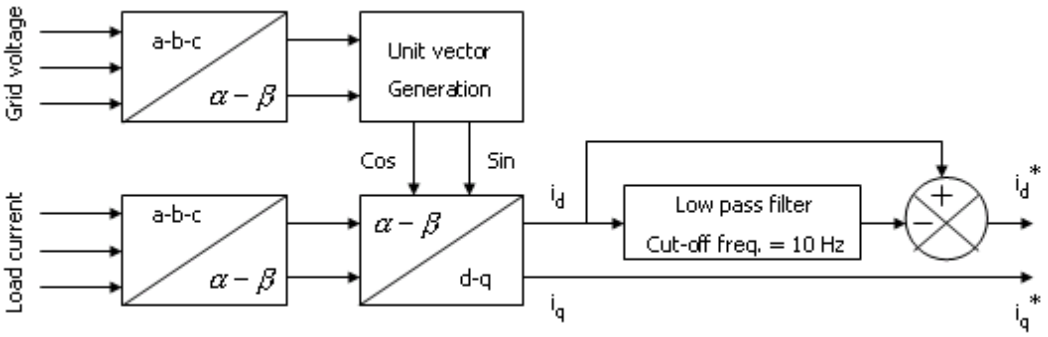

Fig.3.11. Current reference generation for composite compensation

It may be noted that in the above compensation procedure, the only place where a filter is used is the high pass filter in the d-axis. It is being implemented as a low pass filter whose output is subtracted from the original signal. Since the high pass filter has to block only the dc component, the cut-off frequency of the low pass filter will be set as say, 10 Hz. Now, the output of the low pass filter being dc, it will not suffer any magnitude or phase deviation as can be readily observed from a Bode plot as shown in Fig.3.12. So, there needs to be no compensator anywhere. Thus, the Park's Transformation reduces the complexity in the implementation.

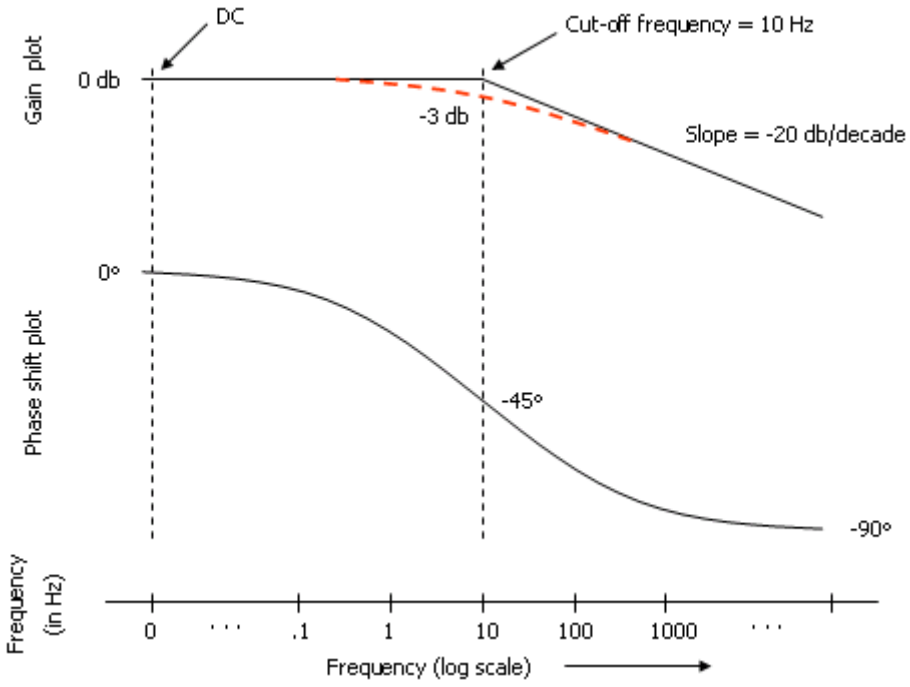

Fig.3.12. Bode plot of low pass filter with cut-off frequency 10 Hz

In this chapter, a detailed explanation of the synchronous reference frame strategy was given and the transformation equations for the Clarke's and Park's Transformation were derived. A detailed idea about how the three phase quantities appear in the α-β and d-q plane was provided and this aided in understanding how the reactive and harmonic current reference can be generated using co-ordinate transformations.

CHAPTER 4

CURRENT AND VOLTAGE CONTROLLERS

In STATCOM, the aim is to make the VSI continuously track and deliver the reactive and harmonic currents demanded by the load. This calls for the use of a *current controller*. Theoretically speaking, this alone should suffice. But practically, the voltage in the DC bus capacitor will generally reduce continuously if there is no controller in place to maintain it at a desired value. The reason for this is that there will be losses at the switching devices (conduction loss and switching loss) and power dissipation at the choke that connects the inverter to the grid (due to the small but finite resistance associated with it). The only source of energy being the DC bus capacitor, it is obvious that it should lose some voltage (as energy stored in the capacitor is given by $\frac{1}{2}CV^2$) to meet the energy losses in the system. So, there needs to be a *voltage controller* to maintain the DC bus voltage at a desired value (or equivalently - to meet the real power requirement of the system). The following sections discuss the controllers in detail.

4.1. THE CURRENT CONTROLLER

4.1.1. Basic idea

The current controller can be better understood by assuming that the DC bus voltage remains constant (that is, by assuming the system to be lossless). With this assumption, once the current reference has been generated from the load current, the problem reduces to making the inverter deliver the same at the PCC with the help of the current controller. This means that the controller along with the inverter should resemble an all pass filter as shown in Fig.4.1.

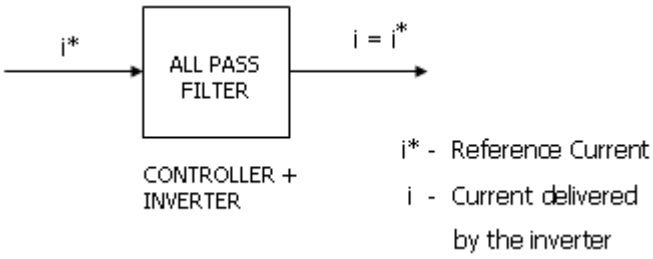

Fig.4.1. Ideal controller-inverter set-up of STATCOM

However, in reality, the controller-inverter setup cannot resemble an all-pass system. To understand this better, let us have a closer look at the inverter. As shown in Fig.4.2, taking a virtual ground at the midpoint of the DC bus capacitor, each pole of the two-level inverter (In the present study, a two-level inverter is used. It will be called simply as 'inverter' in the discussions.) can have only two possible discontinuous output states (voltages) $+\frac{V_{dc}}{2}$ *and* $-\frac{V_{dc}}{2}$. This means that the inverter is incapable of following any continuous current reference directly (as it would require the inverter to be able to produce a continuous voltage at its output).

This raises an interesting question, how a continuous voltage can be produced at the inverter output so that the inverter current can follow the current reference (which will be continuous).

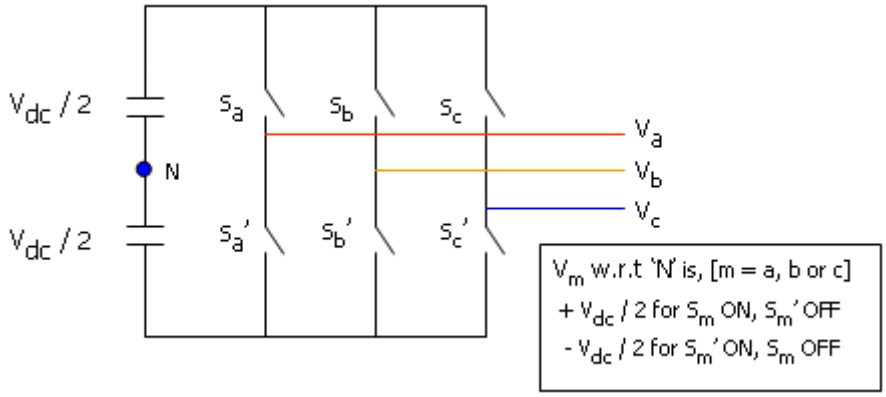

Fig.4.2. Two level inverter

As shown in Fig.4.3 for a sinusoidal pole voltage example, in an inverter, continuous voltages are produced in a time-averaged sense by switching between $+V_{dc}/2$ and $-V_{dc}/2$ at a very high frequency. By time-averaged sense, it is meant that the net area under both the curves is the same during the small interval (switching time period) considered. This is where the various modulation techniques come into play. They help us get the required output voltage in a time-averaged sense.

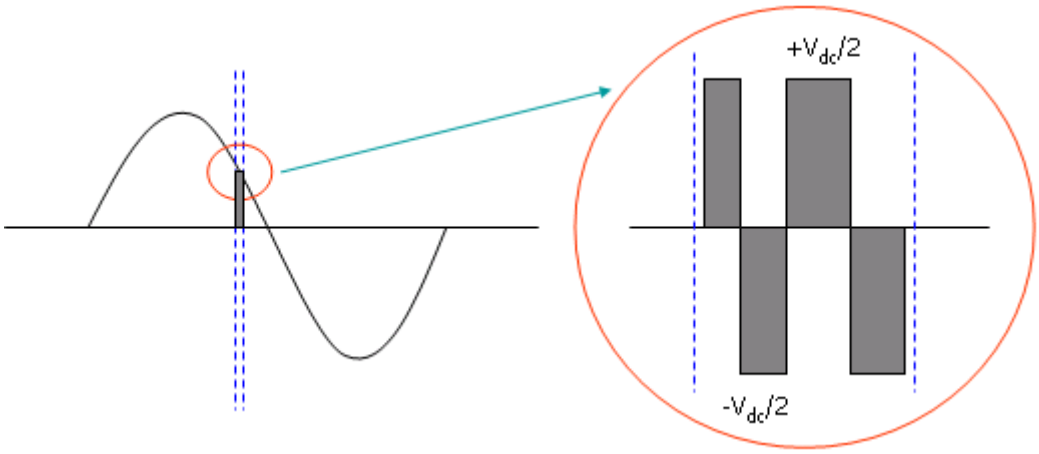

Fig.4.3. Pole voltage being generated in a time-averaged sense

Though modulation techniques help us generate the required (continuous) output voltage in a time-averaged sense, they leave voltage harmonics at switching frequency and its multiples mixed in the output voltage. This cannot be avoided. This voltage harmonics will in turn produce current harmonics in the system which will be injected at the PCC along with the compensating current. To avoid this, the system should be such that the controller-inverter setup acts as a low pass filter (with cut-off frequency of about a decade less than the switching frequency) as shown in Fig.4.4. Thus, the switching harmonics are not allowed to reach the PCC. It is to be noted that only the switching harmonics and not the harmonic currents required by the load are blocked. However, in the process of blocking the switching harmonics, we are limiting the compensation of harmonics to within a limit i.e. we can now compensate only those harmonics below the cut-off frequency of the low pass system.

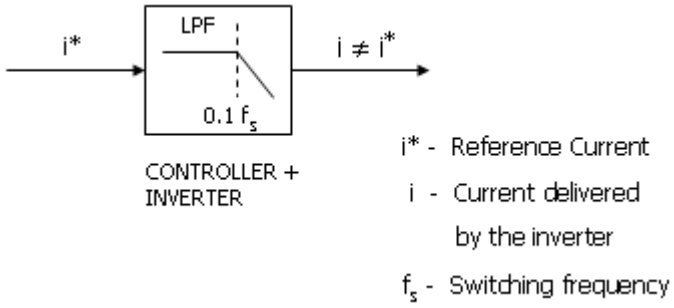

Fig.4.4. Practical controller-inverter set-up of STATCOM

The block diagram of Fig.4.4 can be represented by a familiar control system structure as shown in Fig.4.5. Now, if the transfer function of the 'plant' is found then the controller can easily be derived from that using a first or second order low pass filter transfer function for the total system (shown in dotted box). The plant transfer function is arrived at in the following sub-section and the controller transfer function will be derived in the subsequent sub-section.

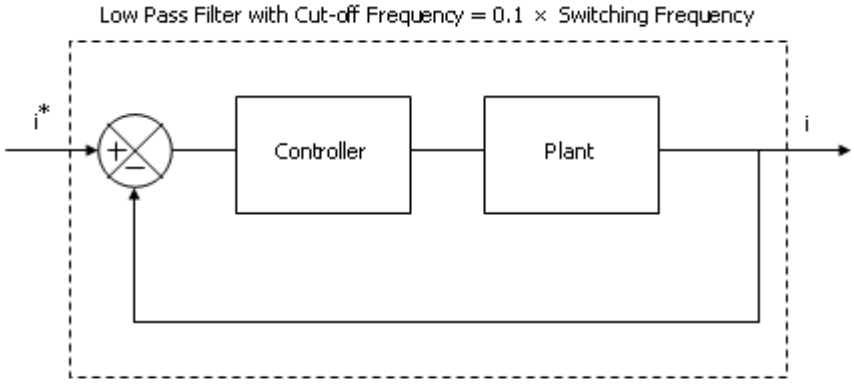

Fig.4.5. Structure of current controller

4.1.2. Derivation of plant transfer function

In the present study, Space Vector Modulation is used to control the VSI. The space vector modulation being a voltage control strategy requires voltage references for control. So, the controller's work is to convert the current references into voltage references according to the difference in the actual current

flowing at the inverter output and the current it is supposed to deliver. Once the voltage references are generated, the inverter along with the choke tries to follow the current reference.

Thus, it is clear that the inverter along with the choke must be the 'plant'. So, the transfer function of the plant can be arrived at by using the Inverter – Choke – Grid setup (R-L circuit) shown in Fig.4.6.

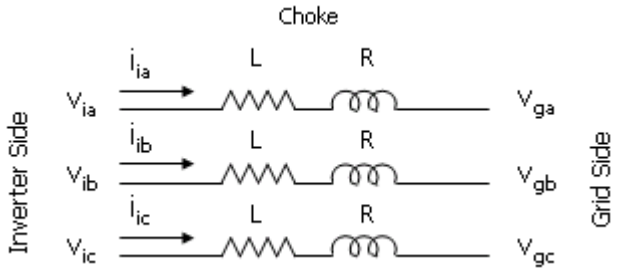

Fig.4.6. Inverter - choke - grid setup as STATCOM's plant

The symbols in Fig.4.6 can be expanded as follows,

v_{ia}, v_{ib}, v_{ic} - Inverter side instantaneous voltages (in volt)

i_{ia}, i_{ib}, i_{ic} - Inverter currents flowing through the choke (in ampere)

v_{ga}, v_{gb}, v_{gc} - Grid side instantaneous voltages (in volt)

L, R - Per phase inductance (in henry) and resistance (in ohm) of the choke

Since the current references in the SRF strategy are in the d-q plane, the equations are first written in the *R-Y-B* plane and then they are transformed to the $\alpha - \beta$ plane and subsequently to the *d-q* plane. This helps in deriving the controller transfer function in the *d-q* plane so that it can be directly used in the practical implementation. This will lead us to getting the voltage references in the *d-q* plane which should subsequently be transformed to the *R-Y-B* plane employing appropriate reverse transformations.

Applying KVL to the R-L circuit shown in Fig.4.6, we have the following equations,

$$v_{ia}(t) - v_{ga}(t) = R \cdot i_{ia}(t) + L \cdot \frac{di_{ia}(t)}{dt} \quad \text{---------- (4.1)}$$

$$v_{ib}(t) - v_{gb}(t) = R \cdot i_{ib}(t) + L \cdot \frac{di_{ib}(t)}{dt} \quad \text{---------- (4.2)}$$

$$v_{ic}(t) - v_{gc}(t) = R \cdot i_{ic}(t) + L \cdot \frac{di_{ic}(t)}{dt} \quad \text{---------- (4.3)}$$

$(4.1) \times \left(\frac{3}{2}\right)$ gives,

$$\left(\frac{3}{2}\right)v_{ia}(t) - \left(\frac{3}{2}\right)v_{ga}(t) = R \cdot \left(\frac{3}{2}\right)i_{ia}(t) + L \cdot \frac{d\left[\left(\frac{3}{2}\right)i_{ia}(t)\right]}{dt} \quad \text{---- (4.4)}$$

$(4.2) \times \left(\sqrt{\frac{3}{2}}\right)$ gives,

$$\left(\sqrt{\frac{3}{2}}\right)v_{ib}(t) - \left(\sqrt{\frac{3}{2}}\right)v_{gb}(t) = R \cdot \left(\sqrt{\frac{3}{2}}\right)i_{ib}(t) + L \cdot \frac{d\left[\left(\sqrt{\frac{3}{2}}\right)i_{ib}(t)\right]}{dt} \quad \text{---- (4.5)}$$

$(4.3) \times \left(\sqrt{\frac{3}{2}}\right)$ gives,

$$\left(\sqrt{\frac{3}{2}}\right)v_{ic}(t) - \left(\sqrt{\frac{3}{2}}\right)v_{gc}(t) = R \cdot \left(\sqrt{\frac{3}{2}}\right)i_{ic}(t) + L \cdot \frac{d\left[\left(\sqrt{\frac{3}{2}}\right)i_{ic}(t)\right]}{dt} \quad \text{---- (4.6)}$$

Referring to eqns. (3.6) and (3.11), we can transform eqns. (4.1) to (4.3) to the α-β plane using eqns. (4.4) to (4.6) as follows,

$$(4.4) \quad \Rightarrow \quad v_{i\alpha} - v_{g\alpha} = R \cdot i_{i\alpha} + L \cdot \frac{di_{i\alpha}}{dt} \quad \text{---------- (4.7)}$$

$$(4.5) - (4.6) \Rightarrow \quad v_{i\beta} - v_{i\beta} = R \cdot i_{i\beta} + L \cdot \frac{di_{i\beta}}{dt} \quad \text{---------- (4.8)}$$

Using eqns. (4.7) and (4.8) and applying the definition of space vector $(\alpha + j\beta)$, we have,

$$(4.7) + \text{j} \,.\, (4.8) \Rightarrow \quad \overline{V}_i - \overline{V}_g = R\overline{I}_i + L\frac{d\overline{I}_i}{dt} \quad \text{---------- (4.9)}$$

From eqn. (3.20),

$$(\alpha + j\beta) = (d\cos\theta - q\sin\theta) + j(d\sin\theta + q\cos\theta) = (d + jq) \cdot e^{j\theta} \quad \text{---- (4.10)}$$

Using eqn. (4.10), we can rewrite eqn. (4.9) as follows,

$$\left(v_{id} + jv_{iq}\right) \cdot e^{j\theta}$$

$$= R \cdot \left(i_{id} + ji_{iq}\right) \cdot e^{j\theta} + L\frac{d\left[\left(i_{id} + ji_{iq}\right) \cdot e^{j\theta}\right]}{dt} + \left(v_{gd} + jv_{gq}\right) \cdot e^{j\theta} \text{ - (4.11)}$$

It must be noted that eqn. (4.11) represents the plant in the α-β plane only though it contains d and q terms. The α and β components have just been expressed in terms of d and q components and the transformation to the d-q plane is still to be effected.

Now, from eqn. (3.19),

$$(d + jq) = (\alpha\cos\theta + \beta\sin\theta) + j(-\alpha\sin\theta + \beta\cos\theta) = (\alpha + j\beta) \cdot e^{-j\theta} \text{ - (4.12)}$$

From eqn. (4.12) we can understand that eqn. (4.11) when multiplied by $e^{-j\theta}$ will transform it to the d-q plane. Further, in eqn. (4.11), $\left(v_{gd} + jv_{gq}\right) = \left|v_{\alpha} + jv_{\beta}\right| = \left|\overline{V}\right|$ since the d-axis is aligned with the grid voltage space vector. Also, $\frac{d\theta}{dt} = \omega$, the fundamental radian frequency of the system. Applying these facts to eqn. (4.11), we have,

$$v_{id} = R \cdot i_{id} + L\frac{di_{id}}{dt} - \omega L \cdot i_{iq} + \left|\overline{V}\right| \qquad \text{---------- (4.13)}$$

$$v_{iq} = R \cdot i_{iq} + L\frac{di_{iq}}{dt} + \omega L \cdot i_{id} \qquad \text{---------- (4.14)}$$

The above equations can be written in a compact matrix form as,

$$\begin{bmatrix} v_{id} \\ v_{iq} \end{bmatrix} = \begin{bmatrix} R & -\omega L \\ \omega L & R \end{bmatrix} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} + \begin{bmatrix} \left|\overline{V}\right| \\ 0 \end{bmatrix} \qquad \text{---------- (4.15)}$$

Eqn. (4.15) represents a MIMO (Multiple Input Multiple Output) system. This can be implemented as a MIMO system or as two independent SISO (Single Input Single Output) systems. In the present study, the latter approach is used. To facilitate the modeling of eqn. (4.15) as two SISO systems, the following substitutions are made:

$$\begin{aligned} v_{id}' &= v_{id} + \omega L i_{iq} - \left|\overline{V}\right| \\ v_{iq}' &= v_{iq} - \omega L i_{id} \end{aligned} \qquad \text{---------- (4.16)}$$

From eqns. (4.15) and (4.16), we have,

$$\begin{bmatrix} v_{id}' \\ v_{iq}' \end{bmatrix} = \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_{id} \\ i_{iq} \end{bmatrix} \qquad \text{---------- (4.17)}$$

It is to be noted that eqn. (4.17) is used only to simplify the control. However, the actual references in the d-q plane will still be given by v_{id} and v_{iq} only. So, once we find v_{id}' and v_{iq}', we need to use them to find v_{id} and v_{iq}. This can be done using the following set of equations derived from eqn. (4.16):

$$\boxed{\begin{aligned} v_{id} &= v_{id}' - \omega L i_{iq} + |\overline{V}| \\ v_{iq} &= v_{iq}' + \omega L i_{id} \end{aligned}} \qquad \text{---------- (4.18)}$$

Eqn. (4.17) represents two SISO systems each of which are identical. Here, the d-axis SISO system alone is considered in the following explanations. The same methodology can be applied to the q-axis SISO system also.

From eqn. (4.17), $$v_{id}' = R \cdot i_{id} + L\frac{di_{id}}{dt} \qquad \text{---------- (4.19)}$$

Or in s-domain, $$\frac{I_{id}(s)}{V_{id}'(s)} = \frac{1}{(R + sL)} \qquad \text{---------- (4.20)}$$

Eqn. (4.20) can be represented in block diagram form as shown in Fig.4.7 and represents the plant of the SISO system in the d-q plane. The q-axis plant can also be derived to be the same.

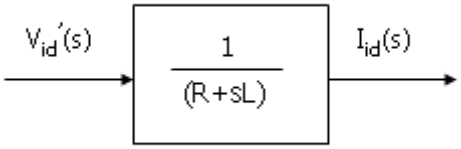

Fig.4.7. D-axis plant transfer function in d-q plane

Having arrived at the plant transfer function, let us proceed to find out the controller transfer function. Here again, the d-axis alone is considered. The same can be extended to q-axis also.

4.1.3. Determination of controller transfer function

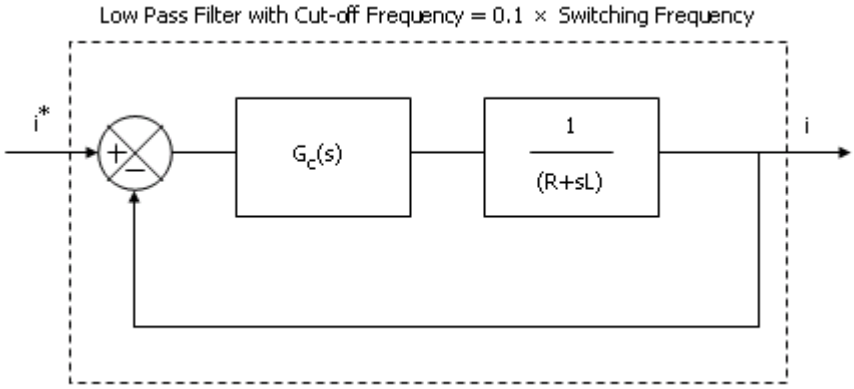

Fig.4.8. Structure of d-axis current controller with plant transfer function defined

Knowing the plant transfer function $G(s) = \frac{1}{R + sL}$, Fig.4.5 can now be redrawn as shown in Fig.4.8. Considering the overall system as a first order low pass filter for the sake of simplicity, we can write,

$$\frac{G_c(s) \cdot \left[\frac{1}{R + sL}\right]}{1 + G_c(s) \cdot \left[\frac{1}{R + sL}\right]} = \frac{1}{\tau \cdot s + 1}$$

$$\Rightarrow \frac{G_c(s) \cdot \left[\frac{1}{R + sL}\right]}{1 + G_c(s) \cdot \left[\frac{1}{R + sL}\right]} = \frac{\frac{1}{\tau \cdot s}}{1 + \frac{1}{\tau \cdot s}}$$

$$\Rightarrow \quad G_c(s) \cdot \left[\frac{1}{R + Ls}\right] = \frac{1}{\tau \cdot s}$$

$$\Rightarrow \qquad \boxed{G_c(s) = \frac{L}{\tau} + \frac{\left(R \diagup \tau\right)}{s}}$$

From the above controller transfer function, we can see that the controller is a PI controller with $\boxed{K_p = \frac{L}{\tau} \text{ and } K_i = \frac{R}{\tau}}$.

The overall current controller time constant 'τ' is related to the cut-off frequency ('ω' in radians) by the relationship $\tau = \frac{1}{\omega}$. As has been detailed earlier, the cut-off frequency is set to a decade below the switching frequency. Thus, knowing the switching frequency, the controller constants can easily be arrived at. The compensation of harmonics is possible only till the frequency 'ω' (as the higher frequencies will be attenuated), termed as the bandwidth of the system.

4.2. THE VOLTAGE CONTROLLER

4.2.1. Basic idea

Now, we shall go further and remove our earlier assumption that the DC bus voltage is constant. Then, there needs to be a voltage controller as shown in Fig.4.9.

What happens actually is that the DC bus loses some of its energy to compensate for the energy losses of the system and in this process its voltage starts to drop. As the voltage tries to drop, the voltage controller acts and maintains the DC bus voltage constant by absorbing active power from the grid. Thus, the voltage controller indirectly uses the DC bus voltage (rather than measuring the actual losses in the system) to supply the energy losses of the system from the grid.

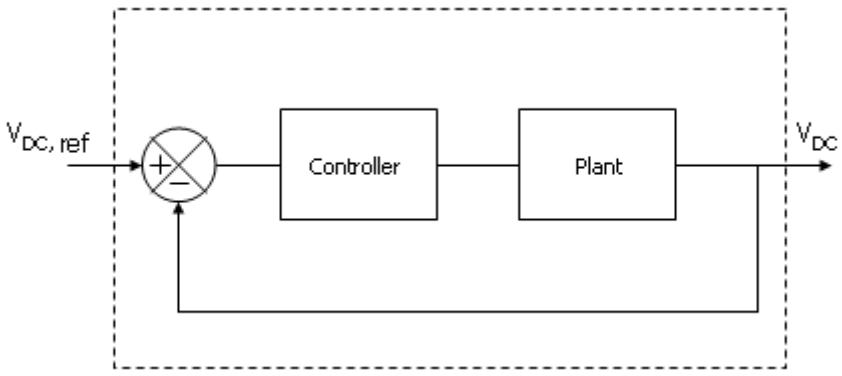

Fig.4.9. Structure of voltage controller

In Fig.4.9, the idea is to make the DC bus voltage remain constant at $V_{DC,ref}$. This implies that the total system (within the dotted lines in Fig.4.9) should resemble an all pass filter. However the parameter under consideration (DC bus voltage) being DC, the total system can be made equivalent to a low pass filter with cut-off frequency closer to Zero (so that the voltage will be almost purely DC at the DC bus). From the above discussion, we can represent the voltage control loop as shown in Fig.4.10.

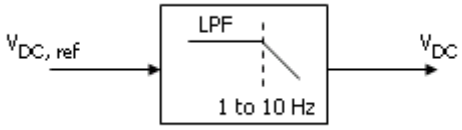

Fig.4.10. Conceptual representation of the voltage controller

From Fig.4.9 and Fig.4.10, it is clear that if the plant transfer function is known, the controller transfer function can be found easily by considering the overall transfer function of the system to be a first or second order low pass filter. The plant transfer function will be arrived at in the following sub-section and the controller transfer function will be derived in the subsequent sub-section.

4.2.2. Derivation of plant transfer function

The DC bus voltage being the output of the plant, the immediate expectation would be that the DC bus capacitor is the plant. However, the DC bus voltage is indirectly controlled by the real current flow into the system which in turn is dependent on the DC component of the d-axis current reference. So, the controller output can only be in the form of a d-axis current reference. This means that the plant cannot be a simple DC bus capacitor but it must be a system which converts the d-axis current reference into the actual DC bus voltage. The DC bus current can be related to the ac side current of the inverter. Besides that, there exists a definite relationship between the current through the capacitor and the voltage across it. Further, the ac side current of the inverter depends on STATCOM's current reference. Considering all these facts, the structure of the controller can be given as in Fig.4.11.

Here the inverter is modeled as a unity gain block since the inverter is a first order system with time constant very much less than the voltage controller time constant. Often the inner current control loop is termed as a 'faster loop' and the outer voltage control loop is termed as a 'slower loop' as the time constant (which is the reciprocal of the cut-off frequency) is much lesser for the current controller $(\omega = 2 \cdot pi \cdot 1000)$ than for the voltage controller $(\omega = 2 \cdot pi \cdot 10)$.

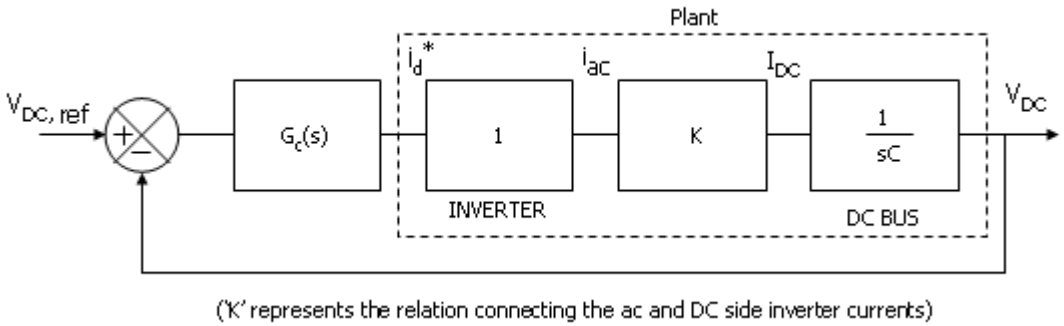

Fig.4.11. Structure of the voltage controller with plant transfer function defined

To find the plant transfer function, we ought to know 'K' which relates the ac and dc side inverter currents. Considering the power factor to be unity (as the STATCOM is used to achieve this, it is appropriate to assume so), the ac and dc side currents are related as,

$$V_{dc} \cdot I_{dc} = 3 \cdot V_{rms}(ph) \cdot I_{rms}(ph) \qquad \text{----------} \quad (4.21)$$

Since the power factor is considered to be unity, the current is aligned with the grid voltage in the ac side. This means that the ac side current in the d-q plane will be aligned with the d-axis and so q-axis component is zero.

We know,

$$\sqrt{i_d{}^2 + i_q{}^2} = \frac{3}{2} \cdot I_{\max}$$

Since q-axis component is zero, we have the relation, $I_{rms} = \frac{\sqrt{2}}{3} i_d$.

Substituting the above relation in eqn. (4.21), we have

$$K = \frac{I_{dc}}{i_d} = \sqrt{\frac{2}{3}} \cdot \frac{V_{l-l(rms)}}{V_{dc}} \qquad \text{---------- (4.22)}$$

Thus, the plant transfer function is, $\frac{\left[\sqrt{\frac{2}{3}} \cdot \frac{V_{l-l(rms)}}{C \cdot V_{dc}}\right]}{s}$. The numerator term being a constant for a designed system, let us denote it by K'. Then, the plant transfer function is $\frac{K'}{s}$, where $K' = \left[\sqrt{\frac{2}{3}} \cdot \frac{V_{l-l(rms)}}{C \cdot V_{dc}}\right]$.

4.2.3. Determination of controller transfer function

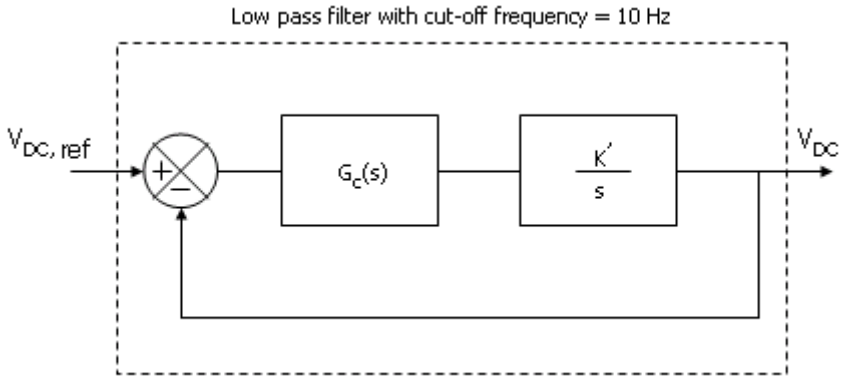

Fig.4.12. Structure of voltage controller with plant transfer function defined

Knowing the plant transfer function $G(s) = \frac{K'}{s}$, Fig.4.9 can now be redrawn as shown in Fig.4.12. Considering the overall system as a first order low pass filter for the sake of simplicity, we can write,

$$\frac{G_c(s) \cdot \left[\frac{K'}{s}\right]}{1 + G_c(s) \cdot \left[\frac{K'}{s}\right]} = \frac{1}{\tau \cdot s + 1}$$

$$\Rightarrow \quad \frac{G_c(s)\cdot\left[\frac{K'}{s}\right]}{1+G_c(s)\cdot\left[\frac{K'}{s}\right]} = \frac{\frac{1}{\tau\cdot s}}{1+\frac{1}{\tau\cdot s}}$$

$$\Rightarrow \quad G_c(s)\cdot\left[\frac{K'}{s}\right] = \frac{1}{\tau\cdot s}$$

$$\Rightarrow \quad \boxed{G_c(s) = \frac{1}{K'\cdot\tau}}$$

From the controller transfer function, we can see that the controller is a proportional controller with $K_p = \frac{1}{K'\cdot\tau}$. The overall current controller time constant 'τ' is related to the cut-off frequency ('ω' in radians) by the relationship $\tau = \frac{1}{\omega}$. As has been detailed earlier, the cut-off frequency is set near zero, say at 10 Hz. Thus, the proportional gain can easily be arrived at by calculating the system constant K'.

On substitution, the proportional gain is given by the relation,

$$\boxed{Kp = \frac{2\cdot pi\cdot 10}{\sqrt{\frac{2}{3}}\cdot\frac{V_{l-l(rms)}}{C\cdot V_{dc}}}}$$

4.3. THE COMPLETE CONTROL STRUCTURE

The complete control structure can be arrived at by combining the various results arrived at in this and the previous chapters.

The different results that are required for the development of the complete control structure are as follows:

1. The d-axis load current when high pass filtered (dc alone removed) will give the d-component of the harmonic content of the load current.
2. The q-axis load current taken as such represents the reactive content of the load current and the q-component of the harmonic content of the load current.
3. The output of the voltage controller represents the active current requirement of the STATCOM to compensate for the various losses.
4. The output of the d and q axis current controllers represent only v_{id}' and v_{iq}' respectively. To get the voltage references required for generation of the gating pulses, we need to add the feed forward terms as given by eqn. (4.18).

The complete control structure is shown in Fig.4.13. There are a few things that are to be observed. Firstly, it may be noted that there are limiters at five places. These limiters are required to make sure that the system does not exceed the designed current and voltage ratings. Next, it may be noted that in the voltage controller, the reference voltage is subtracted from the actual dc bus voltage instead of the actual dc bus voltage being subtracted from the reference voltage. This is because, in developing the current controller, it was assumed that the current flows from the inverter to the grid. This requires the current reference to be always flowing *towards the grid*. However, in the voltage controller, the active current is to be drawn from the grid which means that the current flow is *from the grid*. So, the current reference from the voltage controller should be inverted before being fed to the current controller. This has been done by changing the way the subtraction is made. Finally, it must be understood that the control structure shown here gives only v_d and v_q as the final output. These are to be transformed to the a-b-c plane to proceed with the space vector modulation technique.

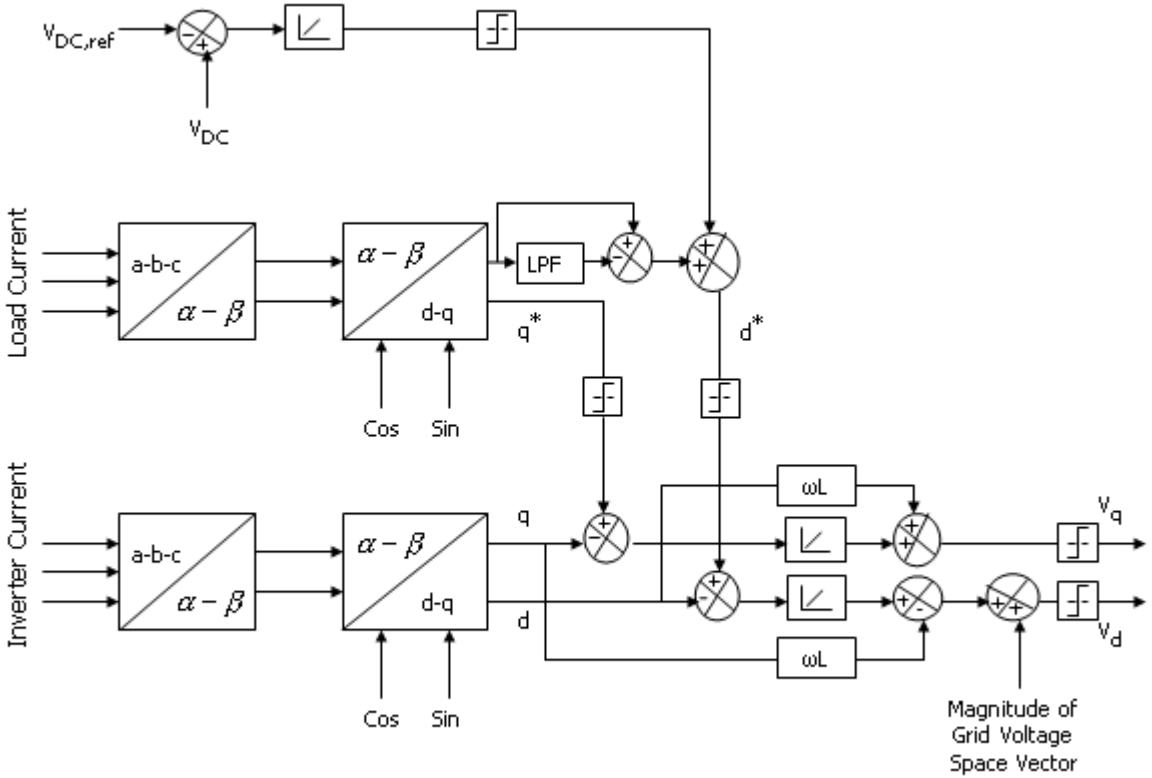

Fig.4.13. Complete control structure for reactive and harmonic current compensation

In this chapter, a detailed explanation of the current and voltage controllers of the STATCOM was given. The control equations were derived and the controller constants were arrived at. Finally, the complete control structure was developed using the various concepts developed in this and the previous chapters.

CHAPTER 5

HARDWARE DESIGN

A test set-up was developed to study how the practical implementation can be done. This chapter explains the inverter design (device, capacitor and choke selection) and gives details of the test set-up developed.

5.1. INVERTER DESIGN

The design of the inverter involves the following steps:

1. Selection of STATCOM's power rating
2. Device selection
3. DC bus capacitor selection
4. Choke selection

5.1.1. Selection of STATCOM's power rating

The STATCOM's power rating is to be decided based on the load. It is to be borne in mind that the STATCOM will be supplying only the reactive and harmonic currents. Once the power rating is decided, the maximum rms current the inverter is required to support can be calculated as:

$$\text{Power Rating (in VA)} = 3 \cdot V_{ph,rms} \cdot I_{ph,rms} \quad \text{----------} \quad (5.1)$$

Where, Vph,rms = per phase rms voltage (in volts)

Iph,rms = per phase rms current (in volts)

In the present study, the STATCOM rating was chosen as 3.5 KVA. The corresponding per phase rms current was calculated as 5A.

5.1.2. Device selection

The selection of the device is based on the following factors:

1. Maximum current flow through the device
2. Maximum voltage stress on the device during "OFF" period
3. Switching frequency required

Maximum current flow

Considering one leg of the inverter (say the left most one) shown in Fig.5.1, it may be noted that the maximum current will flow through switch S_a when S_a is closed (and S_a' is open) and will be equal to the maximum line current. The maximum line current can be found using eqn. (5.1) and bearing in mind that the line current is same as the per phase current in a three-phase three-wire system. The maximum current flow will be the same for all the devices.

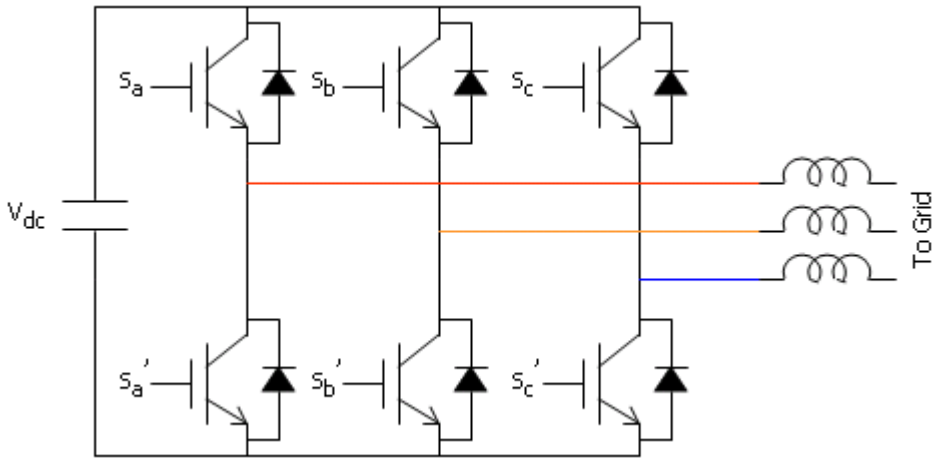

Fig.5.1. Inverter with IGBT switches and anti-parallel diodes

Maximum Voltage stress

Considering the same situation of S_a being closed and S_a' being open, the maximum voltage that is to be blocked by switch S_a' will be V_{dc}. Generally the blocking voltage is chosen slightly higher than V_{dc} so as to avoid device failure.

Switching frequency required

The aim being a composite compensation of both reactive and harmonic currents, the switching frequency should be as large as possible since the maximum harmonics that can be compensated is (0.1 x Switching Frequency) as detailed in section 4.1.1.

5.1.3. DC bus capacitor selection

The DC bus capacitor is selected based on the voltage ripple constraint. The relationship used to arrive at the capacitor value has to be derived from simulations. Considering only reactive current compensation to be done, there will be no net charging of the capacitor over one fundamental cycle. However, there will obviously be current flow through the capacitor. Choosing the peak of the line reactive current to be 4A, the current flow through the capacitor during one fundamental period was found to be as in Fig.5.2.

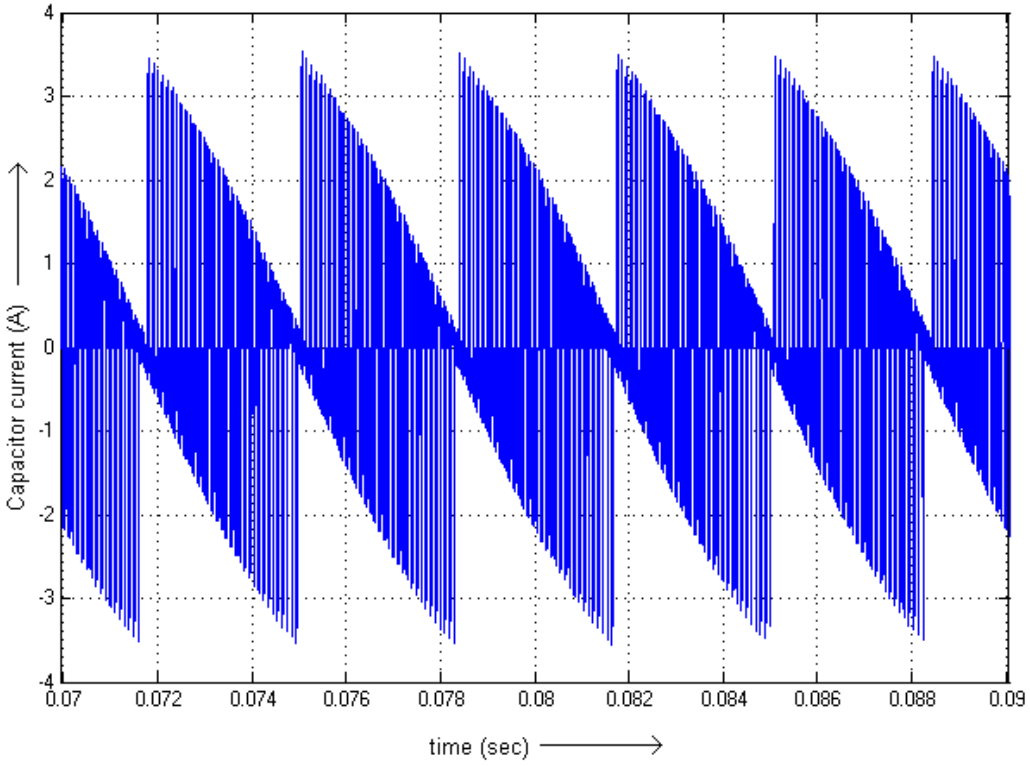

Fig.5.2. Capacitor current during one fundamental period

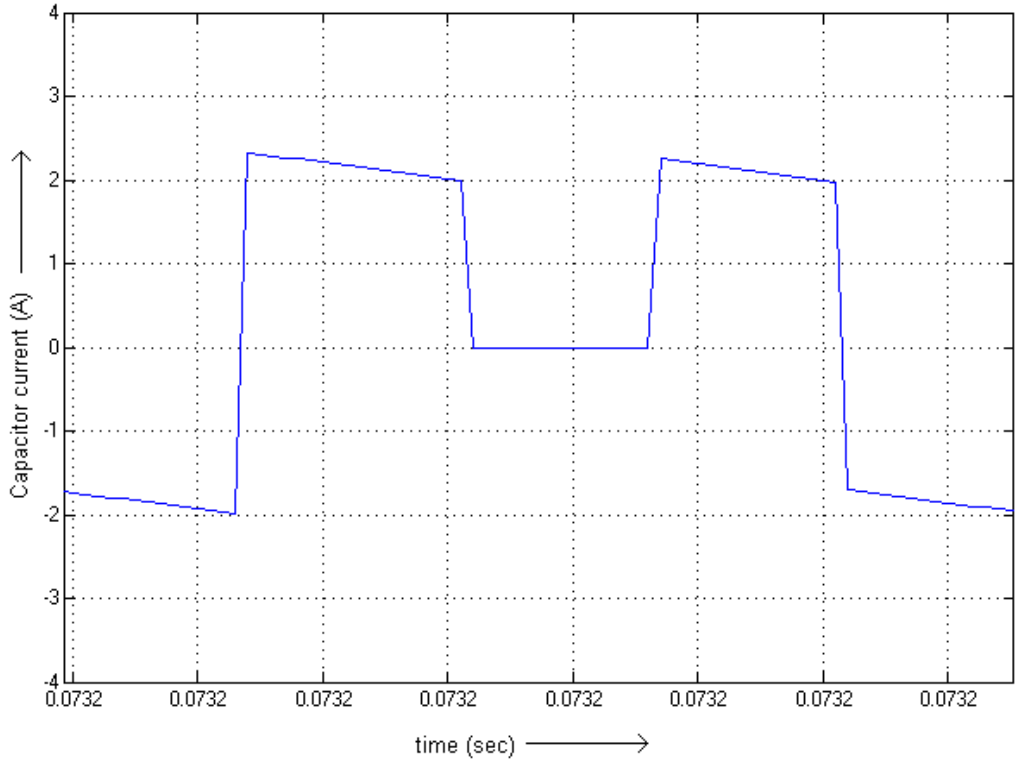

Fig.5.3. Duty cycle around middle of the capacitor current envelope

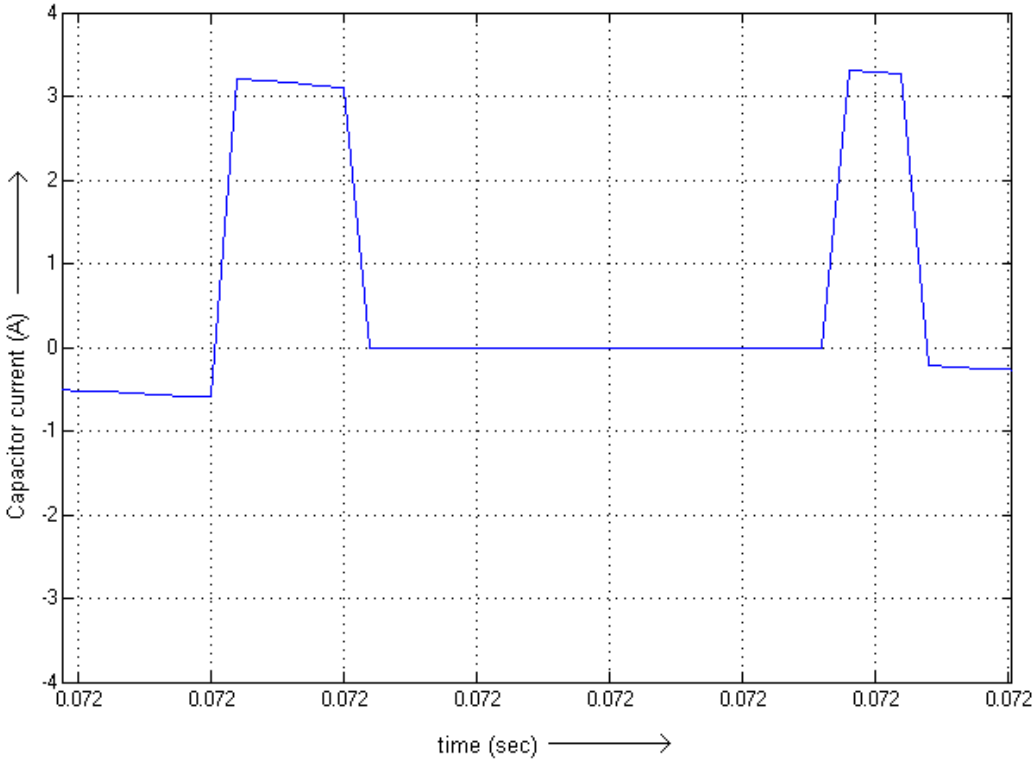

Fig.5.4. Duty cycle around peak of the capacitor current envelope

It may be noted that the capacitor current is alternating at the switching frequency. Also the envelope of the capacitor current waveform repeats at six times the fundamental frequency. A closer look at the capacitor current waveform reveals the fact that the duty cycle of the current during each switching period is dependent on the position of the switching period in the current envelope. Two samples of duty cycles at the middle and peak of the current envelope are shown in Fig.5.3 and Fig.5.4. Due to the varying duty cycle, the rms value at switching frequency will also be different at different regions along the envelope. Fig.5.5 shows the variation of the rms plot of the capacitor current (at the switching frequency).

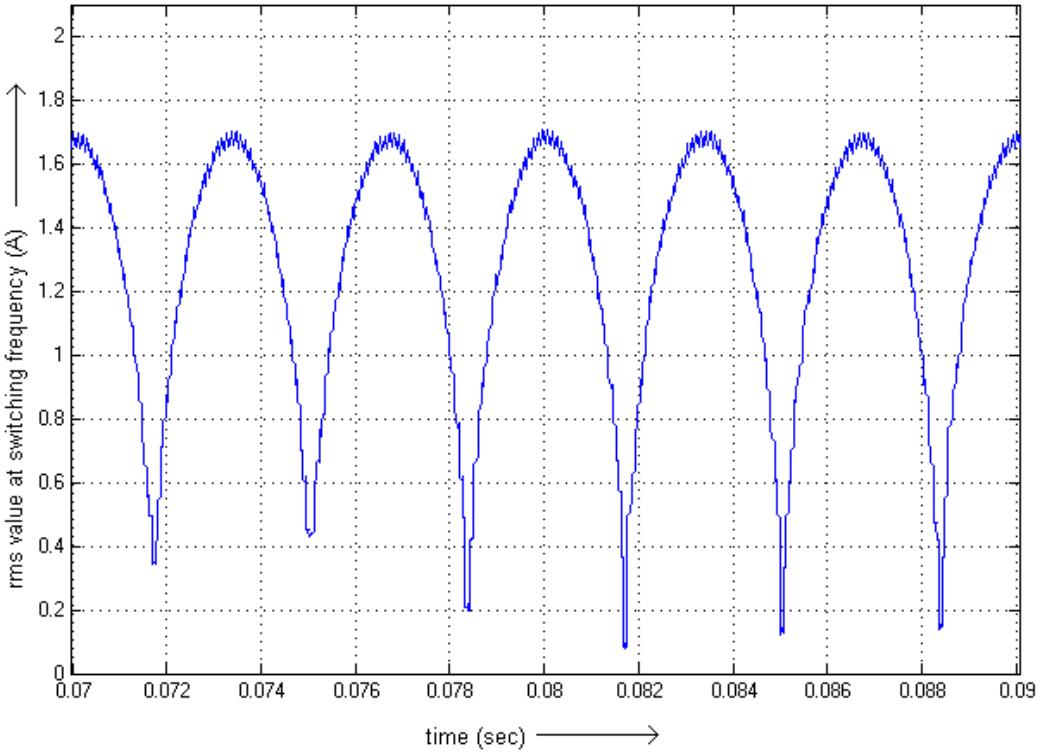

Fig.5.5. RMS value of the capacitor current (at switching frequency)

The various simulation data are as follows:

Value of fundamental reactive current (maximum)	=	4A
Peak value of the capacitor current envelope	=	3.56A
Peak value of the rms current plot (rms value)	=	1.71A

From the simulation data, the following derivation can be done:

Max. ripple current = 89% of fundamental reactive current (max)

Max. rms ripple current = 48% of peak of capacitor current envelope

So, Max. rms ripple current $= 0.48 \times 0.89 \times \sqrt{2} \times$ rms reactive current

$$\therefore I_{ripple,rms} = 0.6041 \cdot I_{reactive,rms}$$

For determining the capacitance, the worst case ripple is to be considered. Neglecting any variations in the ac side current during one switching interval, the worst case charging current will be a rectangular ac waveform whose peak equals that of the envelope. Then, the voltage ripple is related to the rms reactive current and the switching frequency as,

$$\text{Voltage Ripple} = 0.6293 \cdot \frac{I_{reactive,rms}}{f_{switching} \cdot C}$$

The voltage ripple can be assumed to be 5% or 10% of the DC Bus voltage reference and the capacitance selected from the above relation.

5.1.4. Choke selection

As a rule of thumb, a voltage drop of 20% of the grid voltage is assumed at the choke. From this, the inductance of the choke can be computed as follows:

$$\text{Voltage drop at the choke (per phase)} = (\omega L) \cdot i_{ph,rated}$$

$\Rightarrow$ 20% of rms grid voltage (per phase), $v_{drop} = (\omega L) \cdot i_{rated,rms}$

$$\Rightarrow \text{L (choke inductance per phase)} = \frac{v_{drop}}{\omega \cdot i_{rated,rms}}$$

5.2. TEST SET-UP

A test set-up was developed to study the practical implementation of a STATCOM and to know the challenges involved in the same. The rating of the STATCOM test set-up was chosen as 3.5 KVA (corresponding to a current rating of 5A rms). Appendix A gives the details of the inverter hardware components.

The test set-up was designed such that all the auxiliary circuits except for the load current sensing circuit, digital controller, choke and the load, are present in the test set-up itself. The test set-up (shown in Fig.5.6) has the following circuits:

1. IPM (Intelligent Power Module) based inverter set-up
2. Main SMPS for powering the DSP
3. Gate driver SMPS for powering the gate driver circuitry
4. Transformers and resistor divider circuitry for grid voltage sensing
5. LEMs (Hall effect transducers) for inverter current sensing
6. DC Bus voltage sensing circuit
7. SSRs for pre-charge and main contacts
8. Miscellaneous arrangements like connectors to transfer PWM signals from the digital controller to the inverter set-up, connectors to transfer sensed currents and voltages to the digital controller, transistor based pull-up circuits, power supply connectors, etc.

In this chapter, the design of the inverter was explained in detail with explanation on how the various components of the inverter hardware should be chosen. Also, an overview of the test set-up developed for hardware studies was also provided.

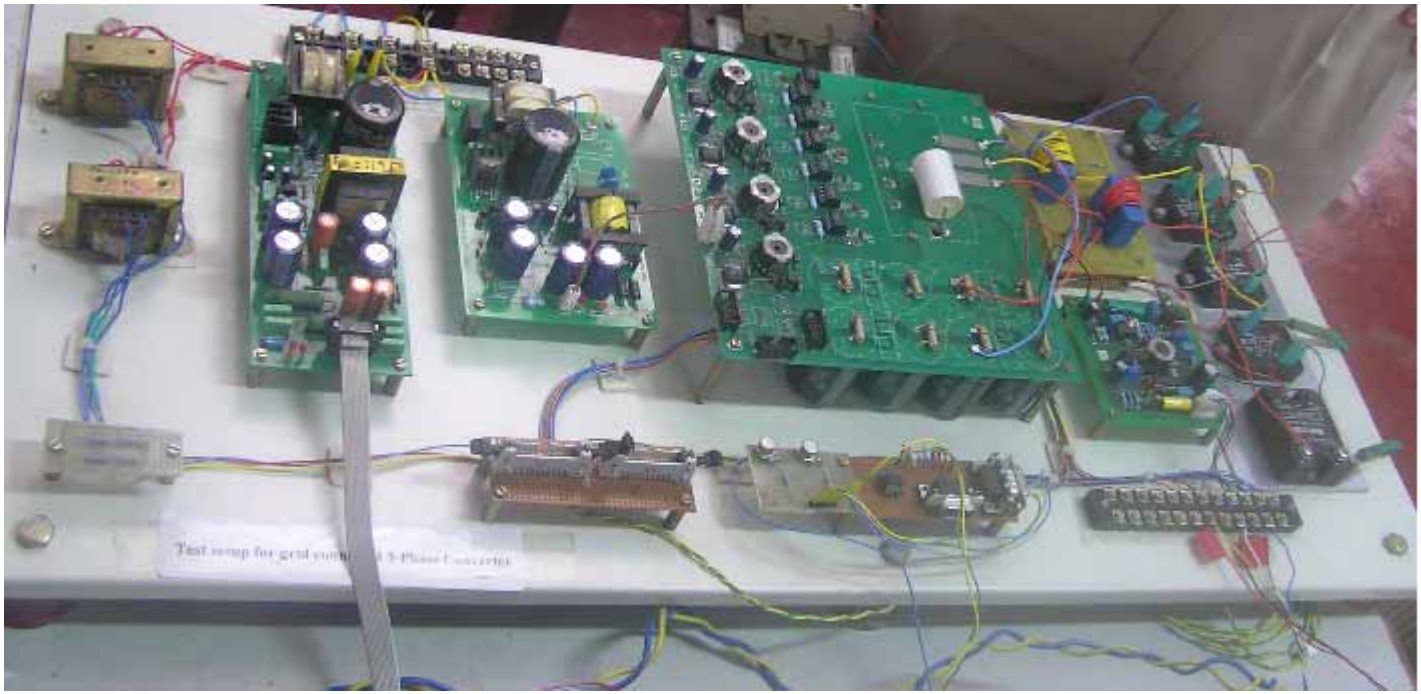

Fig.5.6. Test set-up

CHAPTER 6

IMPLEMENTATION DETAILS

Several implementation studies were carried out using the 32-bit fixed-point TMS320F2812 digital signal processor (henceforth called as 2812 DSP). This chapter discusses some of the important implementation details and explains how some of the implementation challenges can been handled.

6.1. ANTI-ALIASING FILTER

In the digital implementation, the analog signals will be sampled for further processing. The sampling process might lead to 'aliasing' – a phenomenon where different frequencies cannot be distinguished. In order to avoid aliasing, the sampled signal should be band-limited within the 'Nyquist Frequency' [9]. In the present hardware study, the sampling frequency was chosen as 10 KHz and the corresponding 'Nyquist Frequency' is 5 KHz. A simple RC low pass filter used at the input of the ADC channels limit the sensed signals to have frequency well below 5 KHz and thus acts as a simple anti-aliasing filter.

6.2. SELECTION OF Q-FORMAT

The 2812 DSP being a fixed-point processor requires the use of Q-format in calculations. In the present study, Q2.14 format is used i.e. the 16-bit data can have a range of -2 to +2 (to be more precise, slightly less that +2) only. The reason for choosing Q2.14 format rather than the popular Q1.15 format is that the maximum value involved in the equations is 1.5, which can be expressed directly in Q2.14 format unlike in Q1.15 which would require changes in the equations. Table 6.1 lists the various features of Q2.14 format representation.

Feature	Description
Bits	16-bits Integer : 2-bits Fraction : 14-bits
Value of one LSB	$\frac{4}{2^{16}} = 0.00006103515625$
Format	2's complement format
Range of values	-2 to +1.99993896484375
Format after multiplication of two Q2.14 numbers	Q4.28 format
Format after division of two Q2.14 numbers	Q16 format

Table 6.1 Features of Q2.14 fixed point format numbers

6.3. DIGITAL FILTER IMPLEMENTATION

Digital low pass filters are required at several places in the practical implementation. In the present study, *Bilinear Transformation* is used in the implementation of the digital filters. Besides being simple, bilinear transformation ensures that the left half of the s-plane is mapped into the unit circle of the z-domain. The only drawback of the bilinear transformation method is that the entire imaginary axis of the s-plane gets mapped to the circumference of the unit circle. Pre-warping is required sometimes depending on the frequencies under consideration [9]. In the present study, pre-warping was not required.

Discretization can be effected using the following simple steps:

1. Find the transfer function of the low pass filter in s-domain
2. Transfer the s-domain relation to z-domain using the substitution, $s \to \frac{2}{T} \cdot \frac{1 - Z^{-1}}{1 + Z^{-1}}$
3. Apply reverse transformation to get the difference equation and implement the same

6.4. GENERATION OF UNIT VECTORS

The generation of unit vectors is an important part of the entire implementation process as the proper synchronization of the inverter with the grid depends on the accuracy of the unit vectors generated. The use of phase-locked loops (popularly called PLLs) is the widely used method for generation of the unit vectors. But the implementation of a PLL is a computationally intensive process. So, a different methodology as detailed below can be used.

The need for a PLL is the fact that the sensed grid voltage may contain noise and harmonics in it. In the present study, a filter is used to remove the noise and the harmonics thereby avoiding a PLL. The idea is to convert the three phase grid voltage to α-β plane where both the α-component and the β-component are low pass filtered using a digital filter of cut-off frequency 50 Hz. Now, the system frequency being 50 Hz, the fundamental component suffers a phase deviation of -45^{o} and the magnitude gets multiplied by a factor of $\frac{1}{\sqrt{2}}$. Since this is a known fact, the output can be corrected for the phase shift and magnitude variation to generate the unit vectors. More accuracy is obtained by accounting for the phase deviation of the sensed grid voltages at the sensing and anti-aliasing circuits. However a slight inaccuracy does result due to the fact that the grid frequency may not be exactly 50 Hz all the time.

6.5. IMPLEMENTATION OF SPACE VECTOR MODULATION

The Space Vector Modulation was tried out in the present study as it optimally utilizes the DC bus voltage in the linear modulation range. However, the implementation of the space vector modulation technique by means of sector identification and dwelling time calculation is computationally complex. So, the space vector modulation was implemented by the conventional naturally sampled sinusoidal pwm with a special type of zero sequence component mixed to the sine references. This modified sinusoidal pwm references can be shown to be same as the space vector references [3].

The simplified method comprises of the following four steps for generation of the gating signals:

1. Find the three phase references for sinusoidal pulse width modulation (SPWM)
2. Compute the minimum of the absolute references at each instant
3. Add half the value of the reference sinusoid of minimum absolute value at each instant to all three SPWM references, as offset
4. Compare the modified SPWM references to triangular carrier wave to generate the space vector pwm (SVPWM) pulses

Fig.6.1. shows the SPWM reference, the offset and the modified SPWM reference for one phase. Though the phase voltage reference is not sinusoidal (and contains a zero sequence component), the line to line voltage will be purely sinusoidal as the zero sequence component will get cancelled in the line to line voltage.

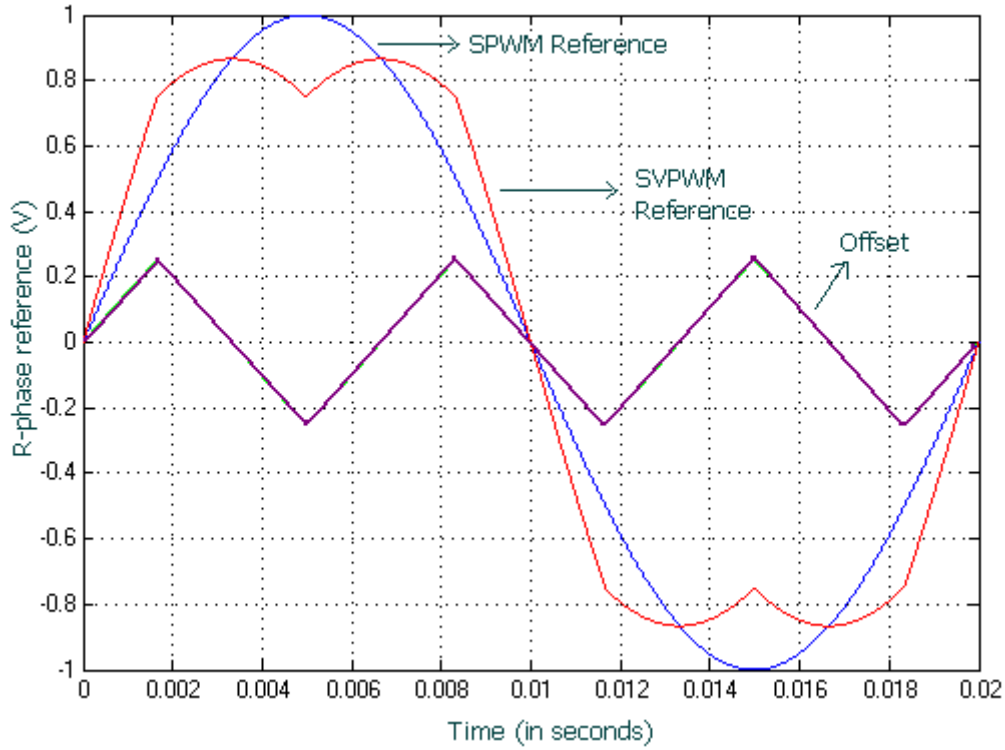

Fig.6.1. Generation of SVPWM reference signal

This chapter focused on several details of practical implementation. Details of different aspects that have to be taken care of in a digital implementation and simplified solutions to several of the implementation problems were discussed.

CHAPTER 7
RESULTS AND DISCUSSIONS

The STATCOM was simulated in MATLAB Simulink and a detailed implementation study was carried out to understand the challenges in the hardware implementation. This chapter discusses the results of simulation and hardware studies.

7.1. SIMULATION RESULTS

The simulations were used to study the following:

1. Step response of current controller
2. Step response of voltage controller
3. Reactive current compensation
4. Composite compensation of reactive and harmonic currents

7.1.1. Step response of current controller

As explained in Chapter 4, the current controller has been designed as a first order system with fast dynamic response. The step response of the STATCOM was simulated by setting the q-axis current reference to maximum positive and negative values.

Fig.7.1 and Fig.7.2 show the results obtained. As can be observed from the figures, the current controller has a good dynamic performance with a step change being tracked within around $800\mu\text{sec}$. Further, the characteristics show that the system is of first order.

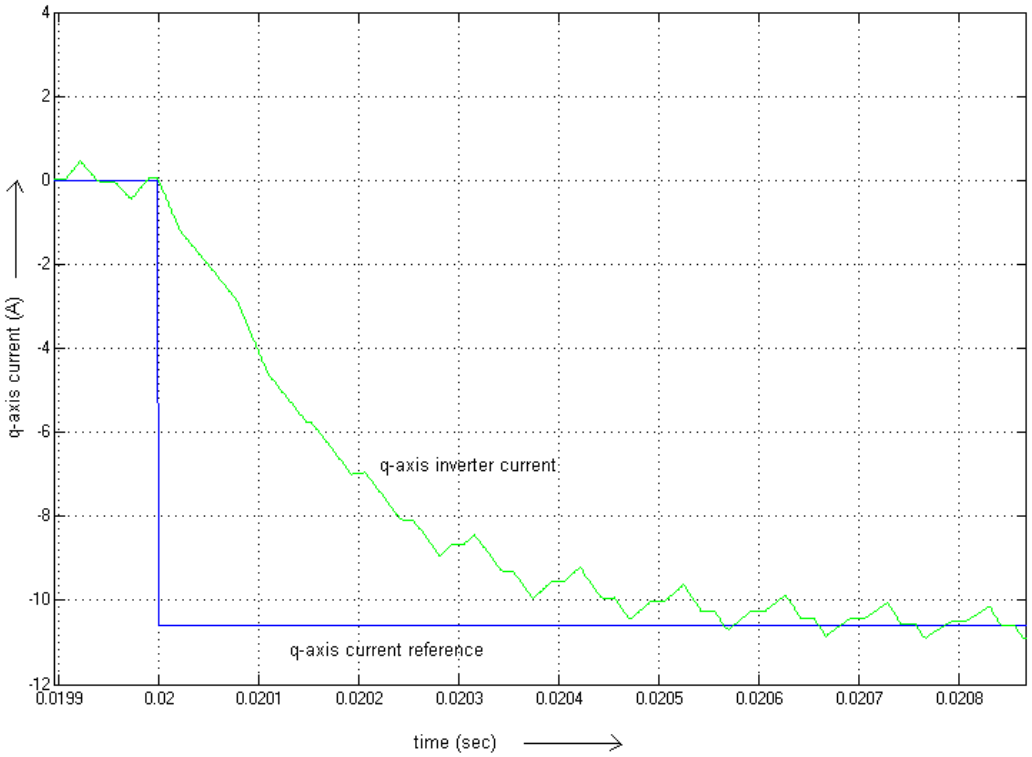

Fig.7.1. Step response of current controller for negative q-axis current reference

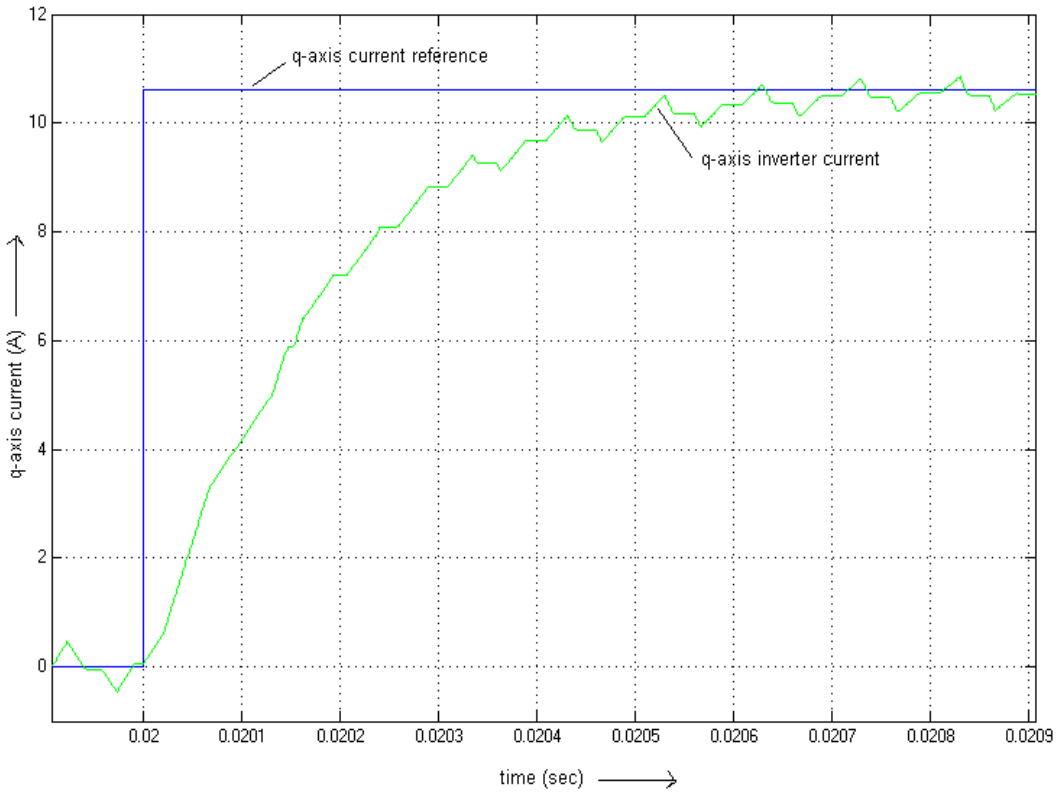

Fig.7.2. Step response of current controller for positive q-axis current reference

7.1.2. Step response of voltage controller

As has been detailed in Chapter 4, the voltage controller is also of first order. However, the voltage control loop has been designed as a slower loop compared to the current control loop. Fig.7.3 shows the step response of the voltage controller. As can be observed, the voltage controller takes about 80 milli-seconds for tracking the reference. Further, the response shows clearly that the voltage control loop is of first order.

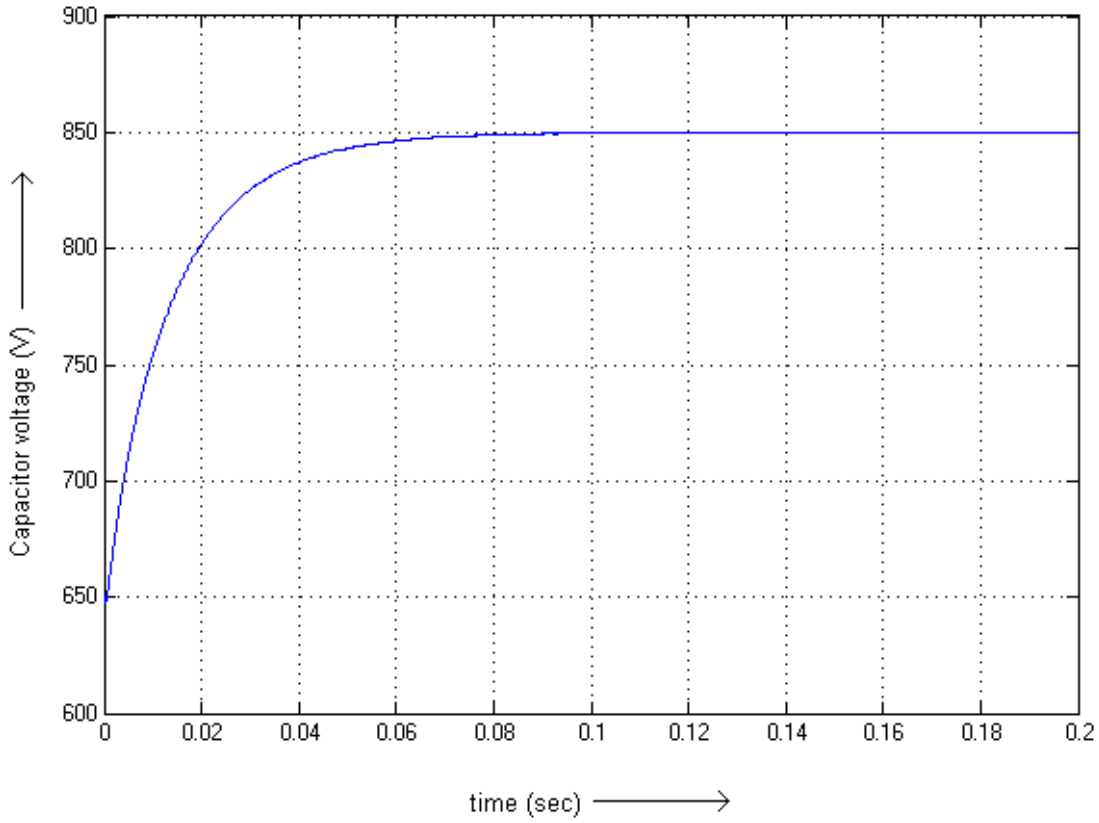

Fig.7.3. Step response of the voltage controller

7.1.3. Reactive current compensation

The reactive current compensation was studied by using loads with lagging currents. The studies revealed that the reactive current compensation gives good results with the power factor nearing unity on compensation.

Fig.7.4 shows a sample result for the following load current data:

Fundamental load current (rms)	=	4 A
Lag	=	-70^{o}
Harmonics	=	not present

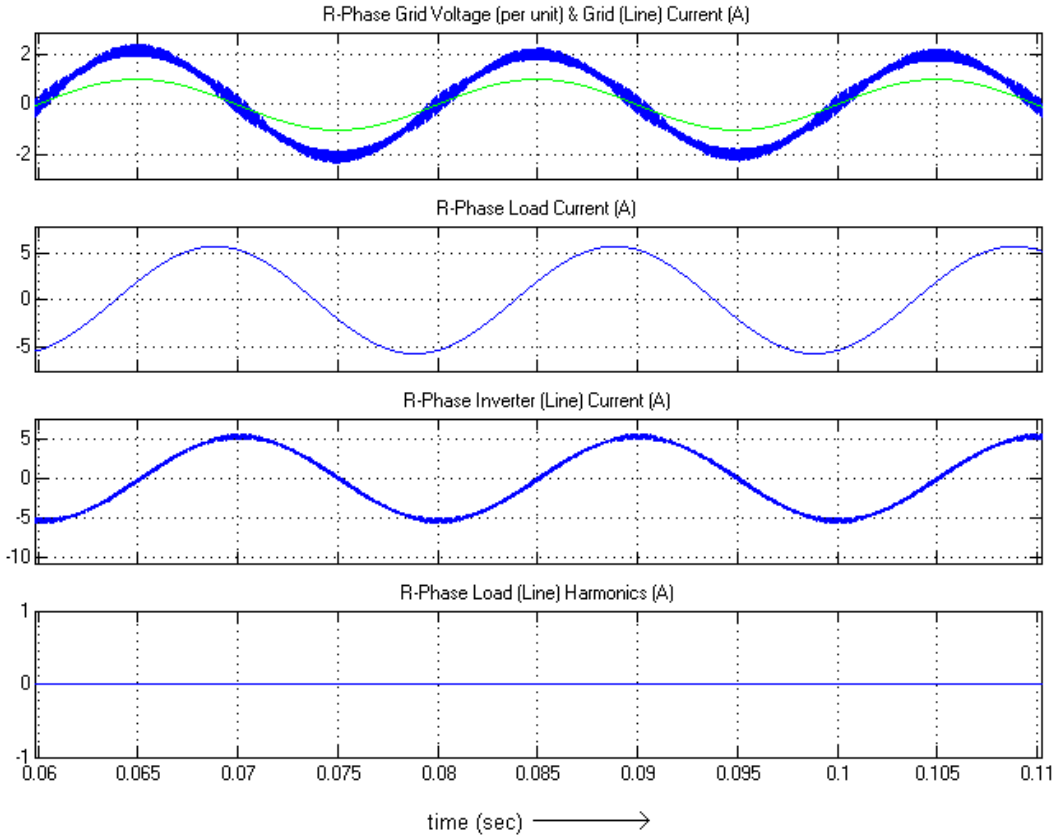

Fig.7.4. Waveforms showing purely reactive current compensation

From Fig.7.4, it can be observed that the STATCOM supplies purely reactive current so that the current drawn by the load from the grid is in phase with the voltage.

7.1.4. Composite compensation of reactive and harmonic currents

A study of composite compensation of reactive and harmonic currents showed good improvement in the THD and near unity power factor. A sample result is shown in Fig.7.5.

The load data and the THD details are as follows:

Load: 3.8A (Fundamental), 0.5A (5^{th} harmonic), 0.1A (7^{th} harmonic), 0.005A (9^{th} harmonic), 0.001A (11^{th} harmonic), 0.0005A (15^{th} harmonic), 0.0001A (17^{th} harmonic)

THD: Improved from 13.4% to 4.6% on compensation

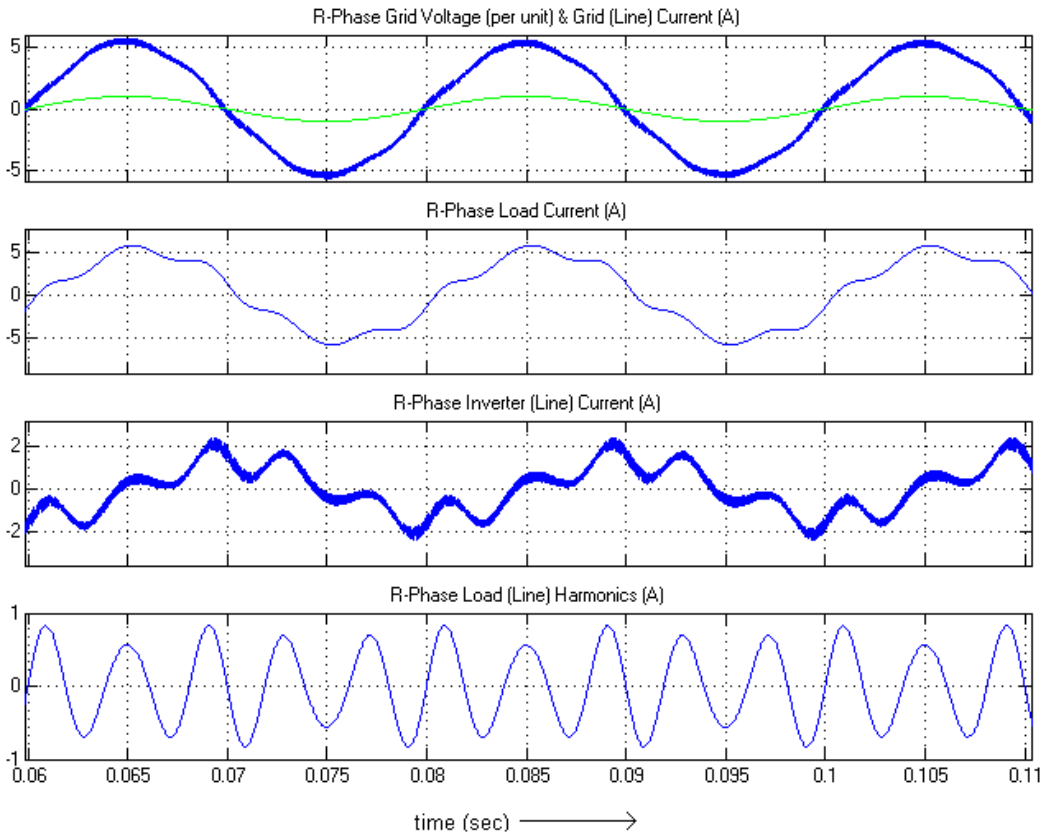

Fig.7.5. Waveforms showing compensation of reactive and harmonic currents

7.2. HARDWARE RESULTS

Some of the results obtained from hardware studies are as follows:

1. Unit vectors
2. Space vector modulation reference and inverter output

7.2.1. Unit Vectors

Fig.7.6 shows the cos and sine unit vectors required for STATCOM implementation. Fig.7.7 shows the Lissajous' curve for the unit vectors. Since the frequency is 50 Hz, the Lissajous' curve which should have appeared as a moving dot, appears as a circle.

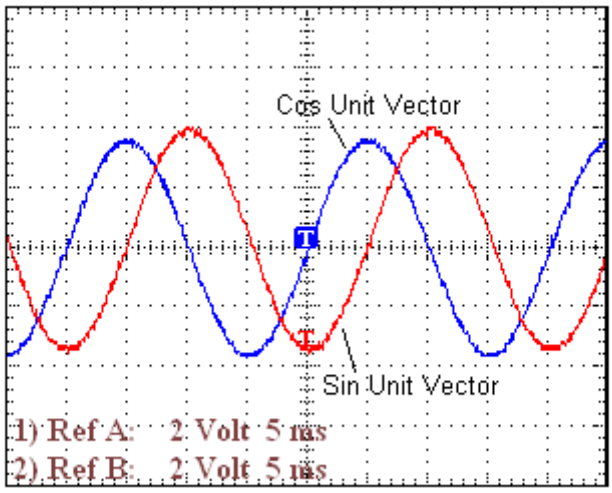

Fig.7.6. Cos and sine unit vectors

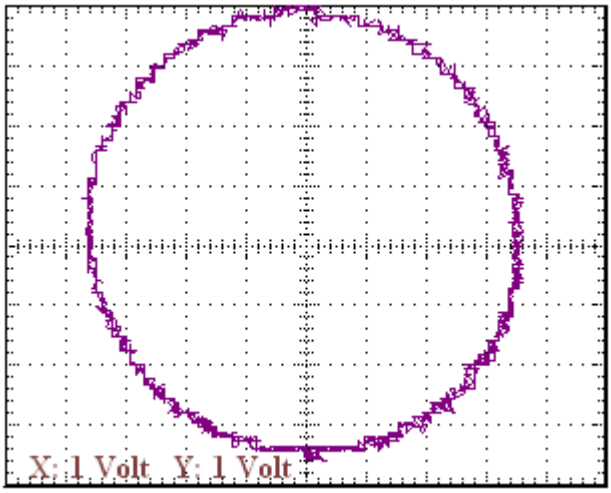

Fig.7.7. Lissajous' curve for the unit vectors

7.2.2. Space vector modulation reference and inverter output

As has been detailed in section 6.5, SVPWM reference has been generated from the SPWM reference. Fig.7.8 shows the space vector modulation reference along with the sinusoidal pulse width modulation reference. This may be compared with the simulated waveform shown in section 6.5.

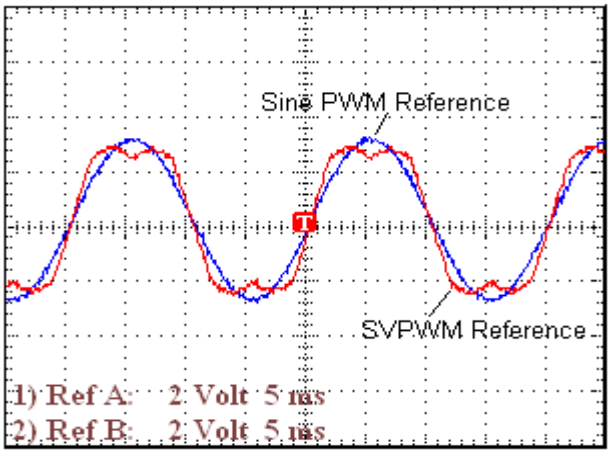

Fig.7.8. SVPWM reference

The inverter was tested with a choke modified as a star-connected purely inductive load by shorting one end of the choke. The choke being almost purely inductive should draw an almost purely inductive current. Fig.7.9 shows the result obtained. The result can be seen to match with the expected output.

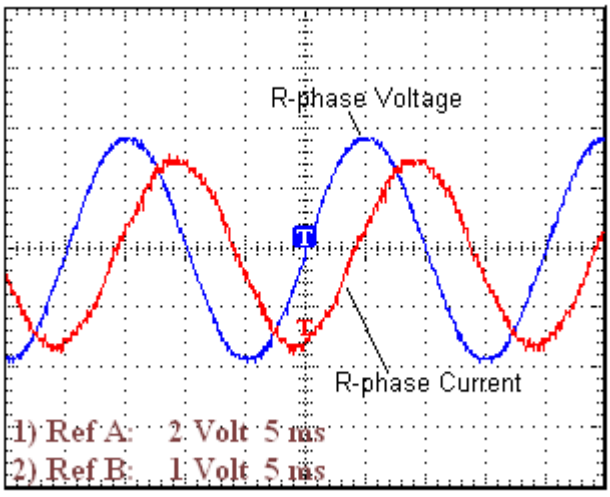

Fig.7.9. Inverter phase voltage and line current for inductive load

In this chapter the various results obtained from simulation of the STATCOM in MATLAB was given. Also, the results obtained from the several hardware tests conducted with the aim of understanding the implementation challenges was detailed.

CHAPTER 8

CONCLUSIONS

The basic principle and controller design of a STATCOM was studied in detail in the present work. The simulation studies helped in understanding the principles involved in STATCOM development while the hardware studies revealed several implementation challenges. This chapter gives a gist of the complete work and provides inputs for possible future studies in this area.

8.1. THE PRESENT STUDY

In the present study, the Synchronous Reference Frame based STATCOM was simulated and the results studied. The study shows that the system gives good dynamic performance under varying load conditions. Whereas the reactive current compensation gives highly favourable results, the harmonic performance depends largely on the load. Harmonics may not be completely compensated owing to the limitations posed by the inverter which can produce voltages only in a time-averaged sense. On the implementation side, the studies done showed several aspects. Firstly, the proper generation of the unit vectors is important as it is what helps in the synchronization of the inverter with the grid. Secondly, it could be understood that proper scaling is required to avoid errors in the computations. Thirdly, on the hardware front, due importance has to be given for protection circuitry as the STATCOM system is to be connected to the grid. Protection should be given through the software also. Further, proper testing techniques should be devised for testing the system to avoid any failure. Also, it was understood that any small hardware defect like current / voltage sensing failure or software errors like improper sequencing of actions may result in the failure of the complete system.

8.2. SCOPE FOR FUTURE WORK

Further work on STATCOM can be aimed at improving the speed of response, implementing improved inverter techniques, trying out more improved compensation techniques and the like. Some possible things that can be done are listed here.

Firstly, the current reference generation can be improved by using delay compensation techniques. Also, some techniques like predictive approach for current reference generation may be studied [6]. Secondly, changes can be brought about in the implementation of the controller so as to speed up the response time. The system may be modeled as a second order system and the responses can be studied. Finally, the inverter topology may also be changed. Three-level inverters may be studied. Thus, STATCOM is an area where there is a wider scope for further studies.

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APPENDIX – A

HARDWARE - COMPONENT DETAILS

A.1. IPM DETAILS

Part Number	:	PM15CZF120
Manufacturer	:	Mitsubishi Electric, Japan
Rating	:	1200 V, 15 A
Switching freq:		upto 15 KHz
Deadband reqd:		> 3 micro-sec
Features	:	Inbuilt gate driver, fault output for over-voltage, under-voltage, over current and temperature faults

A.2. CAPACITOR DETAILS

Manufacturer	:	Epcos
Voltage rating	:	450 V
Capacitance	:	330 micro-farad

A.3. CHOKE DETAILS

Current rating	:	50 A
Inductance	:	13 milli-henry

A.4. CURRENT TRANSDUCER DETAILS

Manufacturer	:	LEM
Part Number	:	LA100P
Ratings	:	100 A / 50 mA conversion ratio