EE2001 - Digital systems lab
Critical paths and maximum frequency of operation

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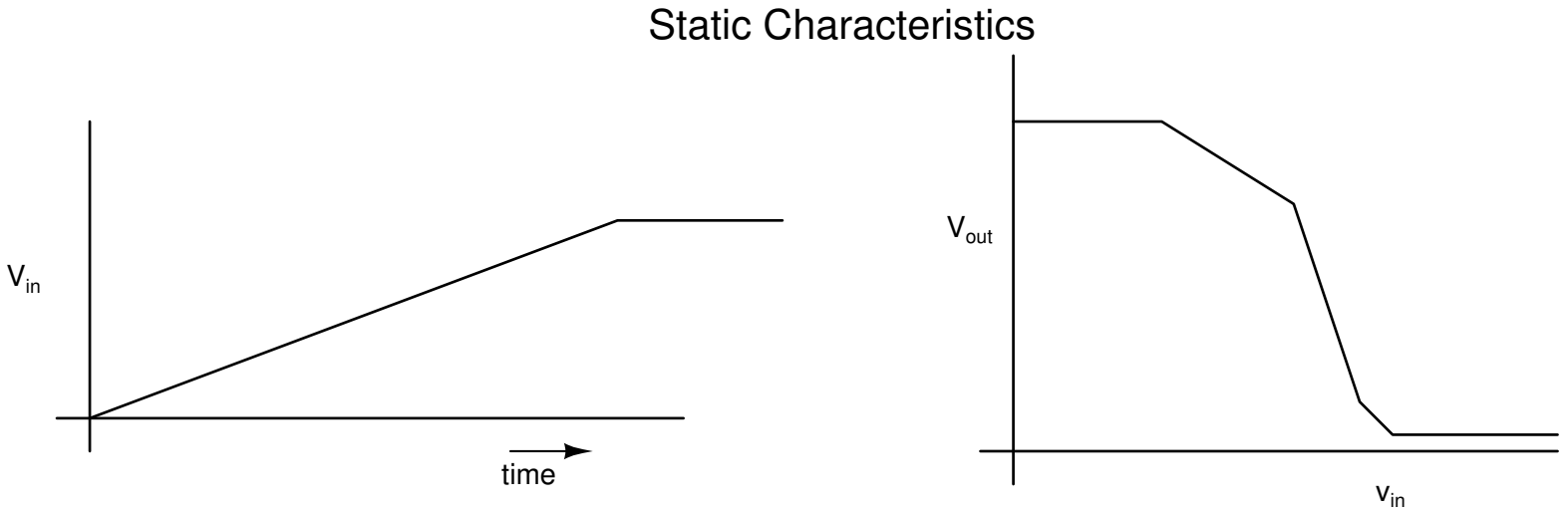
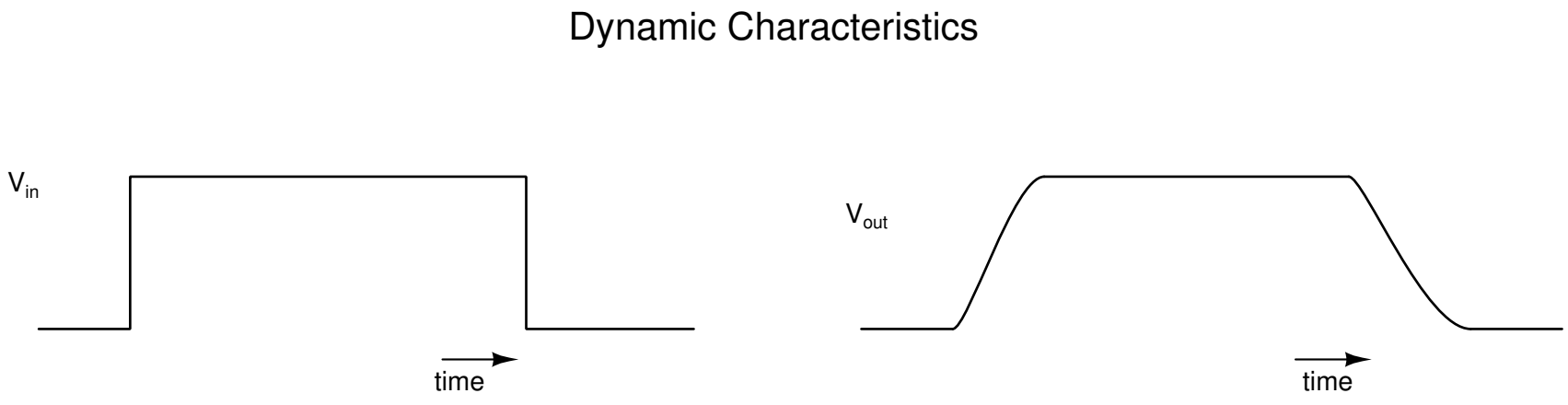
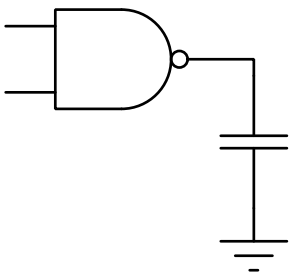
- Functional simulation - Verilog/C
- Timing analysis - Critical paths

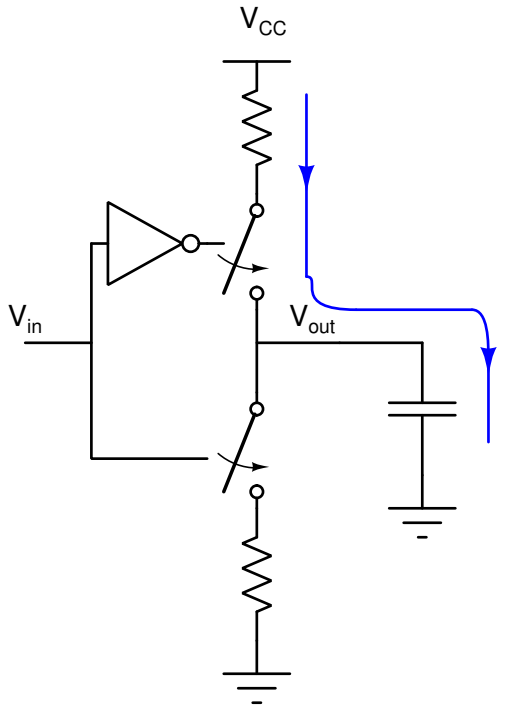
Static and dynamic behaviour





Propagation delays

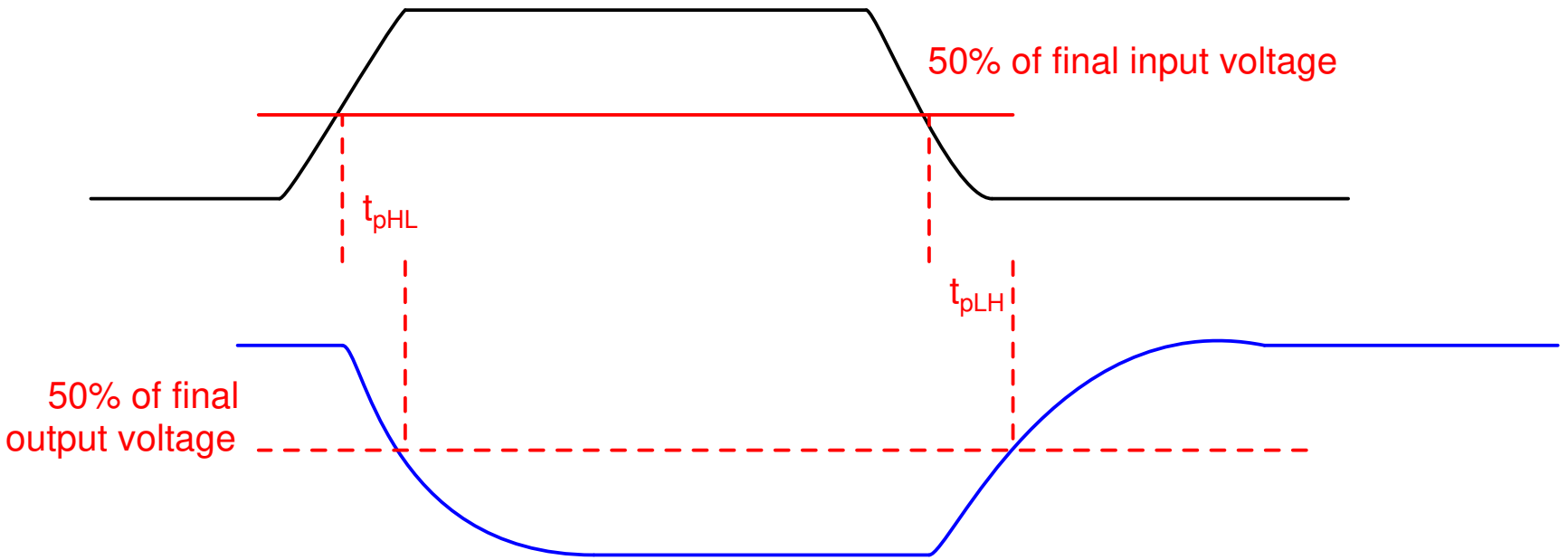




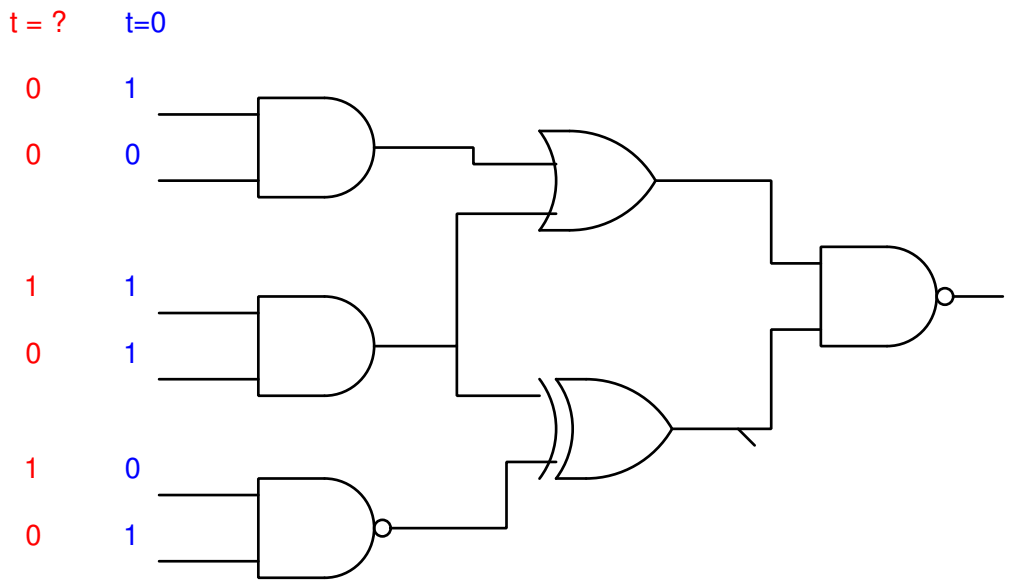
Due to

- Delays in turning transistors ON/OFF.
- Charging and discharging capacitors (wiring/parasitic/input capacitances of transistors and gates).

Propagation delays

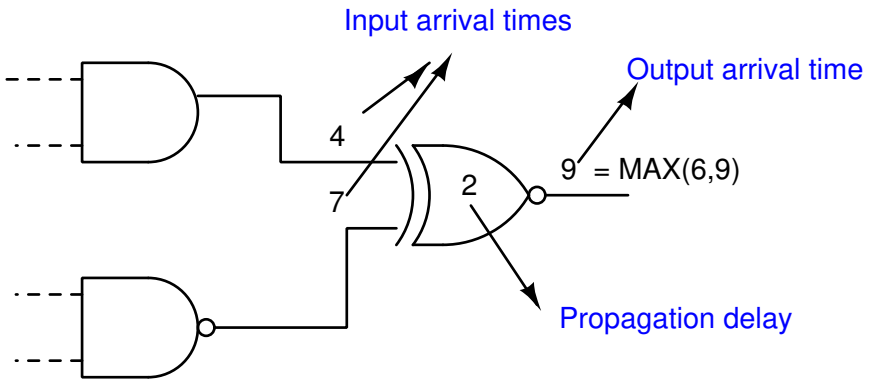


$$t_{pd} = \frac{t_{pHL} + t_{pLH}}{2}$$



Finite delay between arrival of inputs and arrival of outputs. How quickly can the inputs change?

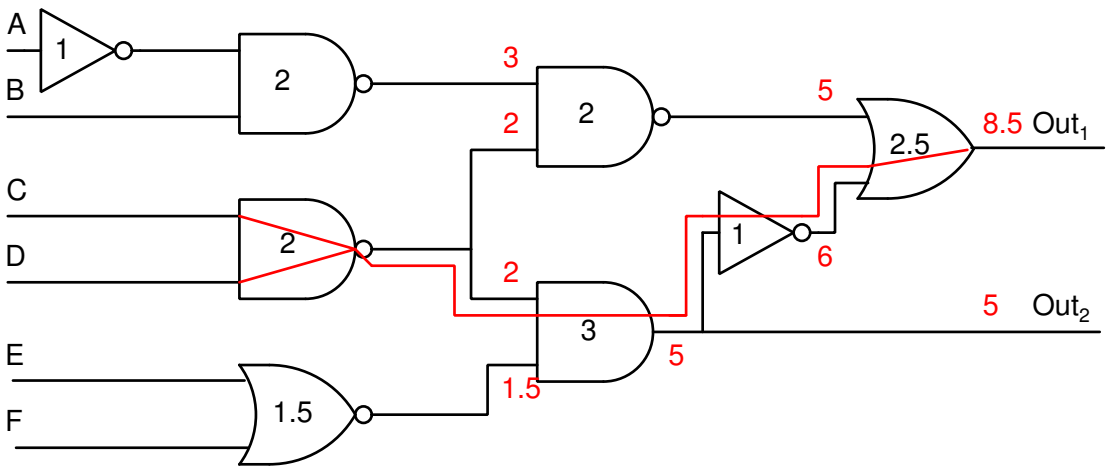
Static timing analysis

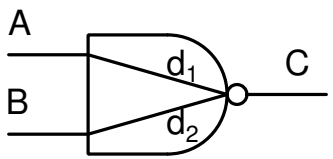


- Inputs to a gate can arrive at arbitrary times. Arrival depends on all the gate preceeding it.
- Delays are input dependent. Take the worst case delay
- Separate function from timing.
- Longest path problem in a graph. Use SUM and MAX.

Critical paths - Static timing analysis

All primary inputs available at t=0.





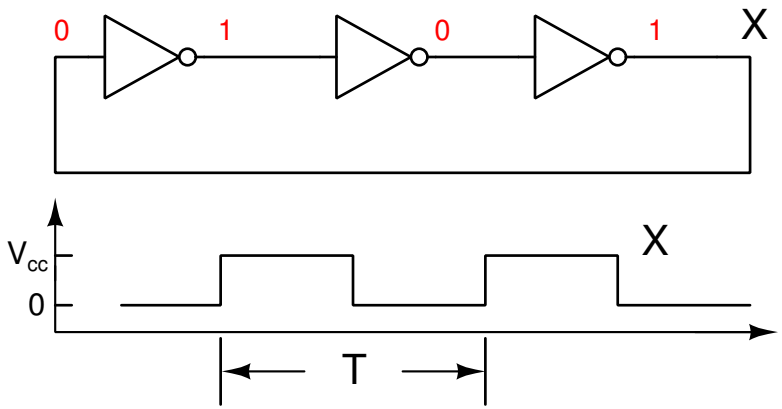
Gate delay = MAX(d_1, d_2)

The next set of inputs must arrive at t $>$ 8.5 units.

Measured propagation delays - Test structures

Due to manufacturing variations, delays vary greatly from circuit to circuit. Measure on-chip delays.

Ring Oscillator

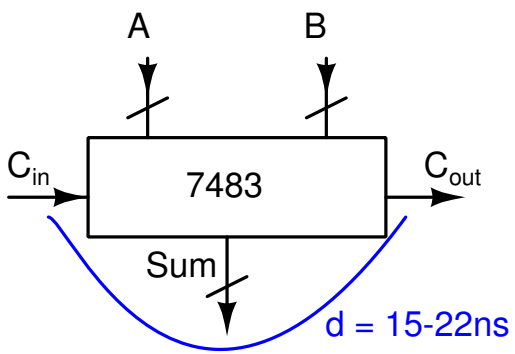


- After 3 propogation delays (t_{pd}), voltage at X goes from V_{OL} (logic 0) to V_{OH} (logic 1)
- View the signal X on the oscilloscope and measure the frequency.
- $3t_{pd} = \frac{T}{2}$

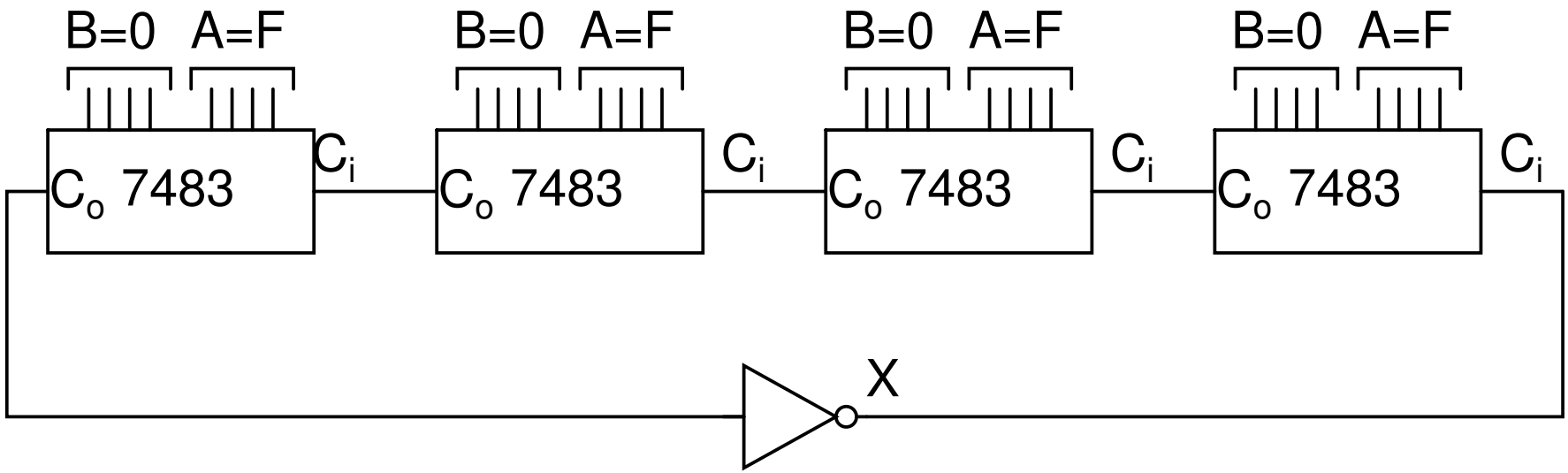
7483 - Carry lookahead adder

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to any Σ Output		16 15	24 24	ns	V_{CC} = 5.0 V C_L = 15 pF Figures 1 and 2
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to Σ Outputs		15 15	24 24	ns	
t_{PLH} t_{PHL}	Propagation Delay, C_0 Input to C_4 Output		11 15	17 22	ns	
t_{PLH} t_{PHL}	Propagation Delay, Any A or B Input to C_4 Output		11 12	17 17	ns	



Propogation delay of the adder



- In an adder chain, the last input to arrive is usually the carry input.
- The critical path is the carry path.

Experiment 7

- Learn how to use the oscilloscope - TAs will give a demo
- Wire up the ring oscillator using inverters and measure the oscillation frequency. If you cannot measure it, increase the (odd) number of inverters in the loop. Estimate the propogation delay.
- Connect four 4-bit adders (7483) and an inverter so that it oscillates. Estimate the propogation delay of the 7483.
- Using XOR and AND gates design a multiplier that multiplies two 2 bit numbers. Identify the critical path and measure the critical path delay.

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