

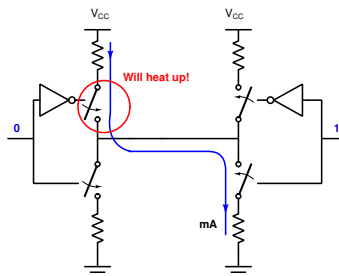
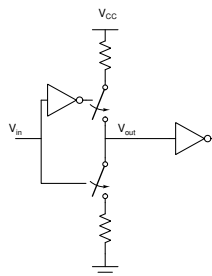
EE2001 - Digital systems lab

Open Collector gates

Vinita Vasudevan



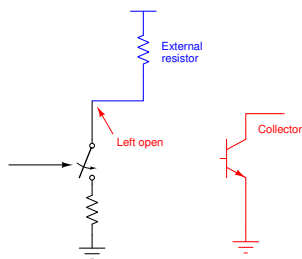
Model of a gate



When output is high, typical current $400\mu\text{A}$. The current is 10s of mA when output is low. In the worst case, could destroy one of the switches if outputs are connected together. Voltage could be at an intermediate level and cannot be interpreted as a 0 or 1.

Should make sure only one gate drives a bus as any given time.

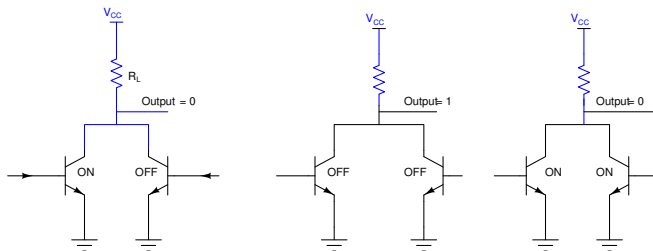
Open Collector gates



- ▶ If the switch is closed, the output is low
- ▶ Actually there is a transistor with the collector terminal left open. If the input is such that the transistor is OFF (open switch), the output is high. Otherwise it is low.

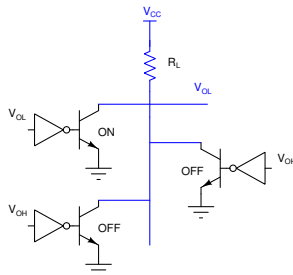
The transistor can typically sink a lot more currents than the conventional TTL output. Used to drive displays, for eg. 7447 is open collector.

Open Collector gates - Wired AND



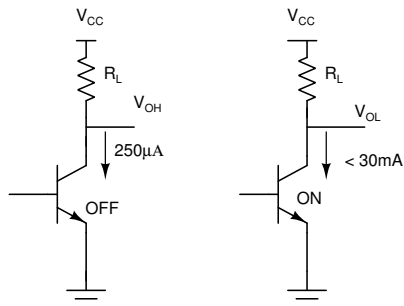
Driving a bus

Use the wired AND property of open collector gates to drive the bus.



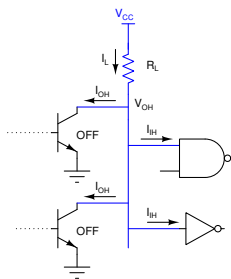
Open collector buffers: One of the inputs drives the bus. The input to all other gates should be adjusted so that the corresponding outputs are high (i.e. turn OFF the output transistors).

Practical gates



Note the current direction is into the gate for both output high and low voltages. The value of the resistor should be adjusted so that we get valid high and low voltages.

Sizing the external resistor



$$\begin{aligned}
 V_{OH} &\geq V_{OH,min} \\
 \Rightarrow V_{CC} - I_L R_L &\geq V_{OH,min} \\
 \Rightarrow R_L &\leq \frac{(V_{CC} - V_{OH,min})}{I_L}
 \end{aligned}$$

$$I_L = N_{OC} I_{OH} + N_F I_{IH}$$

where,

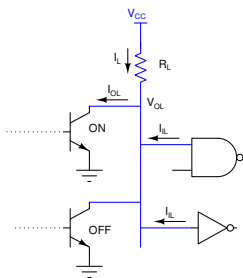
$$I_{OH} = 250\mu A, I_{IH} = 40\mu A$$

N_{OC} : Number of open collector gates

N_F : Number of fanout gates.

Sizing the external resistor

Need to size R_L so that we get an acceptable low ($\leq V_{OL}$) and high ($\geq V_{OH}$) voltage.



$$V_{CC} - I_L R_L \leq V_{OL,max}$$

$$\Rightarrow R_L \geq \frac{(V_{CC} - V_{OL,max})}{I_L}$$

$$I_L = I_{OL} - N_F I_{IL}$$

where,

$$I_{OL} = 16mA \text{ and } I_{IL} = 1.6mA.$$

OPen collector versus tristate gates

- ▶ Open collector gates can handle larger currents. Tristate gates do not require multiple resistors.
- ▶ Select inputs must be mutually exclusive, otherwise you can get indeterminate output voltages. If the resistor is sized correctly, you will always get a valid high/low voltage.
- ▶ Open collector gates can replace AND gates in positive true logic (OR in negative TRUE logic).

Experiment 7

- ▶ Using LEDs verify the wired AND property of open collector gates.
- ▶ Given two 4 bit inputs A and B, design a circuit that has output = $\text{MAX}(A,B)$ using open collector buffers (7407). Please share.

You can use a magnitude comparator (7485) and any other gates required. Use LEDs or seven segment displays to display the output.