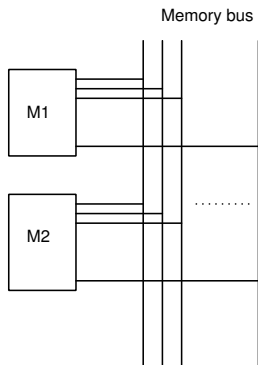


EE2001 - Digital systems lab

Tristate gates

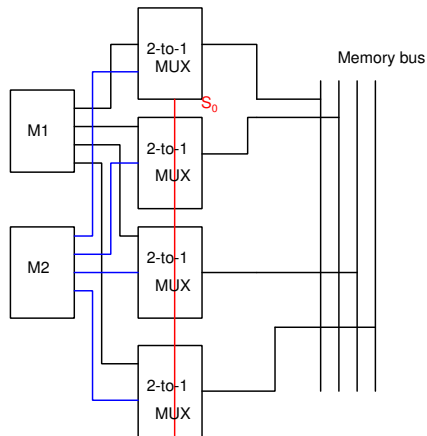
Vinita Vasudevan





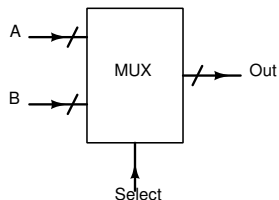
- ▶ Multiple devices connected to a single bus - eg. Memory
- ▶ Can we connect outputs of TTL gates?

Use a MUX



Can use several 2-to-1 MUXes to route one of the inputs to the output.

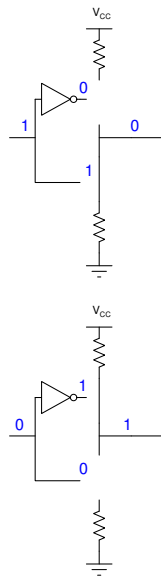
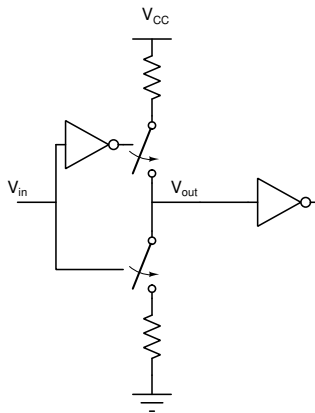
Solution with a MUX



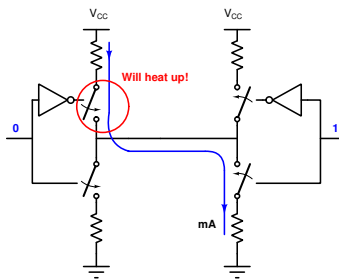
The number of MUXes needed is equal to the number of output lines. Larger the number of memory modules, larger the size of the individual MUXes (if you have 4 memory modules instead of 2, you need 4-to-1 MUXes).

Need to reduce the number of ICs.

Model for a gate



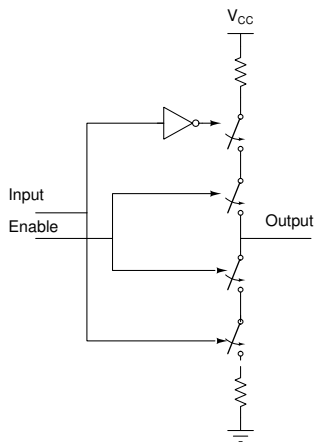
Why not connect outputs?



When output is high, typical current $400\mu\text{A}$. The current is 10s of mA when output is low. In the worst case, could destroy one of the switches if outputs are connected together. Voltage could be at an intermediate level and cannot be interpreted as a 0 or 1.

Should make sure only one gate drives a bus as any given time.

Tristate gates



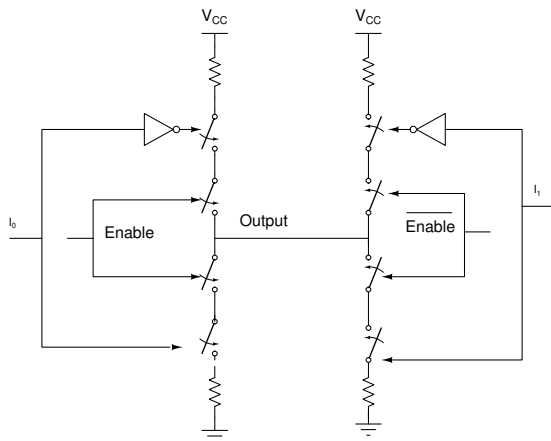
Truth Table of Tristatable Inverter

Enable	Input	Output
0	X	Z
1	0	1
1	1	0

X: Dont care

Z: Tristate

Output is an open circuit when Enable = 0.



Can connect multiple gates to a common bus and enable only one at a time

Experiment 6

Given two 4 bit inputs A and B, design a circuit that has output = $\text{MAX}(A,B)$ using

- ▶ 2-to-1 MUXes
- ▶ Tristate buffers (74245). Please share if you have only one of these.

You can use a magnitude comparator (7485) and any other gates required. Use seven segment displays to display the output.