EE2001 - Digital systems lab

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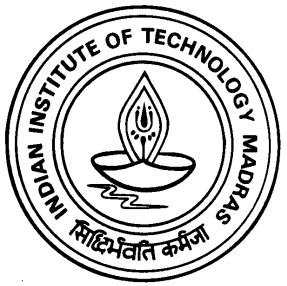


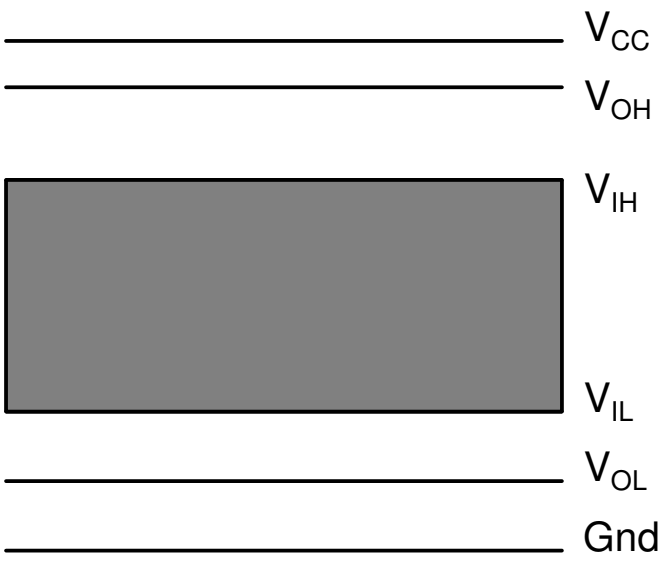
Objectives

- Practical aspects of digital design - Augment the theory course
- In the theory course - study gates at functions/logic level.
- Logic '0' and '1' are represented by voltages. Components have nonzero input and output currents.
- Each component has a datasheet detailing input and output behaviour.
- How do you design using these datasheets?

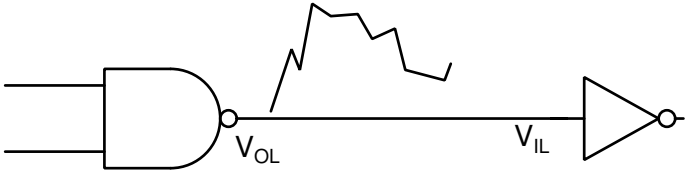
Practical aspects

- What is the range of voltages representing a logic high and low?
- What is the maximum number of gates that can be connected to the output of a gate? (Fanout)
- Propogation delay
- Power consumed

Range of voltages corresponding to logic high and low levels - different for different logic families. You will be using TTL or LSTTL gates.

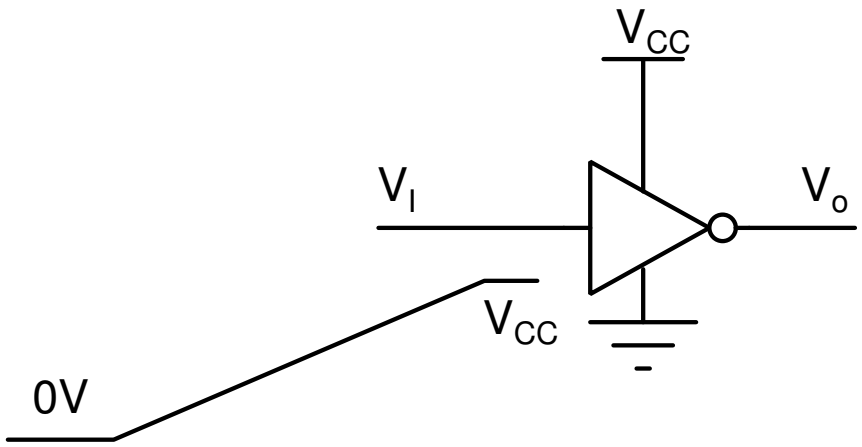


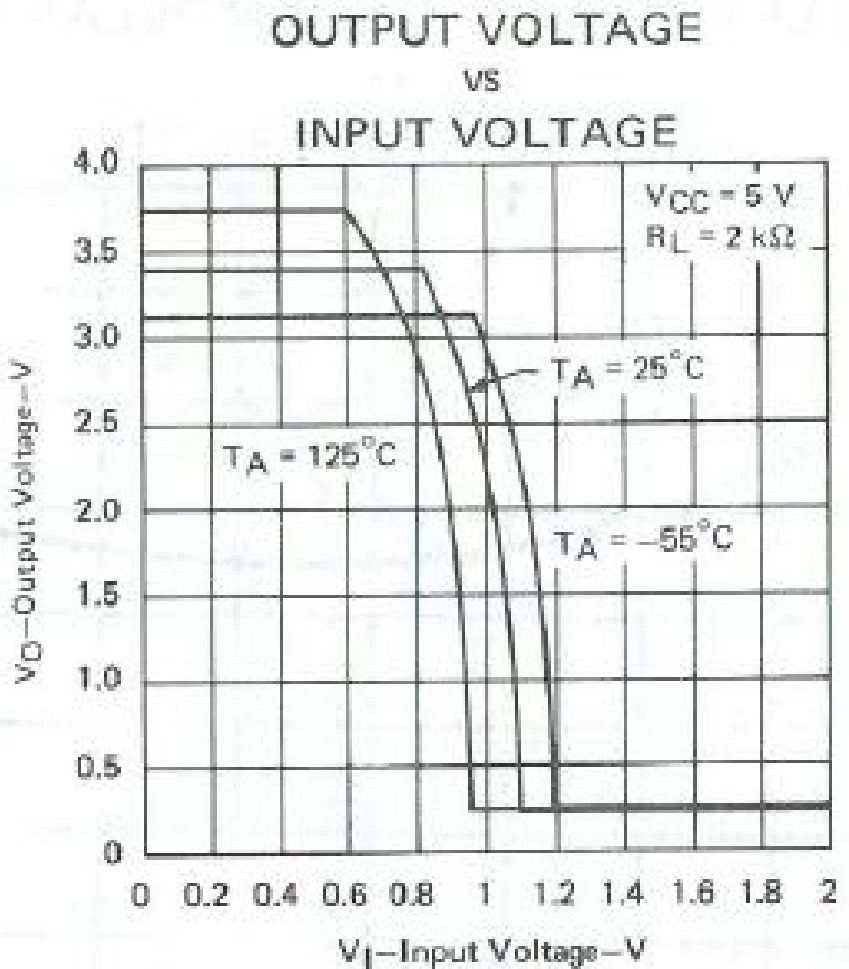
- Typical output high and low voltages (V_{OH} and V_{OL})
- Lowest output voltage that will be regarded as a logic 1 at the input. (V_{IH})
- Highest output voltage that will be regarded as a logic 0 (V_{IL})



Noise margins:
$NM_H = V_{OH} - V_{IH}$,
$NM_L = V_{IL} - V_{OL}$

Voltage transfer characteristics

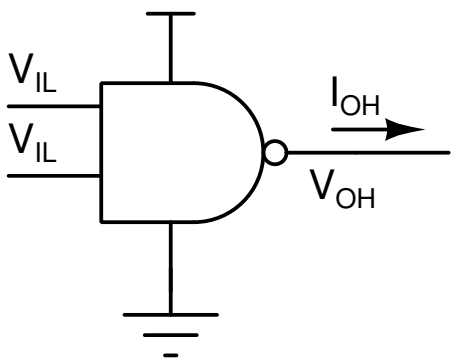


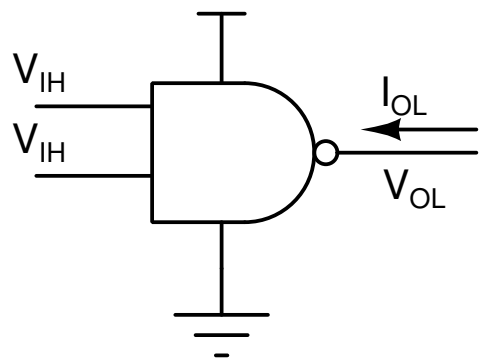


Static characteristics - input voltage is changed slowly.

Practical gates - 74xx LSTTL

	MIN	NOM	MAX	Units
Supply Voltage V_{CC}	4.75	5	5.25	V
High level output current I_{OH}			-400	μA
Low level output current, I_{OL}			8	mA
Operating free air temperature	0		70	$^{\circ}C$





	MIN	NOM	MAX	Units
High level input voltage V_{IH}	2			V
Low level input voltage V_{IL}			0.8	V
High level output voltage V_{OH}	2.7	3.4		V
Low level output voltage V_{OL}		0.25	0.5	V
High level input current, I_{IH}			20	μA
Low level input current, I_{IL}			-0.4	mA

Output characteristics

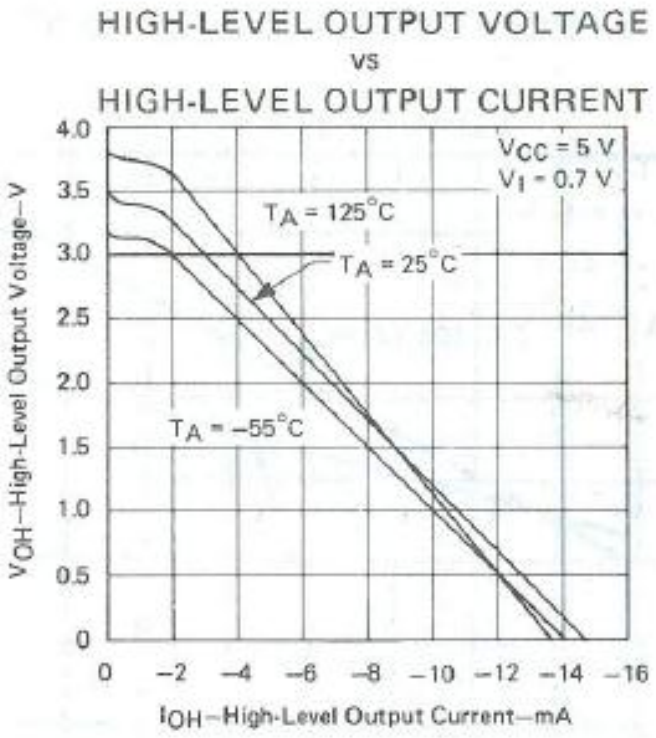


FIGURE D2

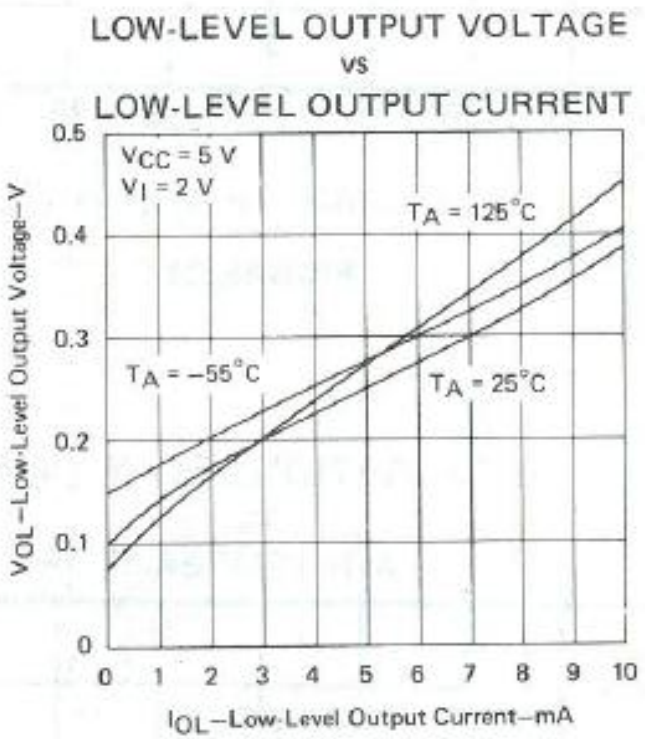
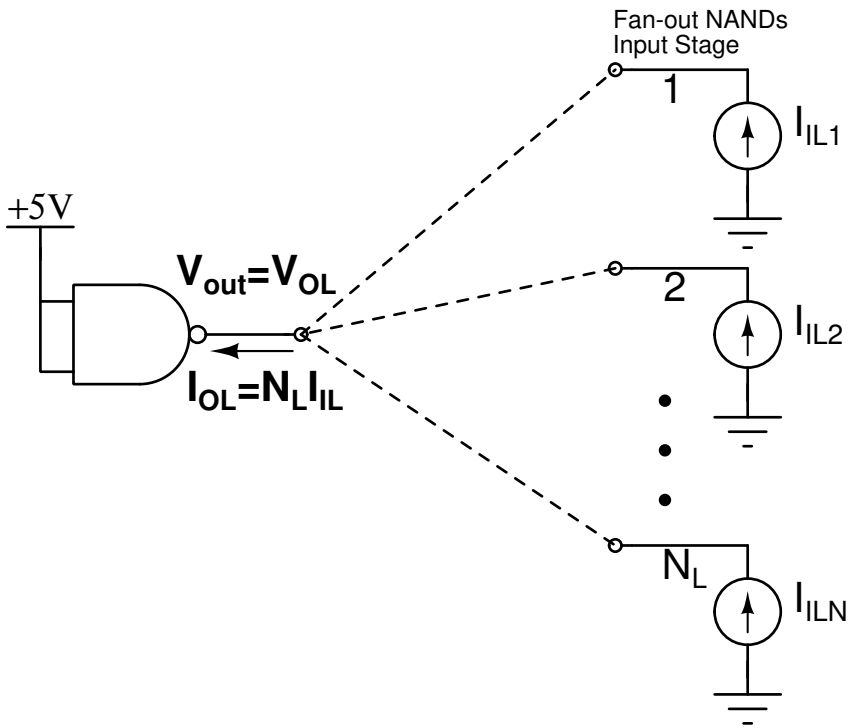
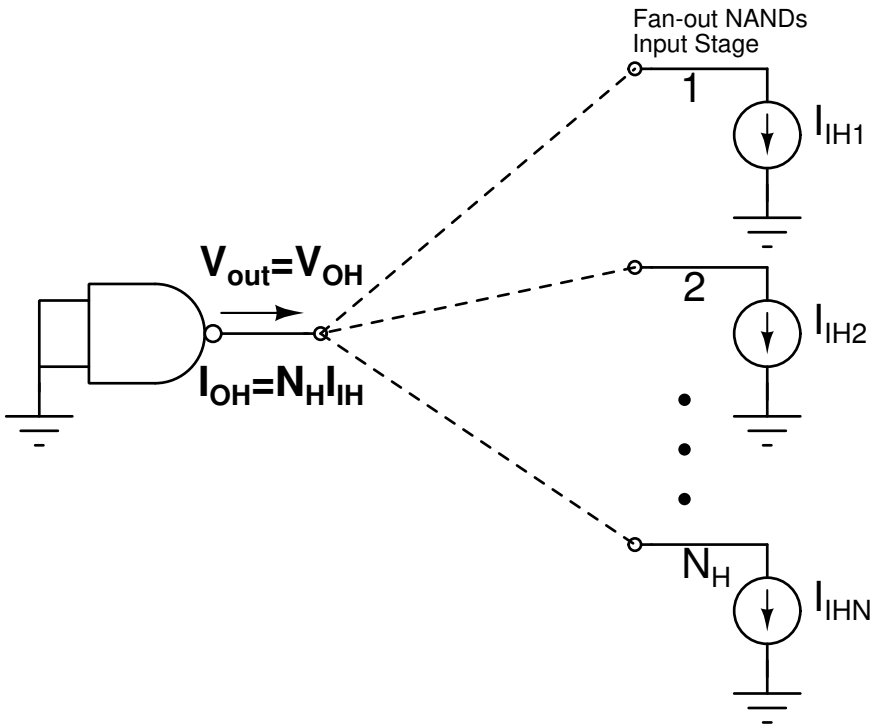


FIGURE D3

Maximum number of gates that can be connected when output voltage is low



Maximum number of gates that can be connected when output voltage is high



Fan-out of the gate is the minimum of $(N_H,\ N_L)$.

Practical Gates: Data sheets

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '00, '04, '10, '20, '30			SERIES 54H / SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L / SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS / SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S / SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−500			−100			−400			−1000	μA
	74 Family			−400			−500			−200			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			20			2			4			20	mA
	74 Family			16			20			3.6			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

Practical gates: Data sheets

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.7			0.7			0.8	V
				74 Family			0.8			0.8			0.7			0.8			0.8	
V_{IK}	Input clamp voltage	3	V_{CC} = MIN, I_I = §				−1.5			−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.25	0.5			0.5	
			I_{OL} = 4 mA	Series 74LS												0.4				
I_I	Input current at maximum input voltage	4	V_{CC} = MAX	V_I = 5.5 V			1			1			0.1						1	mA
				V_I = 7 V												0.1				
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			50			10							μA
				V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.3 V									−0.18							mA
				V_{IL} = 0.4 V			−1.6			−2						−0.4				
				V_{IL} = 0.5 V															−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX	54 Family	−20		−55	−40		−100	−3		−15	−20		−100	−40		−100	mA
				74 Family	−18		−55	−40		−100	−3		−15	−20		−100	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page															mA

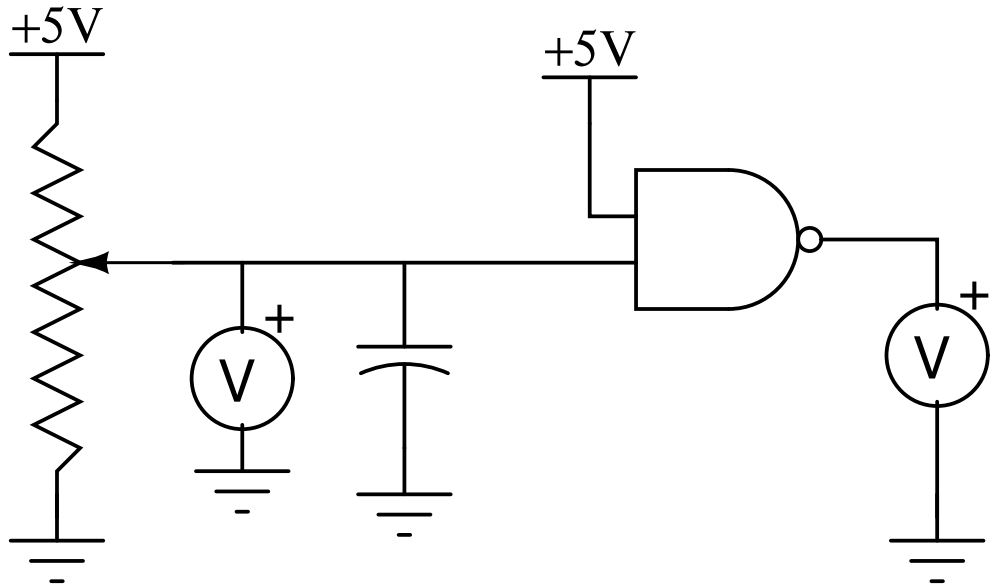
Experiment 4 - Input and Output characteristics of LSTTL gates

Objectives

1. To get familiar with data sheets of TTL logic gates
2. To understand various static logic gate characteristics: typical output high and low voltages, noise margins, input and output current levels and fanout.

Transfer characteristics

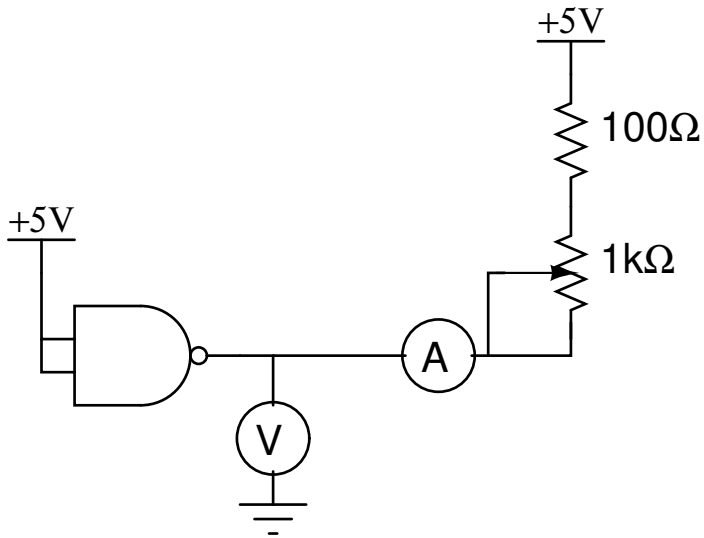
Using the following circuit , measure the output voltage while changing the magnitude of the input voltage slowly.



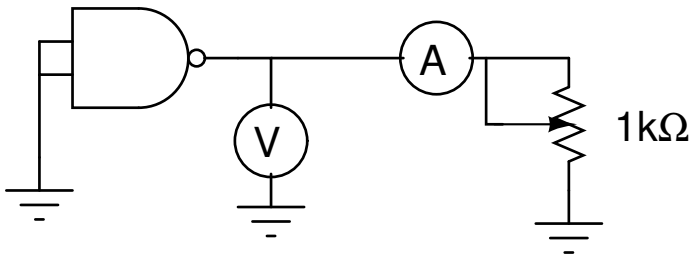
(1)

Output characteristics

Using circuit (3), measure the output current as a function of the output voltage when both the inputs of the NAND gate are in logic-1 state.
Using circuit (4), measure the output current as a function of the output voltage, when both the inputs are in logic 0 state.



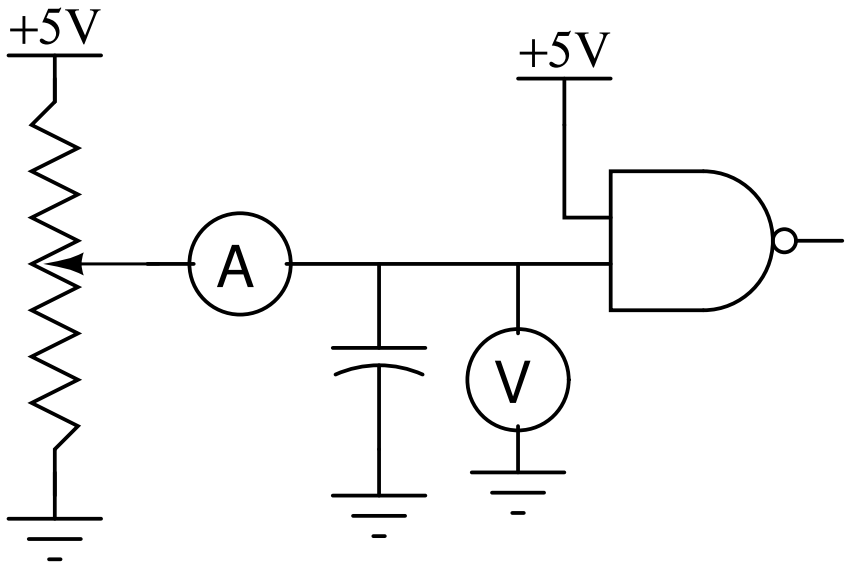
(3)



(4)

Input Characteristics

Using the following circuit, measure the input current as a function of the input voltage.



(2)

From these experiments find the fan-in and fanout of the NAND gate

General Instructions for all experiments

- First download datasheets for all components and get pin diagrams.
- Must strictly use a colour code for the wiring. For eg. use red wires for V_{CC}, black for ground and green for signals. This will make it easier to debug.
- Use the two vertical bars on the edges of the breadboard for V_{CC} and Ground.
- A circuit should a single reference voltage. All Grounds should be connected together, including that of the measuring instrument
- Connect V_{CC} and Ground of all components and do a simple functional check of each component before you start woring.
- All wires should be cut to the required length.

- Plan the layout of the circuit in such a way that there is enough free space for wiring and probing. Ensure that open ends of multiple wires do not touch each other.
- Check the wiring before powering up the circuit.
- Make any modifications after **disconnecting/switching off** the power supply.
- In case the outputs are different from the expected values, as a primary step in debugging, check if the V_{CC} and GND pins get their appropriate values in all the ICs used in the circuit.
- You should design and wire up the circuit on Monday. The lab session on Tuesday is meant for testing, debugging and understanding results.
- Each group should have a lab notebook that has the circuit design and a record of the results obtained. At the end of each session, get it signed by the teaching assistant.