Digital IC design

Elmore Delay model for RC trees

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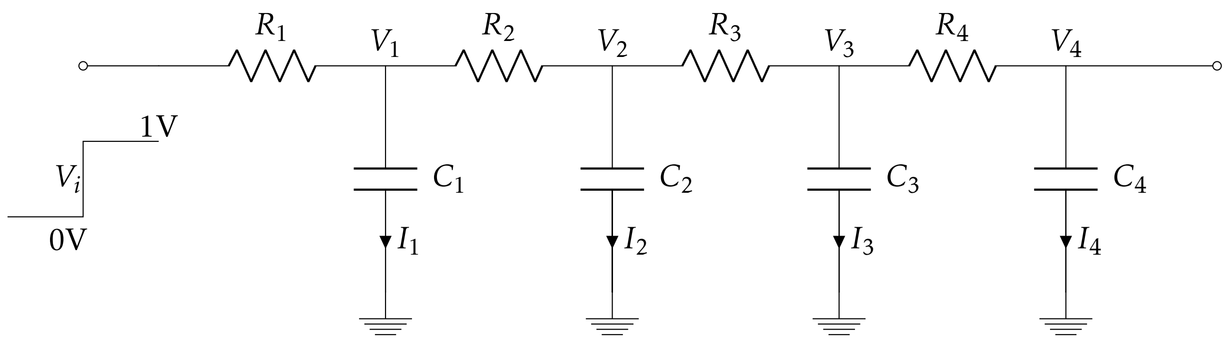
The Elmore delay model is used to appximate the delay through gates and interconnects modelled as RC trees. The method estimates the step response at the output of the RC tree network by estimating the dominant time constant τ, which is a measure of the delay. The output response is then approximately $1 - e^{-\frac{t}{\tau}}$. Consider the following simple RC tree.



$$
\begin{aligned}
V_4 &= V_i - (I_1 + I_2 + I_3 + I_4)R_1 - (I_2 + I_3 + I_4)R_2 - (I_3 + I_4)R_3 - I_4R_4 \\
&= V_i - I_1R_1 - I_2(R_1 + R_2) - I_3(R_1 + R_2 + R_3) - I_4(R_1 + R_2 + R_3 + R_4) \\
&= V_i - R_1C_1\frac{dV_1}{dt} - (R_1 + R_2)C_2\frac{dV_2}{dt} - (R_1 + R_2 + R_3)C_3\frac{dV_3}{dt} - (R_1 + R_2 + R_3 + R_4)C_4\frac{dV_4}{dt}
\end{aligned}
$$

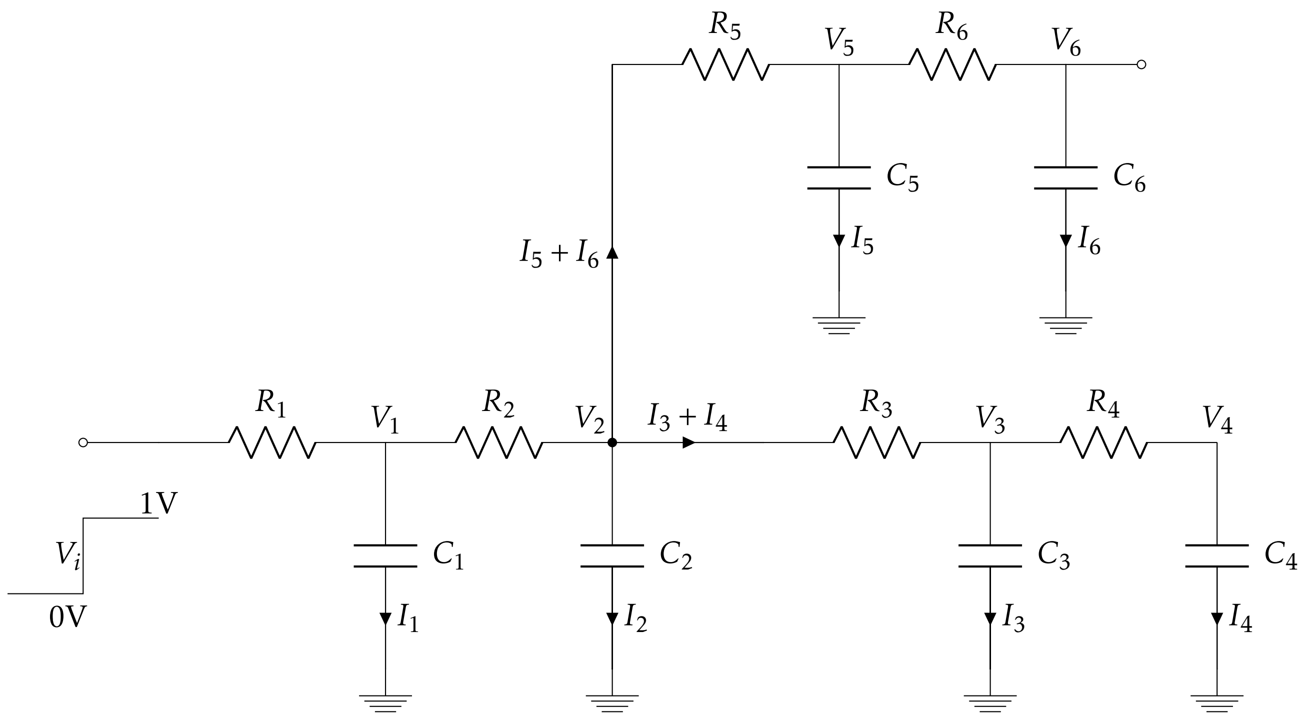
We know that the final voltage across all capacitors is 1V. Since we want to find the dominant time constant, lets approximate V_4 as $V_4 = 1 - e^{-\frac{t}{\tau}}$. Since $V_i = 1$V at $t = 0^+$, we have

$$
\begin{aligned}
&1 - V_4(t) = R_1C_1\frac{dV_1}{dt} + (R_1 + R_2)C_2\frac{dV_2}{dt} + (R_1 + R_2 + R_3)C_3\frac{dV_3}{dt} + (R_1 + R_1 + R_3 + R_4)C_4\frac{dV_4}{dt} \\
&\implies e^{-\frac{t}{\tau}} = \sum_{k=1}^{4}\left(\sum_{i=1}^{k} R_i\right)C_k\frac{dV_k}{dt}
\end{aligned}
$$

Integrating both from 0 to ∞ and noting that the final voltage is 1V on all nodes, we get the dominant time constant as

$$
\tau = \sum_{k=1}^{4}\left(\sum_{i=1}^{k} R_i\right)C_k
$$

What if the tree has branches, as in the following example?



Supposing we want to estimate the step response at V_6.

$$\begin{aligned}
V_6 &= V_i - (I_1 + I_2 + I_3 + I_4 + I_5 + I_6)R_1 - (I_2 + I_3 + I_4 + I_5 + I_6)R_2 - (I_5 + I_6)R_5 - I_6 R_6 \\
&= V_i - I_1 R_1 - I_2(R_1 + R_2) - I_3(R_1 + R_2) - I_4(R_1 + R_2) - I_5(R_1 + R_2 + R_5) - I_6(R_1 + R_2 + R_5 + R_6) \\
&= V_i - R_1 C_1 \frac{dV_1}{dt} - (R_1 + R_2)C_2 \frac{dV_2}{dt} - (R_1 + R_2)C_3 \frac{dV_3}{dt} - (R_1 + R_2)C_4 \frac{dV_4}{dt} \\
&\qquad - (R_1 + R_2 + R_5)C_5 \frac{dV_5}{dt} - (R_1 + R_1 + R_5 + R_6)C_6 \frac{dV_6}{dt}
\end{aligned}$$

Following a similar procedure as before (set $V_i = 1\text{V}$, $V_6 = 1 - e^{-\frac{t}{\tau}}$, integrate) and setting $p = \{1, 2, 5, 6\}$, $q = \{3, 4\}$ and $c = \{1, 2\}$ we get

$$\tau = \sum_{k \in p} C_k \sum_{\substack{i \in p \\ i \leq k}} R_i + \left(\sum_{k \in c} R_k \right) \left(\sum_{j \in q} C_j \right)$$

Note that p contains the indices of resistors and capacitors in the main path, q contains indices of capacitors in the branch and c contains indices of resistors common to the main path and the path from v_i to the branch (charging path for the capacitors in the branch).